PROCEEDINGS OF SCIENCE

The Silicon Vertex Detector of the Belle II Experiment

Thomas Bergauer*
HEPHY Vienna
E-mail: thomas.bergauer@oeaw.ac.at
for the Belle II SVD collaboration

The Belle experiment at the Japanese KEKB electron/positron collider has been successfully operating for more than ten years. A major update of the machine is foreseen between 2010 and 2014, resulting in a 40 times higher luminosity compared to the previous peak value. Since the previous detectors were already close to their operational limits in terms of occupancy and readout speed, large parts have to be upgraded, which leads to the Belle II experiment. The Silicon Vertex Detector (SVD) aimed for this upgrade will consist of four layers of double-sided silicon strip sensors, complemented by a two-layer inner pixel detector based on DEPFET technology. The sensors will be read out using the APV25 chip, originally developed for the CMS experiment at CERN. Several innovations like the Origami chip-on-sensor concept or readout electronics utilizing hit-time finding have been introduced for this project and will be presented in this paper. Moreover, test results of prototypes ranging from the silicon sensors to readout modules will be presented.

19th International Workshop on Vertex Detectors - VERTEX 2010
June 06 - 11, 2010
Loch Lomond, Scotland, UK

*Speaker.

PoS(VERTEX 2010)044

1. Introduction

The Belle detector, operating at the KEKB collider in Tsukuba (Japan), was commissioned 1999. In a decade of operation, it accumulated data of B-meson decays corresponding to an integrated luminosity of 1000 fb^{-1}. Measurements performed at Belle have offered important insights into the flavor structure of elementary particles, especially in the violation of the CP symmetry among quarks. Results of the Belle collaboration, together with data from its counterpart BaBar [1] at SLAC, led to the Nobel Prize in Physics for M. Kobayashi and T. Maskawa [2] for their theory of CP violation.

1.1 The Belle Experiment

The present Belle experiment was designed more than ten years ago [3]. It stopped data taking in June 2010 and parts of the detector are now disassembled. It consisted of different types of subdetectors which were arranged cylindrically around the beam pipe at the interaction point, which can be seen in figure 1. Since the accelerator provides asymmetric beams with 8 GeV electrons and 3.5 GeV positrons, respectively, the experiment was also not fully symmetric but spectrometer-shaped with asymmetric acceptance angles.

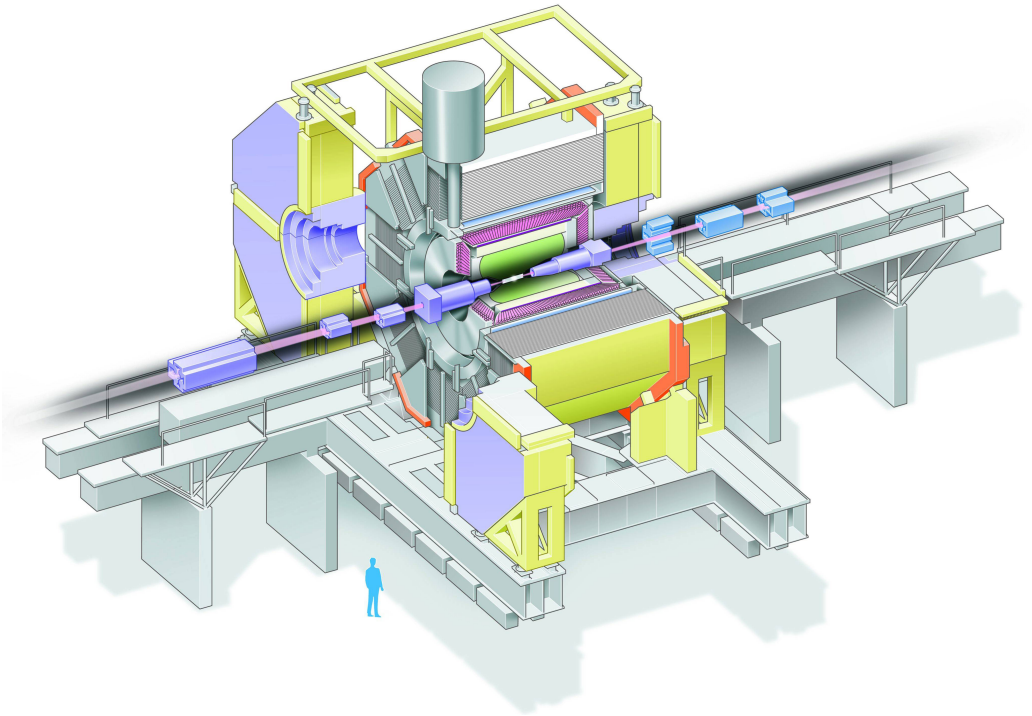

Figure 1: *Layout of the Belle Experiment.*

The innermost part is a vertex detector utilizing silicon strip detectors around the interaction point. Together with the Central Drift Chamber it allows particle tracking; the momentum is measured in a magnetic field of 1.5 T provided by a superconducting solenoid. Other components of the experiment are (from inside to outside) an Aerogel Cherenkov counter, a Time-of-Flight coun-

ters, and an electromagnetic calorimeter, surrounded by the superconducting solenoid and finally the K_L Meson and Muon detectors.

1.2 SuperKEKB and Belle II

The demand for high statistics measurements and precision studies of rare processes have led to an upgrade program for both the machine (KEKB $\rightarrow$ SuperKEKB) and the experiment (Belle $\rightarrow$ Belle II) until 2014, aiming at a peak luminosity of $8 \times 10^{35}\, cm^{-2}\, s^{-1}$. This is an increase by a factor of 40 compared to the world-record figure of the present Belle experiment. The design of the accelerator will use the so-called nano-beam option in the intersection region [4].

2. The Belle II Silicon Vertex Detector

The Silicon Vertex Detector of Belle, for historical reasons called SVD2, has been in operation since 2003. It is the innermost component of the former experiment and is composed of four layers of Double-Sided Silicon Sensors (DSSDs) at radii of 20, 43.5, 70 and 88 mm from the beam axis. According to the asymmetry of the Belle experiment, the SVD2 acceptance region covers the polar angle range between 17 and 150°. The sensors, built from 4" silicon wafers, are forming ladders, which are entirely read out from their edges outside of the acceptance region. The strips are daisy-chained and read out using the VA1TA chip of the Viking family with a shaping time of 800 ns. Because of the high luminosity provided by the machine, this results in occupancy problems, with hit rates of about 10% in the innermost layer. The occupancy problem is one of the major driving forces for a new SVD detector for the Belle II experiment.

As the luminosity will increase by a factor of 40, it is obvious that the old SVD will not work for Belle II. Therefore, a new detector is currently under construction. One major change compared to the existing SVD is the introduction of slanted forward detectors in order to reduce material budget and the total number of channels. Moreover, it will improve the signal-to-noise ratio of forward hits. Due to the asymmetry of the experiment, no slant angle for the backward region is needed. The forward part will be realized by trapezoidal sensors, as shown in a rendering of the new SVD in figure 2.

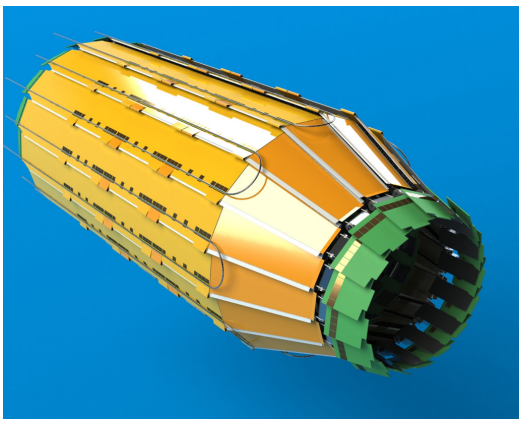

Figure 2: *Belle II SVD showing the ladders of the outermost layer. The trapezoidal sensors in the forward region are clearly visible.*

2.1 Layout

Similar to the SVD2, the future Belle II SVD will be equipped with four layers of DSSDs, but complemented by two inner layers of pixel detectors (PXD), which are based on the DEPFET technology [5]. For consistency, both pixel and strip ladders are numbered consecutively. A layout showing the position of the ladders can be seen in figure 3.

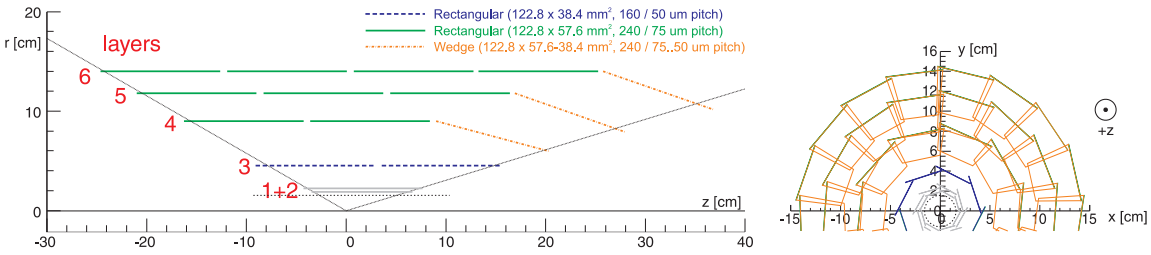

Figure 3: *Configuration of the four strip layers, with slanted sensors in the forward region, and the two PXD layers.*

The geometry is mainly driven by the achievable sensor size in six-inch wafer technology (see next section) and how to fit integer multiples thereof within the acceptance region. Table 1 gives details about the number of sensors and ladders per layer.

Layer	**Radius** (mm)	**Ladders**	**Sensors /ladder**	**Sensors**	**RO chips /sensor**	**RO chips**
6	140	17	5	85	10	850
5	115	14	4	56	10	560
4	80	10	3	30	10	300
3	38	8	2	16	12	192
Sum		49		187		1902

Table 1: Geometrical properties of the Belle II SVD. As the sensors are flat, the radii given here are the minimum distances from the beam axis. "RO chips" stands for the number of APV25 readout chips. For coherence with the PXD layer numbering scheme, the innermost strip layer is 3.

The slanted forward region requires sensors of trapezoidal shape, and only one design is foreseen to be used in all layers. The slant angle varies in such a way that the non-parallel strips of those sensors all intersect with the beam pipe. In reality, this condition cannot exactly be met due to the windmill structure (see figure 4).

This structure is caused by the *Origami* chip-on-sensor concept (see section 2.4 below), which will be applied to all sensors except those located at the edge of the acceptance. It foresees pitch adapters bent around the sensor edge. These bent fanout pieces can only be applied at the outer sides in a windmill structure, as shown schematically in Fig 4. Together with the readout direction, this unambiguously determines the layout of each hybrid.

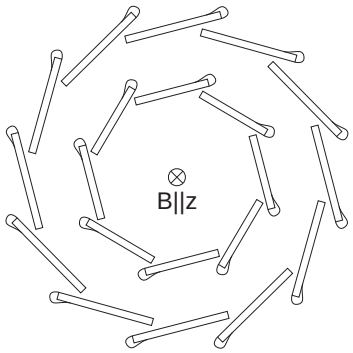

Figure 4: Schematic cross-section of a windmill structure with Origami modules. The flex pitch adapters, which are bent around the sensor edges, can only be placed on the outer edge of each sensor.

2.2 Double Sided Silicon Sensors

The design of the silicon sensors is driven by the fact that material reduction is the most crucial item for the Belle II experiment. Thus, the largest available sensors have to be used and the design has to be double-sided to achieve a low material budget. Nowadays, typical wafer processing facilities are able to produce six-inch wafers, so this wafer size has been chosen for the production of the sensors.

The entire SVD is composed of only three different sensor types, which is shown in figure 3. Two of them are rectangular for the barrel part. Since the innermost layer uses a narrower pitch, but the same number of strips as the outer layers, those sensors are smaller in width. The third design is trapezoidal for the slanted forward part. All sensors are about 300 micron thick with orthogonal strips on opposite faces, with the strips on the p-side facing parallel to the beam axis. A floating, non-readout intermediate strip is placed between pairs of readout strips. On the n-side of the detector, strip insulation is achieved using p-stop technique. The bulk resistivity was defined such that the full depletion voltage is between 40 Volts and 120 Volts, corresponding to a resistivity of 3 to 8 $k\Omega cm$. Table 2 lists the dimensions of the different sensor types and their key parameters.

Hamamatsu Photonics (HPK), the Japanese company that provided the DSSDs on four inch wafers for the SVD2 in the past, had decided some time ago to quit the production of doubled-sided sensors. Therefore, a market survey was started to investigate which alternative vendors exist. As a result, a prototype batch of trapezoidal sensors for the forward part has been designed and ordered at Micron Semiconductor (UK). Meanwhile, HPK announced that they are restarting the production of DSSDs. Therefore, a test order was launched with HPK for the barrel sensors.

The first batch of HPK sensors has been intensively tested and results from IV and CV curves are shown in figure 5. Strip-by-strip measurement results reveal roughly 5% non-working strips per sensor, which is confirmed by HPK data. Since this production is the very first test of a new production line and only for evaluation purposes, the Belle quality cuts have not been applied yet and no detailed data are presented. The next, improved batch is expected back in autumn this year and is supposed to reduce the number of non-working strips.

For the trapezoidal forward sensors, Micron Semiconductor was chosen as supplier for a prototype batch. A detailed design of those sensors has been developed (see figure 6). First prototype

Quantity	Large sensor	Small sensor	Trapezoidal sensors
SVD layer(s)	3	4, 5 and 6 (barrel)	4, 5 and 6 (forward)
length	122.9 mm	122.9 mm	125.58 mm
width	59.6 mm	38.4 mm	57.59 … 38.42 mm
depletion voltage	$< 120V$		40 V (typ.), 70 V (max.)
thickness	320 μm	320 μm	300 μm
# readout strips p-side	768	768	768
# readout strips n-side	512	768	512
pitch p-side	75 μm	50 μm	75…50 μm
pitch n-side	240 μm	160 μm	240μm
Slant angles			Layer 6: 21.1° Layer 5: 17.2° Layer 4: 11.9°

Table 2: Basic parameters of the double sided sensors.

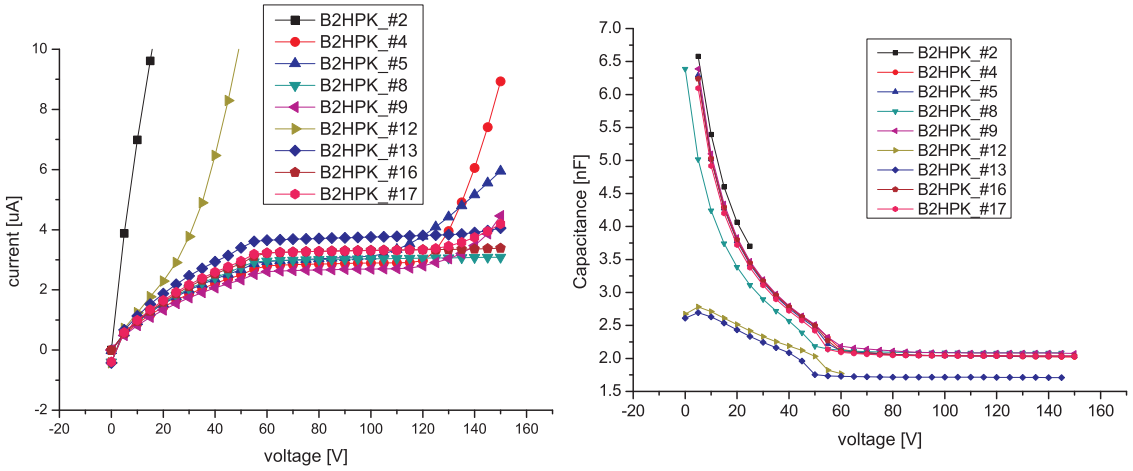

Figure 5: Results of electrical characterization of HPK double sided silicon sensors. Dark current versus voltage behavior (left) and capacitance versus voltage (right) behavior.

sensors of this design have been received very recently from the vendor and are currently under electrical characterization. After thorough testing on the sensor level with strip-by-strip characterization and longterm stability tests, these devices will be used for building full-size prototype ladders.

2.3 Front-End Readout

As mentioned earlier, the occupancy problem is a driving factor for a new SVD readout chain. The shaping time of the front-end readout amplifier is the most crucial element in this respect. Rather than taking the enormous effort of designing a new chip, we decided to use the existing, well-tested and radiation-hard APV25 chip [6], which was originally developed for the CMS experiment at the LHC. This chip perfectly fits the needs of Belle II. Compared to the 800 ns of the

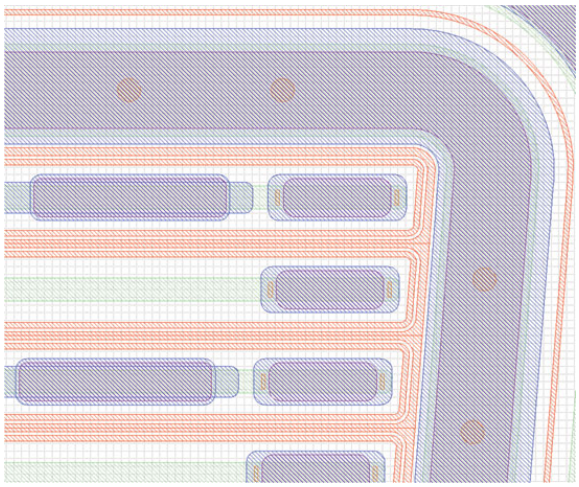

Figure 6: *One corner of the trapezoidal sensor design on the n-side. Four strips (horizontal) and a part of the bias line are shown with the p-stop atolls in red and the implant strips in green. The contact windows in the passivation are given in blue.*

VA1TA chip, the shaping time of the APV25 is just 50 ns. Moreover, an internal pipeline of 192 cells allows a certain trigger latency and to record subsequent triggers while reading out data from previous events.

2.3.1 Hit time finding

For LHC operations, the APV25 chip is operated in the so-called *deconvolution* mode [7] to narrow down the sensitive time window. However, this needs clock-synchronous particle hits at LHC frequencies and thus cannot be used for Belle II because of the quasi-DC beam [8]. Nevertheless, the APV25 can be configured to record the signal in (multiples of) three consecutive clock cycles. This feature can be used to scan the shaping curve upon the reception of a trigger. Once the shaping curve is known, off-detector data processing can be used to apply a numerical fit, yielding peak amplitude and timing. This so-called *hit time finding* allows to discard off-time background hits and minimize the overall occupancy. Figure 7 summarizes the methods used to achieve the goal of minimizing the occupancy by a factor of 100 in total. This procedure was tested on several prototype detector modules in various beam tests during the past years. The overall result is an RMS timing resolution of typically 3...4 ns with cluster signal-to-noise values between 12 and 15 [9].

2.4 Origami Chip-on-Sensor Concept

One drawback, which comes along with faster shaping times of the readout chip, is a higher noise figure. With 250 e + 36 e/pF, the APV25 performs excellent compared to its competitors. Obviously, these numbers are higher than that of the VA1TA chip with 180 e + 7.5 e/pF, especially if one compares the capacitance-dependent slope. One consequence is that daisy-chaining of several detectors to form long strips is no longer an option with the APV25, as its input capacitance and thus the strip length as well as any pitch adapter must be minimized.

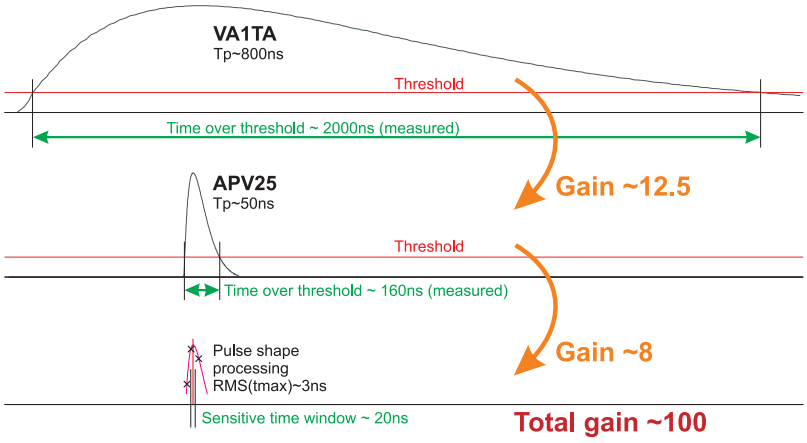

Figure 7: *The occupancy reduction from Belle to Belle II by a factor of 12.5 is achieved by reducing the shaping time from 800 ns (with the old chip) to 50 ns using the APV25 readout chip. By using hit time finding, this can be further reduced by a factor of 8, resulting in a total gain of 100.*

Therefore, the only solution to overcome this problem is to place the readout chips as close as possible to the silicon sensors. This leads to what we call the *Origami* chip-on-sensor concept, shown in figure 8. The module consists of a rectangular silicon sensor described in section 2.2. It

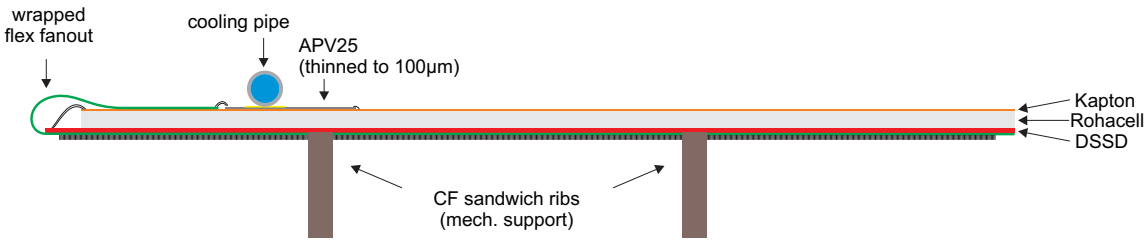

Figure 8: *Side view of the Origami chip-on-sensor concept for a 6" DSSD. The wrapped flex, which connects the strips of the bottom side, is located at the left edge.*

is covered by a 1 mm thick layer of Rohacell, a low density, but rigid foam used for thermal and electrical insulation. A Kapton flex is placed on top, on which the APV25 readout chips are glued and which contains electric circuits implemented in $5\mu m$ thin copper layers. The strips of the top (n-)side of the sensor are connected to it by wire-bonds. For the bottom side of the sensor (p-side), two flex fan-outs are wrapped around the sensor edge. This arrangement allows to place all readout chips in one row on the top side of the module while having just one, thin cooling pipe for heat dissipation from the chips. A picture of the Kapton flex hybrid, the two fan-outs and the silicon sensor before folding is shown in figure 9. In a relatively complicated procedure, the flex fan-outs have to be bent around the sensor, without damaging the wire-bonds underneath. A customized vacuum positioner, used in this process, is shown in figure 10.

2.5 Mechanics

The *Origami* structure consisting of silicon sensor, Rohacell and Kapton layers is carried by

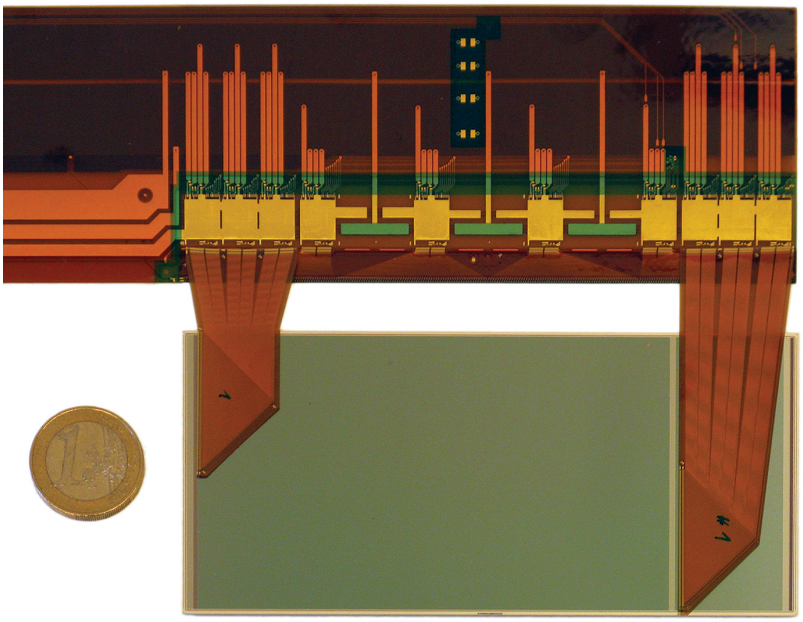

Figure 9: *Six-inch wafer DSSD ($\approx 125 \times 60\,\mathrm{mm}^2$), Origami hybrid ($\approx 445 \times 57\,\mathrm{mm}^2$; only about a third is shown here) and pitch adapters arranged in the Origami style, but not folded.*

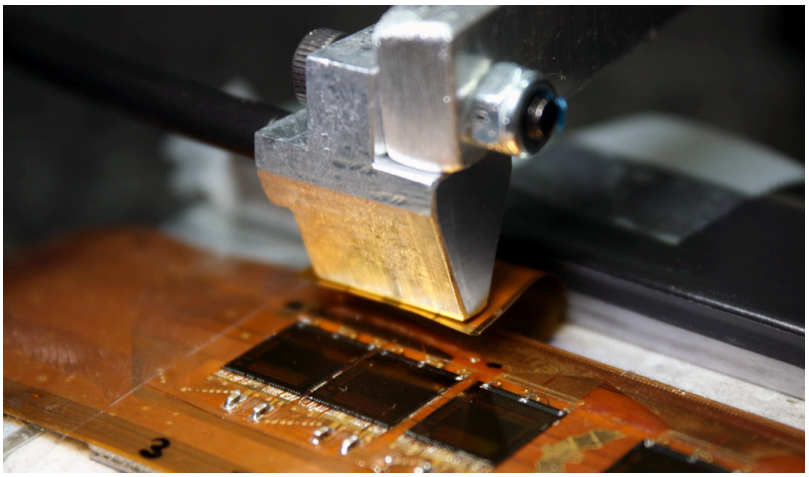

Figure 10: *Origami module: Bending and positioning of the flex fan-outs.*

two ribs composed of a sandwich structure of carbon fiber and Rohacell. Four modules with rectangular sensors and one trapezoidal sensor are needed to build up a ladder of the outermost SVD layer (see figure 3). A finite-element analysis has been performed to calculate the gravitational sag caused by the rib design. It was found that the Rohacell layer of the ribs must be of 2 mm thickness to keep the sag always $< 100\mu m$. This design guarantees a low material budget of only 0.58% of X_0 in average for the full ladder.

2.6 Cooling

One APV25 chip dissipates approximately 350 mW of power. Signal-to-noise improves by

approximately 20% at $-10°$C compared to the uncooled condition. The *Origami* concept needs only one cooling pipe per ladder, which is directly attached to the top of the APV25 readout chips. A very thin pipe has to be used to keep material budget on a reasonable level. As the SVD is close to the PXD, a common cooling concept will be established. A dual-phase CO_2 approach is the baseline, since it allows relatively low temperatures at minimal material expense, but with the drawback of high pressures. However, high pressure also occurs in conventional mono-phase cooling system if the pipe diameter has to be kept low because of material budget considerations. A prototype blow system is now being designed. Based on the gained experience, a close-loop system will be constructed, which will be based on the well-working design of LHCb [10].

3. Summary

The KEKB accelerator is the highest luminosity machine in the world. An elaborate upgrade of KEKB and Belle until 2014 is planned to result in an 40-fold increase in luminosity for high-precision measurements and study of rare processes. This needs upgrades of all sub-detectors, especially a new, enlarged Silicon Vertex Detector. It will consist of two DEPFET pixel layers, complemented by four layers equipped with double sided strip detectors.

The largest currently available sensors on six inch wafers will be used to minimize the amount of support structure material. Prototype batches have been ordered at Hamamatsu for barrel sensors and at Micron Semiconductor (UK) for trapezoidal sensors, respectively.

The APV25 readout chip with fast shaping time has been chosen for the readout. Complemented by hit-time-finding, the occupancy will be reduced by a factor of 100 compared to the current system. To maintain a reasonable signal-to-noise ratio, the capacitive load on the amplifier inputs has to be minimized, which leads to the *Origami* chip-on-sensor layout. Together with low-mass ribs as support structures and thin CO_2 cooling pipes the module design guarantees a low material budget. With these techniques, the Silicon Vertex Detector for the Belle II experiment will be ready for the challenges of the future SuperKEKB accelerator starting in 2014.

References

[1] B. Aubert et al., **The BaBar Detector** Nucl. Instrum. Meth. A479, 1 (2002), hep-ex/0105044, 10.1016/S0168-9002(01)02012-5

[2] The Nobel Prize in Physics 2008, http://nobelprize.org/nobel_prizes/physics/laureates/2008/

[3] A. Abashian et al., **The Belle Detector** Nucl. Instrum. Meth. A479, 117 (2002), 10.1016/S0168-9002(01)02013-7.

[4] Z.Dolezal, S.Uno (ed.), **Belle II Technical Design Report**, KEK Report 2010-1 (July 2010)

[5] C. Marinas (for the DEPFET collaboration), **The Belle-II Pixel Vertex Tracker at the SuperKEKB Flavour Factory**, Nucl. Instr. and Meth. 2010 (article in press), doi:10.1016/j.nima.2010.06.292

[6] M.French *et al.*, **Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker**, Nucl. Instr. and Meth. A 466 (2001), 359–365

[7] S.Gadomski *et al.*, **The Deconvolution Method of Fast Pulse Shaping at Hadron Colliders**, Nucl. Instr. and Meth. A 320 (1992), 217–227

[8] KEKB B-Factory Design Report, KEK Report 95-7.

[9] M.Friedl, C.Irmler, M.Pernicka, **Readout and Data Processing Electronics for the Belle-II**, TWEPP-09, CERN-2009-006, 417–421, http://cdsweb.cern.ch/record/1235848/files/p417.pdf

[10] Martin van Beuzekom, Ann Van Lysebetten, Bart Verlaat, **CO_2 cooling experience at LHCb**, PoS (Vertex 2007) 009