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Development of the L1 track trigger for the ATLAS high luminosity upgrade

R. Brenner[*] **(on behalf of the ATLAS collaboration)**
Department of Physics and Astronomy, Uppsala University, Uppsala, Sweden
E-mail: `brenner@mail.cern.ch`

The planned luminosity upgrade of the Large Hadron Collider (LHC) will require several improvements in the ATLAS detector to manage the higher event rates and detector occupancy. A complete replacement of the Inner Detector (ID) is required since the present tracker will not manage the increase in hit occupancy and radiation levels generated by the upgraded LHC machine (SLHC). Also the trigger system needs to be improved to handle the higher data rates to maintain good physics performance. Taking advantages of these two major upgrades, ATLAS is studying the feasibility to include information from the tracking detectors already in the fast L1 trigger decision. In this paper the challenges and possible solutions to implement a track trigger in ATLAS is presented.

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[*] Speaker.

1. Introduction

The LHC has been in continuous operation since the end of March 2010 providing collisions at $\sqrt{s} = 7TeV$. In a few years the collider is expected to provide collisions at the double energy and at a luminosity of $10^{34} cm^{-2} s^{-1}$.

Although the LHC operation and data collection of the experiments are in an early phase, the planning of an upgrade of the LHC machine has started [1]. The energy of the machine cannot be upgraded without a full replacement of all the magnets in the ring but with upgrades in the interaction region the luminosity can be increased by an order of magnitude to about $10^{35} cm^{-2} s^{-1}$. The early start of the upgrade work is motivated by the long time it takes to develop, produce and install accelerators and detectors. The drawback is that little is known about the physics to be explored after the upgrade.

Before the upgrade the existence of the Higgs boson and physics beyond the Standard Model has most likely been discovered or ruled out to the energy limit of the machine. Since only the luminosity will be upgraded only physics studies that are statistics limited at LHC will benefit from the upgrade. The gain can however be lost if the data selection and collection efficiency at SLHC is worse than at LHC.

One major challenge at SLHC will be the sensitivity and performance of the first level trigger (LVL1). The present ATLAS LVL1 trigger decision is based on input from the muon chambers and the calorimeter system only. No tracking is included and the reason is that the tracking detectors cannot be read out fast enough for the trigger decision. With the trigger bandwidth of 100 kHz already saturated at LHC, thresholds will need to be raised or the trigger made more selective to maintain performance. There are fortunately room for improvements of the trigger. A big fraction of the LVL1 trigger bandwidth is presently filled with fake triggers due to limited granularity of the trigger detectors resulting in wide slopes on trigger thresholds and fakes from ambiguities, cavern background and pile-up. The fraction of fake triggers can be reduced if information from the high granularity tracking detectors are used in the trigger. The effect using tracking information in the trigger can easily be seen by comparing the performance of the present LVL2 trigger with and without tracking included. Several studies are ongoing investigating the effect of the tracking on the LVL1 trigger rates, thresholds, efficiencies and purities. An example is to study the effect of combining the present LVL1 trigger with a simulated track trigger that is based on the present track LVL2 trigger algorithms. It may not be possible to build a LVL1 track trigger of the same quality as the present LVL2 trigger, hence the effect of a degraded algorithm is studied. Preliminary results based on simulation studies of the present detector layout, shown in Fig. 1, indicate that the effect is small even if the pT resolution of the LVL1 track trigger is 2.5 times worse than the present LVL2.

The studies are also important for defining requirements for a track trigger. Even if initial results are encouraging large challenges remain. The perhaps biggest challenge is to instrument the tracking detector with trigger functionality without increasing the power and material budget of the tracker since every increase in the material budget will affect both the trigger and off-line performance.

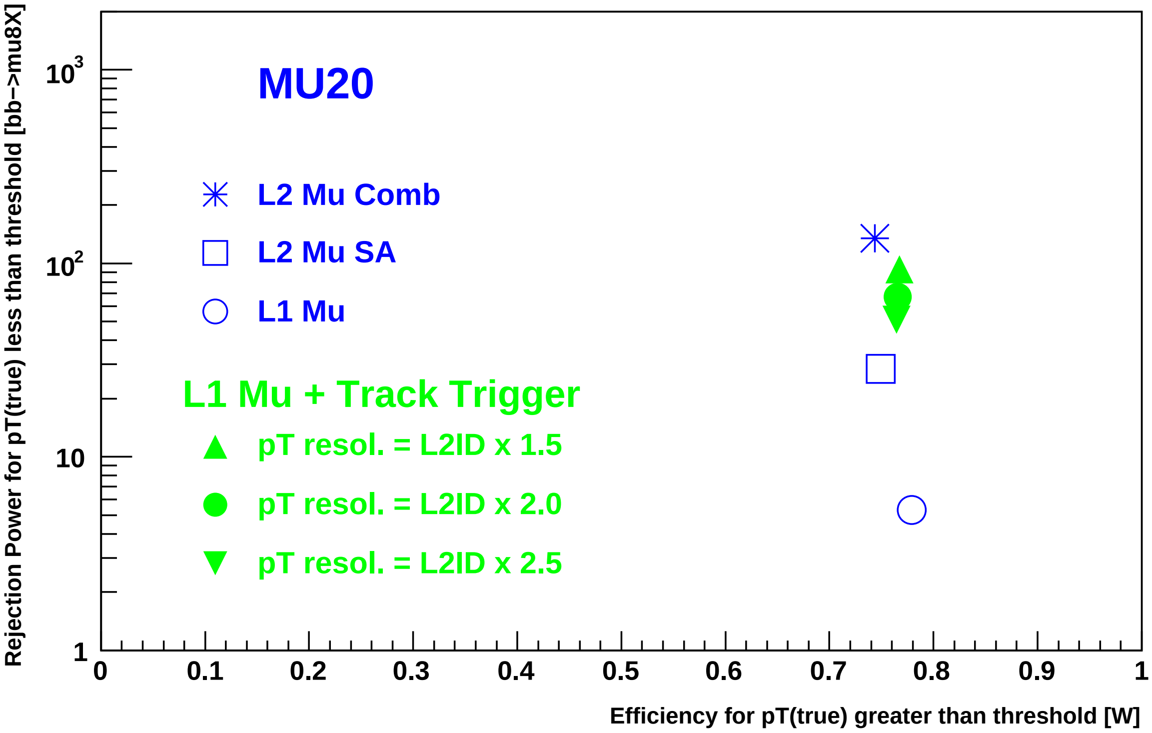

Figure 1: The plot shows the trigger rejection vs. efficiency for a 20 GeV muon with the LVL1 muon trigger combined with a LVL2 track trigger where the pT resolution of the track trigger has been degraded 1.5,2 and 2.5 times to simulate a possible future LVL1 track trigger. For comparison the corresponding points for a L1 muon, L2 stand-alone and a combined L2 muon + track trigger are presented.

2. Track trigger concepts

From the 40 million events produced every second in ATLAS a maximum of 100 thousand are selected by the LVL1 trigger. The full tracker is presently read out only upon an accepted LVL1 trigger. If the tracker was read out at the event production speed the bandwidth would have to be increased 400 times. To contribute to the LVL1 trigger the tracker has to be capable of sending information to the central trigger processor at 40 MHz with latencies well within the trigger latency. The trigger latency is today limited by the pipeline lenght in the SemiConducter Tracker which is 3.2μs but the lenght is going to be doubled at SLHC. The gain in latency is however not expected to double at SLHC since there are other detectors that in turn will limit the latency if not upgraded. Since the bandwidth cannot with today's technology be significantly increased without a major impact on material budget, the amount of data sent from the tracker to the trigger processors has to be decreased. ATLAS is investigating two concepts for instrumenting the track trigger. The two are conceptually very different with challenges in different parts of the system. The Region-of-Interest concept requires no modification to the layout of the tracker and modest modifications to the front-end electronics but has a large impact on the ATLAS trigger and data acquisition architecture. Futhermore the concept relies on seeding from the calorimeter or muon systems. The concept has been described in detail at Vertex 2009 [2]. The momentum discrimination concept was originally developed by CMS [3] for track triggering upgrade and it is self-seeded running in parallel with

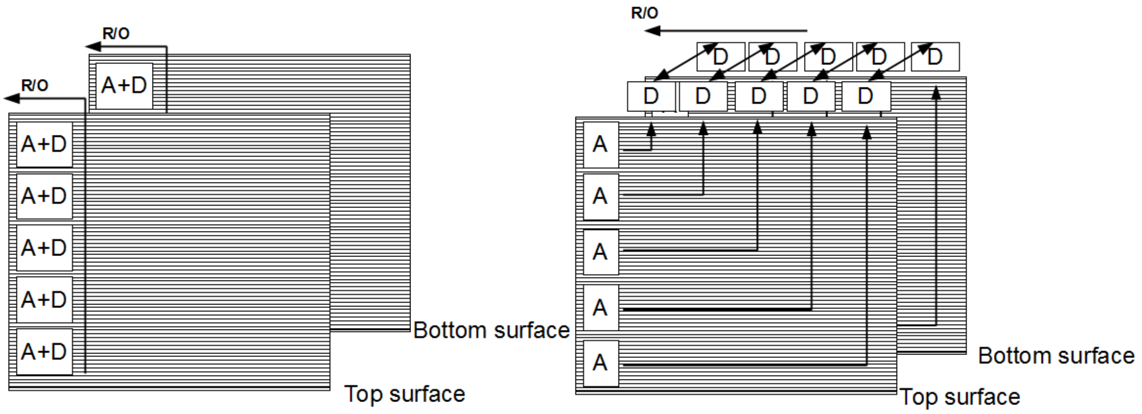

Figure 2: A schematic comparison between the present stave layout for SLHC (left) and a modified stave layout with trigger functionality (right).

the calorimeter and muon systems. The implementation of the concept in the design of the present ATLAS tracker upgrade will be discussed here in more detail.

2.1 Momentum discrimination concept

Data reduction can be achieved if hits from only high momentum tracks are selected and transferred from the tracking detector. For this to work on-detector intelligence capable of momentum discrimination is required. The magnitude of data reduction depends on the achieved momentum threshold.

The basic concept of momentum discrimination is based on two closely spaced doublet layers of silicon micro-strip detectors with the strips on both layers aligned with magnetic field in the tracker. High momentum tracks are bent less by the magnetic field than low momentum tracks giving a smaller transversal shift between clusters on the two silicon layers. By optimizing the spacing between layers and the detector pitch the desired momentum threshold can be selected. For a reduction of 400 on tracks coming from the beam spot a momentum threshold of around 5 GeV is required. The momentum discrimination concept does however not reduce fakes from secondary tracks since they do not come from the beam spot.

The present tracker layout has three layers of pixel detectors at small radius plus one b-layer of pixel detectors very close to the beam, three layers short strip detectors (2.5 cm long) at medium radius and two layers of long strip detectors (10 cm long) at large radius. The silicon strip layers consist of stave assemblies with two closely spaced silicon strip sensors [4]. The two sensors are rotated slightly with respect to each other to give 2D hit information. The aim of the stave design is to make a very low mass structure with good thermal and electrical performance to cover a large area tracker. The stave was not designed particularly with the trigger in mind but the structure has the potential to be equipped with trigger. The trigger functionality can be accomplished with a minor addition of material if the front-end electronics is split into two parts, as shown in Fig. 2, where the position of the analogue part is as in the base-line stave design and the position of the digital part is moved to the edge of the sensor allowing hit correlation between the two silicon layers [5].

It is essential to leave the analogue part of the electronics in place not to degrade the performance by increasing capacitance and series noise from routing. The binary signals that are generated by the discriminators in the analogue circuit are less sensitive to capacitance and series resistance when routed to the digital circuit. The design requires a fine pitch interconnect between the analogue and digital parts. For the concept to work the stereo angle between the silicon sensors has to be removed which may degrade the off-line performance. The z-coordinate may also be needed for the trigger since the muons detected in the muon spectrometer are bent by the toroidal field in the z-direction. These are the biggest differences together with the weaker magnetic field that makes ATLAS different from CMS where a twice stronger solenoidal field bends the muons in the ϕ-direction.

The effect of removing the z-coordinate on the off-line performance and the matching muons in the muon spectrometer with tracks in the tracker for the trigger are the two most important studies that need to be done to evaluate the feasibility of the momentum discrimination concept.

3. Technology for on-detector intelligence and fast data processing

To meet the latency of the LVL1 trigger the data, once transmitted from the tracker, needs to be rapidly processed. Conventional reconstruction with computers cannot be done fast enough hence dedicated hardware for fast pattern recognition is required. A technology originally developed for CDF is now being further developed and implemented in the Fast Track, FTK, trigger project for ATLAS [6]. The core of the system is a custom-made Associative Memory (AM) hardware processor that compares the data from the tracker with predefined patterns. The FTK is designed to run as an extra layer between the LVL1 and LVL2 trigger at LHC with a luminosity up to $10^{34} cm^{-2} s^{-1}$. The system could conceptually be used at SLHC if the system was designed to match the higher data rates and shorter trigger latency.

A system under study for SLHC is based on ternary Content-Addressable-Memories (CAM) for storage and matching of patterns with tracking data [7]. The figure of merit for the technology is a very large storage space, fast pattern matching and reduction of the number of required patterns by the use of wild-cards, ’don’t care bits’, in the pattern definitions. Studies have been performed on the upgrade tracker design (barrel only) and show that the inclusion of the three short double strip layers in the trigger gives few fake tracks if the hit occupancy is low. Better result can be acieved with inclusion of more layers in the pattern matching but that will require more patterns and have a larger impact on the ID layout. that the spacing of the three short layers in the present baseline layout is not good for triggering purposes. The distance between the three short strip layers has to be reduced to half, to 6 cm, for good trigger performance. The effect of this change on off-line performance has to be studied.

The performance of the fast pattern matching hardware is heavily depending on the hit occupancy in the input data. It is also much more important that the hits that reach the trigger processors have good quality rather than high position resolution. Fig. 3 shows the relation between occupancy and number of fake tracks for random hits. The occupancy can be reduced by several measures. A small quality improvement can already be achieved by selecting clusters in a silicon plane that are 1 or 2 strip wide. The effect is however small since the momentum threshold it gives is low because of the relatively low magnetic field in ATLAS. The momentum discrimination with the

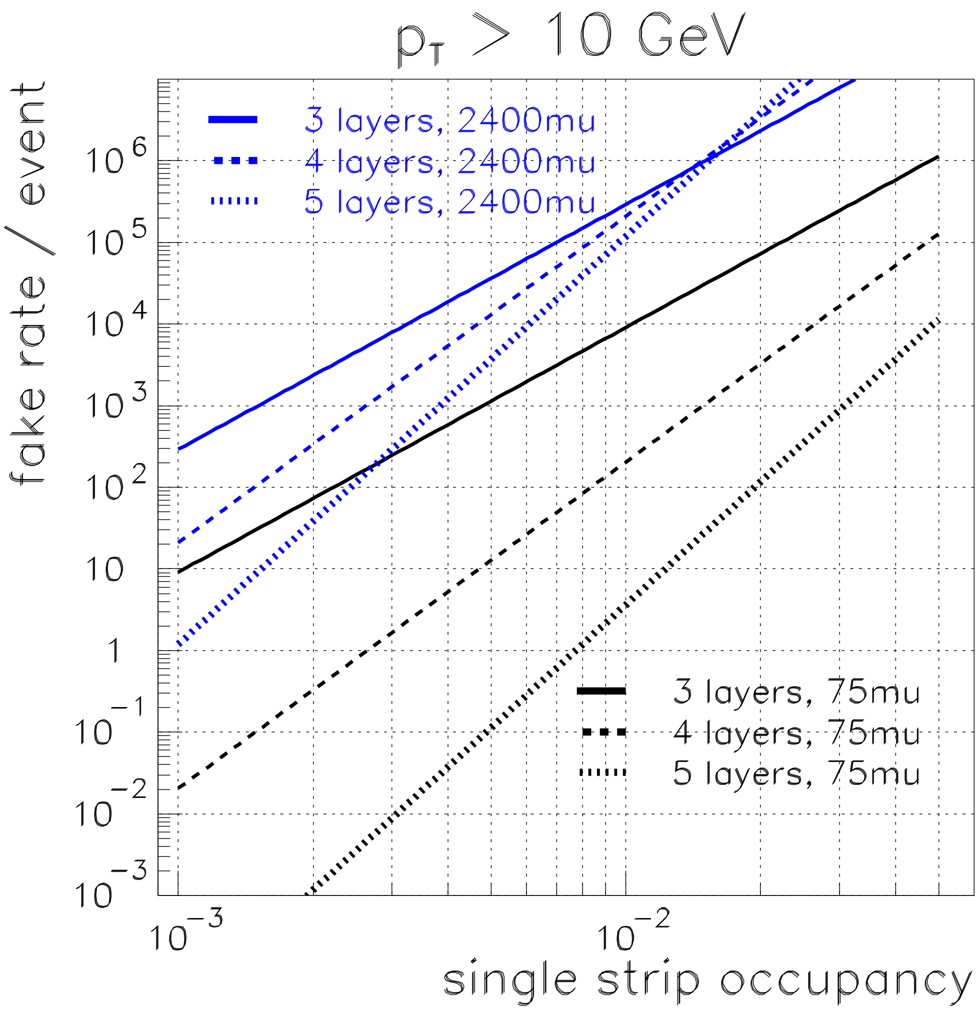

Figure 3: Graph showing the relation between occupancy and number of fake tracks found by pattern matching of randomly generated hits. Patterns are matched to 3, 4 and 5 layers and with two different hit pitches.

doublet layer is therefore crucial for the trigger to work. Coincidences between the two planes in the doublet module select only hits from high momentum tracks that are transferred to the trigger processors. Increasing the separation between the two silicon planes increases the momentum threshold which lowers the occupancy but the counter effect is that the ambiguities increase. Thus a sufficient momentum threshold and occupancy reduction may not be achieved with a single doublet layer only.

The data transfer rate and bandwidth will most probably be the bottle neck for the self seeded trigger. The maximum data transfer rate from a single detector module in the present detector is limited to 180 Mbit/s. The plan is that this will double at SLHC but in order not to risk loss

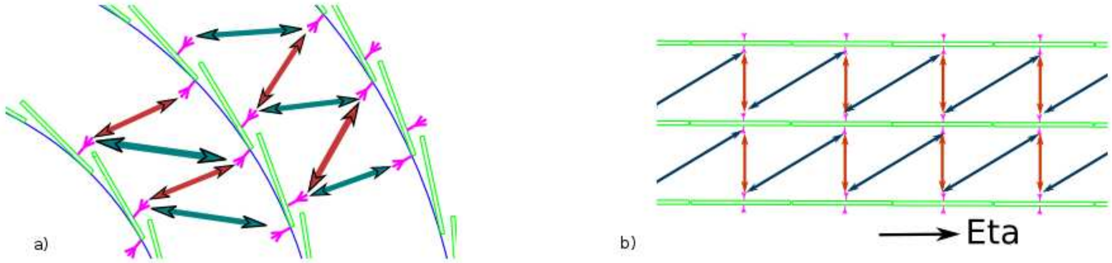

Figure 4: Multimodule data transfer in $r-\Phi$ (a) and $r-z$ (b).

of trigger efficiency an even higher data transfer rate is desirable. Wireless data transfer of data has never been tried in high energy physics experiments because the data transfer speed of this technology has in the past been too low and the components have been relatively big and power hungry for integration in trackers. The emerging technology for future wireless applications using the unlicensed 60 GHz band has several attractive features for use in trackers. The size of the mm-wave components are compatible with the size of other components in the tracker and the technology offers multi-gigabit data transfer rate at low power over short distances. A feasibility study of the usage of 60 GHz technology in the ATLAS tracker has been started [8]. The technology can not only provide a high data transfer rate without adding services. It can also be used to make a topological trigger in the tracker by making coincidences between several doublet layers and to increase momentum discrimination thresholds. Fig. 4 shows that in-detector intelligence would require a large number of short range wireless links between groups of detector modules.

4. Conclusions and outlook

A hardware track trigger contributing to the LVL1 trigger has the potential to increase the selectivity thus the quality of the trigger which would allow the ATLAS detector to take full profit from the luminosity upgrade of the LHC. The readout and processing of the data in time for the LVL1 decision is challenging but there are two complementary concepts for a track trigger implementation under study. The self-seeded track trigger concept can be instrumented in the present tracker design with some modifications in the layout. The impact of these modifications on the off-line performance must be studied in detail. Development of techniques and technology areas of data reduction on-detector, fast tracking and pattern recognition off-detector and fast data transfer will be required for the concept to work.

5. Acknowledgements

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