Timing behavior of the ATLAS Pixel Detector in calibration, cosmic-ray and collision data

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The ATLAS Pixel Detector is the innermost tracking detector of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. It consists of 1744 identical modules built using a hybrid silicon pixel detector technology with in total 80 million readout channels. As with all LHC detectors the Pixel Detector is designed to distinguish signal hits from two subsequent bunch crossings with the time interval of 25 ns (or 1 BC) at the full LHC luminosity. Due to the timewalk effect in the front-end electronics and propagation delays in the readout circuitry each detector module requires an individual timing adjustment with a precision of about 1 ns. Such precision, which is far below the detector's intrinsic timing resolution of 25 ns, has been achieved by taking the collision data with known timing offsets and analyzing timing distributions of hits from particle tracks. In the paper the measured timing characteristics of the modules are analyzed and the timing optimization process is described.

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1. Introduction

The ATLAS Pixel Detector [1, 2] is a silicon tracker that has been designed to provide precise and efficient track and vertex reconstruction close to the collision point. One of the major challenges in the design of the detector is the fast hit identification - to observe rare physics events proton-proton collisions are expected every 25 ns at the full LHC design luminosity of 10^{34} cm^{-2}s^{-1}. In the time interval between the collision events the detector must register the hits and assign them to the correct bunch crossing. Failing to do so will either result in tracking inefficiency (if all hits from a traversing particle are lost) or will affect the tracking precision (partial loss of hits). Therefore a precise timing adjustment of the detector based on the knowledge of its timing behavior is crucial.

The detector design allows a separate clock phase adjustment and timing measurement for each of the 1744 modules. In order to study the timing behavior each module has a dedicated circuitry, which allows fine-tunable delay settings of the test charge injection strobe with respect to the module clock. For optimization of the data taking with collisions the module clock is delayed in 0.3 ns steps with respect to the bunch crossing time. The per-module adjustment relies on the assumption that the pixel-to-pixel timing differences throughout the module are small, which indeed have been proven to be less than 2 ns in the system design test [2]. While the study of the timing behavior has been performed already at the module production stage, the clock phase adjustment requires hits from triggered physics data, taken in the experimental cavern. As will be shown in this paper, the clock phase optimization has been conducted by shifting the clock phase in fine steps and studying the timing distribution of hits from particle tracks under consideration of hit's charge deposition. This way the required precision of less than 1 ns has been achieved.

2. The ATLAS Pixel Detector

2.1 Detector Layout

The Pixel Detector surrounds the interaction region and provides three space-points for tracking in the pseudorapidity range $|\eta| < 2.5$. Its 1744 identical modules are arranged into three cylindrical barrel layers around the beam axis at radii 5, 9 and 12 cm and two endcaps, each consisting of three disks, positioned at distances 50, 58 and 65 cm from the interaction point. Each module consists of a 250 μm thick n^+-on-n silicon pixel sensor with an area of 6.1 $\times$ 1.6 cm^2, read out by 16 front end (FE) chips with in total 46080 channels. To meet the required transverse impact parameter resolution of 15 μm, the pixels have a nominal size of 50 μm $\times$ 400 μm. Each module has a Module Controller Chip (MCC), which handles the digital readout of the 16 FE chips.

2.2 Data Sampling

In operating conditions the detector is permanently ready for data sampling. If a charged particle traverses a pixel cell of the sensor the deposited charge is collected in the corresponding FE pixel cell on the feedback capacitor of the preamplifier, which is discharged continuously by a constant current. Once the output voltage of the preamplifier crosses an adjustable threshold the discriminator fires. The discriminator output goes back to logical low state when the preamplifier signal drops below the threshold. Both edges of the discriminator pulse are detected and each is
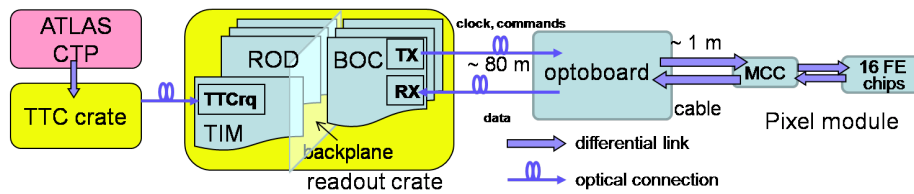
Figure 1: Block diagram of the Pixel Detector readout system

assigned a timestamp provided by the module clock. The difference between the two timestamps is called Time-over-Threshold (ToT) and is a measure of the deposited charge. The timestamp of the discriminator leading edge, the ToT and the cell address information are stored in one of the 9 End-of-Column (EOC) buffers in the FE chip. The data can be kept there for up to 255 BC, specified by the FE latency setting, waiting for a trigger decision.

2.3 Readout System

The block diagram of the readout architecture of the Pixel Detector is shown in Fig. 1. The LHC provides a 40 MHz clock signal, which is distributed together with the synchronization and trigger commands throughout the ATLAS data acquisition system by the Central Trigger Processor (CTP) [3]. The Timing Trigger and Control (TTC) crate, which serves as a CTP interface on the Pixel Detector side, fans out the clock and the commands to 9 pixel readout crates. A TTC Interface Module (TIM) receives the signals and optionally delays them before passing them through the backplane to the Readout Driver (ROD) and the Back of Crate (BOC) cards housed in the same crate. In the TIM the clock signal can be delayed up to 24.9 ns in 0.1 ns steps (in the TTCrq plugin) and the commands for up to 255 BC in 1 BC steps. The ROD encodes the commands and sends them to the BOC where the clock and commands are BiPhase-Mark-(BPM)-encoded before transmission via a $\sim$ 80 m long optical fiber to the on-detector optoboard [8]. There the clock is recovered and sent electrically to the module where it drives the timestamp circuitry. The BPM encoding circuit in the BOC (in the TX plugin) allows to delay the BPM signal up to 40 ns in steps of 0.3 ns, which is ultimately used for the per-module clock phase adjustment.

Based on the information received from the ATLAS trigger detectors the CTP decides if a particular event is interesting and issues a level-one-accept trigger (LVL1A) for the readout. The signal is sent all the way down to the MCC where it can be repeated up to 15 times allowing an up to 400 ns long readout window. Passed to the FE chips the trigger is assigned a timestamp and issues a readout request of all stored hits with the timestamp matching the trigger timestamp offset by the FE latency setting. The requested hits arrive at the MCC, which assembles the event and sends it to the optoboard, which in turn transfers it via the optical link to the BOC. After decoding the data are sent to the ROD for further processing. To maintain error-free signal sampling the phase of the sampling clock in the BOC (in the RX plugin) requires an adjustment. Normally the whole clock cycle is scanned and the operating point is set to far from the error band, which indicates the interval of the delay settings where the input signal and the sampling clock are in phase. Repeated measurements of the position of the error band within the sampling clock cycle allow to determine the stability of the timing settings.

2.4 Timewalk Effect and Pixel Types

The timewalk effect is the dependence of the time of the discriminator threshold crossing on the pulse height of the preamplifier output signal, i. e. the registration time of a hit depends on the deposited charge. It is largely determined by the signal rise time, which is subject to very strict constraints on the power consumption budget and topological size of the FE electronics. For a pixel cell the rise time of the preamplifier signal is ≈ 15 ns [2]. The fall time is determined by the feedback current adjusted by the ToT tuning, with a typical tuning of 30 BC for a 20 ke input charge signal. With these parameters the output pulse of the preamplifier acquires a shape shown in Fig. 2 for two different charge depositions, 4.5 ke and 10 ke, each of which crosses the typical threshold of 4 ke at different times. As shown the timewalk in the case of 4.5 ke injected charge exceeds the time interval between crossing bunches. This may be reduced by lowering the threshold at the cost of a higher noise occupancy. However, also in this case there will be a limited range of small charge depositions registered in the subsequent bunch crossing interval.
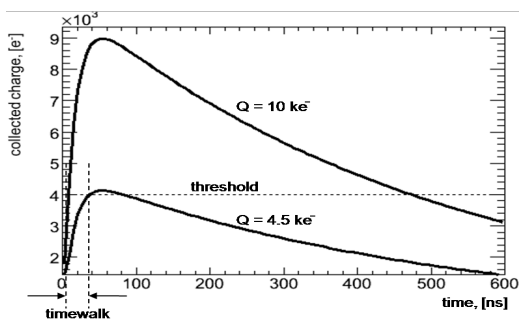

Figure 2: Shape of the preamplifier output pulse for two injected charges, 4.5 ke and 10 ke.
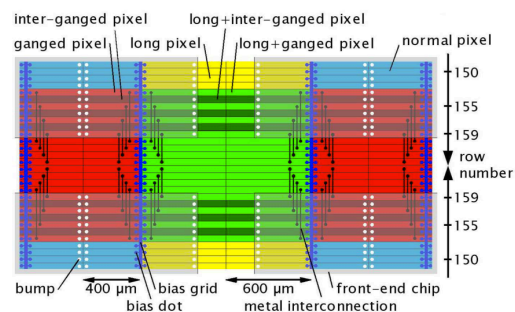

Figure 3: Variety of pixel types in the gap between FE chips, from [5].

To recover these hits in one bunch-crossing readout mode a so-called hardware timewalk correction is implemented. It duplicates registered hits with the ToT below a programmable threshold *ThrDub* by storing them twice, once with the registered hit time and once with the hit time decremented by one bunch crossing. This will result in an increase of the data volume delivered to the off-detector readout electronics, which is measured to be a 10% effect for the typical ThrDub setting of 5 BC during the test beam [6]. Another feature allows the rejection of a hit if its ToT is below a second threshold *ThrMin*.

To prevent inefficiencies in the gap between FE chips, a set of special pixel types, different from the nominal ones, have been introduced in this area, as shown in Fig. 3. Pixels of one special type, called *long*, are extended by 200 μm in the longitudinal direction parallel to the beam. Other pixels, called *ganged*, are connected on the sensor in pair in a special way and share a common readout channel. Pixels between ganged pixels, called *inter-ganged*, have the nominal dimensions, but see a larger input capacitance due to the sensor interconnects. There is also a small number of combinations of these pixel types, which are normally assigned to the larger category according to their performance. Since a higher input capacitance degrades the timing performance, this has been compensated for ganged and inter-ganged pixels in the FE design by increasing the size and the bias current of the input transistor of the preamplifier. Additionally, one long pixel per FE chip on the edge of the module, called *test* pixel, can be used for monitoring the output signals of its FE

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circuit. Due to the additional load capacitances, the timing performance of this pixel is significantly degraded.

3. Timing Calibration Scans

Prior to the operation with LHC beams several calibration scans have been developed to study the timing behavior of the front-end electronics. Their results provide input for the simulation of the timing response of the detector and can be used to monitor changes in the detector performance expected with irradiation. Since a test charge can be injected in each FE pixel cell individually, the timing performance is measured per pixel. The timing calibration scans utilize the capability of the MCC to delay the charge injection strobe with respect to the module clock in fine adjustable steps. This circuitry itself requires periodical calibration.

3.1 T0 Tuning

For performing some of the detector calibration scans the exact conditions as in detector operation with beams need to be reproduced. In particular the measurement of the in-time threshold and the calibration of the ToT response as a function of input charge require a simulation of the optimal adjustment between the module clock phase and the bunch crossing time. This simulation is achieved by the T0 tuning, which exploits a delay line in the MCC to set the timing of the charge injection. The appropriate delay setting for each module is determined such that an injected reference charge of 100 ke is detected 5 ns after the corresponding clock transition. This 5 ns margin takes the maximal possible timing uncertainties into account, still permitting a 20 ns window for detecting signals of lower amplitude in the same clock cycle. This approach is similar to the one used for timing optimization with collision data.

The delay setting calculation is based on the module average of the clock transition times measured per pixel. The actual T0 position (or margin) for individual pixels has a certain dispersion shown in Fig. 4 for all measured pixels grouped by their type. As shown, nearly all pixels except for test pixels fit into a 4 ns window which is considered as a good approximation of all pixel-to-pixel timing variations.
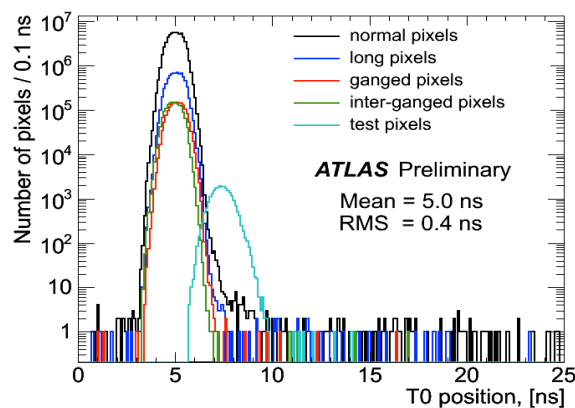

Figure 4: Calculated T0 position within a clock cycle after T0 tuning for a 100 ke charge injection for all measured pixels grouped by their pixel type.

3.2 In-time Threshold Scan

The in-time threshold is defined as the minimal charge that can be assigned to the correct bunch crossing provided that the clock phase is optimized with respect to the bunch crossing time. If the T0 tuning has been performed, the in-time threshold is equivalent to the charge with the timewalk of 20 ns with respect to the reference charge of 100 ke. To measure the in-time threshold, a scan of the respective charge range is performed, by repeating the injections and measuring the probability of the hit detection in the target bunch crossing. The charge value with a 50% hit detection probability is defined as an in-time threshold.

The in-time threshold measured this way for the full detector at a discriminator threshold of 4000 e is shown in Fig. 5(a), grouped by pixel types. The plot demonstrates that the in-time threshold is on average 1400 e larger than the discriminator threshold. This is a considerable difference since the signals above the discriminator threshold and below the in-time threshold, even if they are detected, may not be read out. Compared to the normal pixels the in-time threshold value is slightly different for the special pixels in the gap between FE chips. The higher sensor capacitance seen by preamplifiers justifies the larger in-time threshold for the long pixels. This effect has been compensated for the ganged and inter-ganged pixels, therefore they have the same or even a lower in-time threshold. The small hump on the distribution of long and test pixels at approximately 4600 e and 5800 e, respectively, has been traced back to pixels disconnected from the sensor.
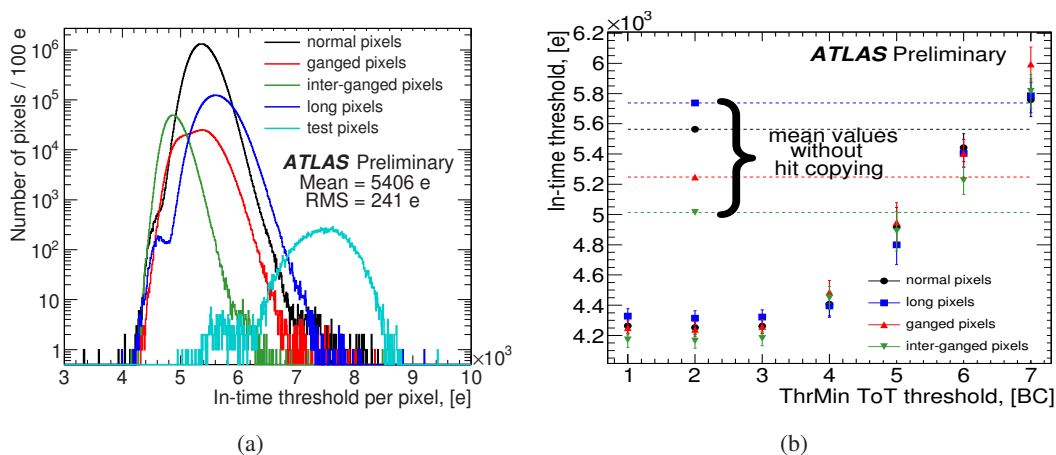

Figure 5: (a) In-time threshold for all scanned pixels in the detector, grouped by pixel types. (b) Reduction of the in-time threshold using the hardware timewalk correction mechanism. The plot shows the average in-time threshold per pixel type for one example pixel module as a function of the ThrMin setting with a hit duplication threshold ThrDub set to 12 BC.

The in-time threshold measured using the timewalk correction mechanism is shown in Fig. 5(b) for one example pixel module grouped by pixel types. For this measurement the duplication of all potentially late hits was activated by setting ThrDub threshold to 12 BC. The threshold ThrMin, which determines the minimal ToT required for a hit to be stored, has been varied. Using this explicit rejection of small ToT hits the in-time threshold is reduced to only about 300 e above the discriminator threshold. Furthermore, the measurement at 6 BC ThrMin is close to the standard in-

time threshold measurement, which suggests the usage of this threshold setting for hit duplication. Another interesting observation is that the rejection of hits with a ToT below 3 BC has no effect on the in-time threshold, which is assumed to be driven by the slow turn-off of the discriminator.

3.3 Timewalk Profile

To determine the delay in crossing a given discriminator threshold Q_{thr} as a function of injected charge q a dedicated scan has been performed. For each charge the MCC delay required to detect 50 % of hits in the target readout window was measured. This delay was subtracted from the delay measurement with the reference charge of 100 ke. The result of such a scan averaged over normal pixels from one example FE chip is shown in Fig. 6(a). The data points were fit with the function derived from the expected functional form of the preamplifier response:

$$\text{hit detection time} = p_0 - p_1 \cdot ln(1 - \frac{Q_{thr}}{q}) \tag{3.1}$$

where the parameter p_0 determines the timewalk value of the asymptotically high input charge relative to the measurement with the reference charge and the parameter p_1 is the rise time of the preamplifier. This fit was performed for all measured pixels averaged by pixel type per FE chip and the residuals with respect to the measured data are shown as a function of input charge in Fig. 6(b). Apart from small systematic deviations a good description of data by the parameterization is observed. Furthermore, one notices that the distribution of residuals broadens to more than 1 BC peak-to-peak close to the discriminator threshold. Since a direct timewalk profile measurement on the whole detector is a very time consuming operation, both the p_0 and p_1 parameters are determined from the in-time threshold measurement, which is currently taking about half an hour for the whole detector.

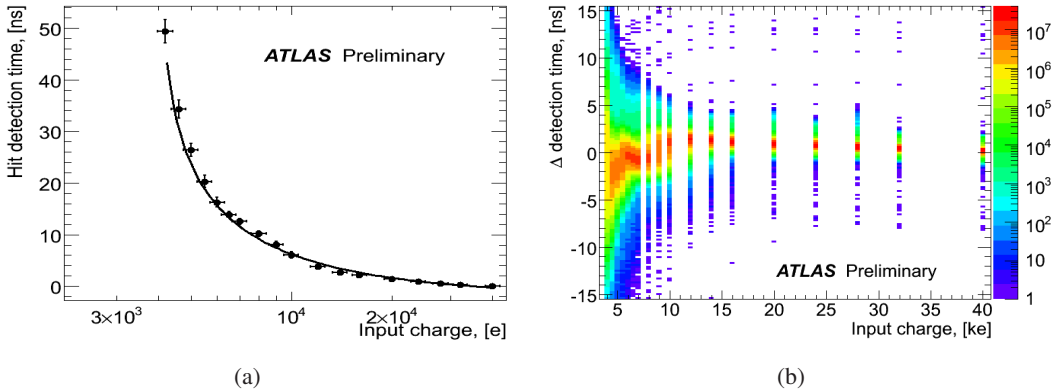(a)   (b)

Figure 6: (a) Hit detection time averaged over normal pixels from one example FE chip with respect to the time of detection of the reference charge of 100 ke, as a function of the input charge. Data points are overlaid with the fit curve defined by Eq. 3.1. (b) The residuals between per-pixeltype per-FE chip parameterizations and the measured points for each pixel.

4. Initial Timing Adjustments Using Cosmic-Ray Data

In 2008 after the integration of the Pixel Detector into the ATLAS readout, the trigger latency in the pixel off-detector electronics was adjusted using cosmic-ray tracks. To study the LVL1A trigger timing and the pixel module timing an 8 BC long readout window had been used. Individual module clock phases were aligned by compensating the estimated total clock propagation delays from the off-detector electronics to the corresponding module. After this adjustment the majority of hits from muon tracks were found within 2 BC as shown in Fig. 7(a). The width of the distribution is the convolution of three effects: a random traversing time of muons in the clock cycle, the timewalk effect and the timing alignment of the modules with respect to each other. To estimate the third effect the corrections for the other two have been made. By requiring clusters with a charge deposition greater than 15 ke the timewalk impact was minimized. The time of the passage of a muon was measured using an external timing reference, the Transition Radiation Tracker (TRT) detector timing information T_{TRT} (Δt = 3.1 ns) [7]. A histogram of the averages of individual module timing values after the correction for T_{TRT} is shown in Fig. 7(b). As shown, the modules are aligned within 1 BC peak-to-peak with an r.m.s. of 5 ns.
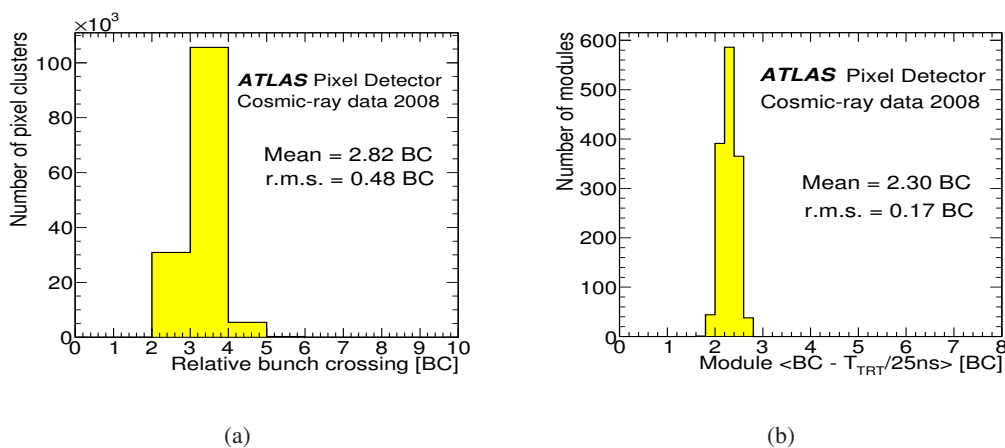

(a) (b)

Figure 7: (a) Timing distribution of individual pixel clusters on track. (b) Per-module detection time of clusters with > 15 ke charge deposition corrected to the time of passage of a muon T_{TRT} [7].

5. Timing Adjustments Using Collision Data

The first proton-proton collision data with a center of mass energy of $\sqrt{s}$ = 900 GeV have been taken in November 2009. To allow for timing studies the readout window was set to 5 BC. In order to investigate maximal possible energy depositions the FE latency setting was set to 255 BC. Hits from collision events were positioned in the middle of the readout window to read out at least one BC before any expected physics data, in order to study the noise level. The example ToT versus relative BC histograms for all accumulated hits shown in Fig. 8 were provided directly by the online monitoring for each module. The timewalk pattern is clearly seen, i.e. the hits with high ToT are detected earlier. For some of the modules, similar to the one shown in Fig. 8(a), the high

ToT values were distributed over two bunch crossings, whereas the majority of the modules were collecting high ToT hits in one BC, as shown in Fig. 8(b). Clearly, in the first case the clock phase is not optimized for squeezing the readout window and requires an adjustment. The calculation of the timing corrections from the minimal ToT registered in the target BC with the help of the calibration data was found to be not precise enough. However, accompanied by inspection of the monitoring histograms by eye, it has been used for the gross timing adjustment of the modules.
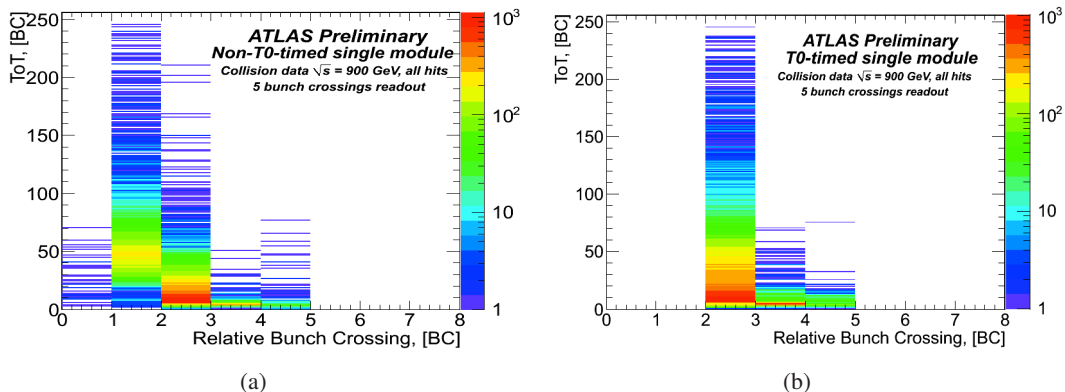

(a)   (b)

Figure 8: Example timing distribution of all hits according to their ToT recorded within 5 BC readout window for two different modules with (a) non-optimized timing and (b) optimized timing.

To further optimize the module timing special runs have been taken after the restart of the LHC in April 2010. For these runs the clock has been delayed in 1 ns steps for all modules in parallel until the high ToT hits in all modules made a transition into the previous relative bunch crossing. The effect is seen in the timing distribution of hits from reconstructed particle tracks shown in Fig. 9 for different delay settings for a particular module. The maximal delay prior to the
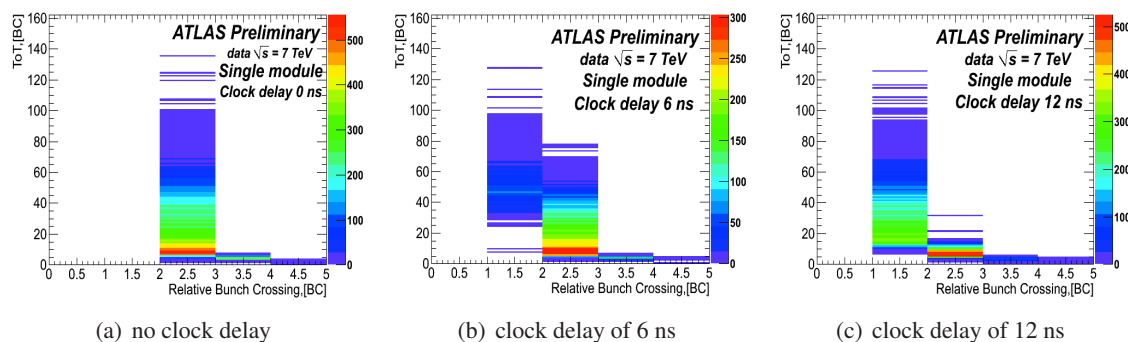

(a) no clock delay   (b) clock delay of 6 ns   (c) clock delay of 12 ns

Figure 9: Timing distribution of hits on particle tracks by their amplitude for different clock delay settings.

transition, referred to as T0 position, has been measured per module and plotted as a histogram in Fig 10(a). Using these delay values the individual module clock phases were optimized. To verify the adjustment an another special run with the clock delays adjusted from -0.5 ns to + 4.5 ns in 0.5 ns steps has been performed and the maximal delays were measured once again, see Fig 10(b). Comparing the r.m.s. values of both distributions a significant improvement in the alignment of

T0 positions of modules with respect to the previous measurement is observed. The absolute T0 position however was found to be too close to the transition region, which is partially explained by a shift of the clock received by ATLAS from the LHC. The results were used for the second iteration of the module clock optimization. Note that due to the large readout window of 5 BC there were no hit efficiency losses incurred by these special runs.

The timing distribution of clusters on tracks in the whole detector measured after the adjustment is shown in Fig 11. As shown, the vast majority of clusters is registered within two bunch crossings, which gave us enough confidence to squeeze the readout window gradually down to 2 BC. By analyzing the timing distribution of hits according to their ToT values the maximal ToT of hits in the bunch crossing following the peak was calculated. This value, typically 6-7 BC, is used as a threshold for the ToT duplication once the readout window is reduced to 1 BC. At that stage the stability of the per-module timing settings becomes essential. After the final adjustments it was verified by measuring the phase of the data returned from the detector with respect to the off-detector electronics clock. The maximal difference between the measurements for each module repeated over about 3 weeks of operation is shown in Fig 12. The cause for large delay differences of 3 ns and partially also 2 ns was tracked down to a failure of the hardware, which has been replaced. The remaining differences of up to 2 ns, expected from the stability studies of the optical link tuning [8], can be tolerated within the safety margin of 5 ns without hit efficiency losses.
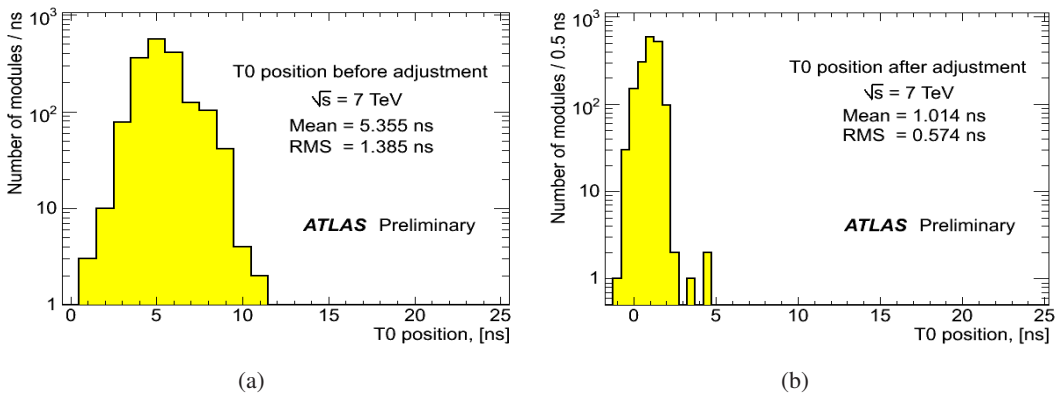

Figure 10: Maximal applicable clock delay per module prior to the transition of high ToT hits into the previous bunch crossing for (a) the initial measurement (b) the measurement after optimization.

6. Summary

In preparation for 1 BC readout operation the clock phases of the individual ATLAS Pixel Detector modules have been adjusted to optimize for the assignment of hits from charged particle tracks to a single bunch crossing. Initially, the adjustment was based on the calculation of clock propagation delays and verified with cosmic-ray data. Then, the adjustment was refined using a set of collision data taken with known clock delays in the readout. By analyzing timing distributions of hits from particle tracks and requiring a 100% efficiency for the hits with high charge depositions in the target bunch crossing an optimization has been performed resulting in a precision of less
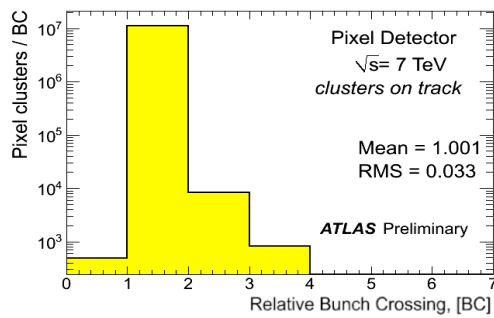
Figure 11: Timing distribution of clusters on tracks after optimization.
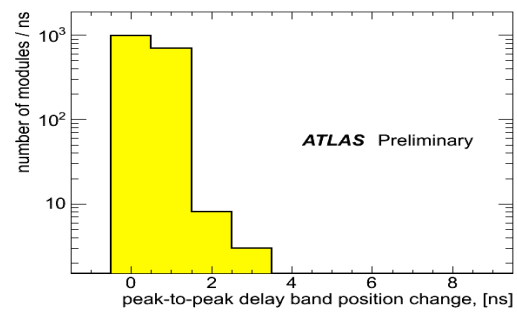

Figure 12: Maximal timing variation per module.

than 1 ns. The stability of the adjustment settings was measured to be well within the safety margin of 5 ns. In addition a timing calibration procedure has been established for monitoring the timing characteristics of the detector in-situ.

Acknowledgment

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