

Atlas Tracker Upgrade: Silicon Strip Detectors and Modules for the sLHC

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It is foreseen to increase the luminosity of the Large Hadron Collider (LHC) at CERN by a significant factor, with the upgraded machine dubbed Super-LHC (sLHC). The ATLAS experiment will require a new tracker for sLHC operation. In order to cope with the increase in pile-up backgrounds at the higher luminosity, an all silicon detector is being designed. The new strip detector will use significantly shorter strips than the current SCT in order to minimise the occupancy. As the increased luminosity will imply a corresponding increase in radiation dose, a new generation of extremely radiation hard silicon detectors is required. Extensive R&D programmes are underway to develop silicon sensors with sufficient radiation hardness. In parallel, new front-end electronics and readout systems are being designed to cope with the higher data rates. The challenges of powering and cooling a very large strip detector will be discussed. Ideas on possible schemes for the layout and support mechanics will be shown.

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Introduction

After the LHC reaches its design luminosity $\mathcal{I}_{max} = 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [1], LHC upgrades in two phases bringing a significant increase in luminosity. This will allow the extension and continuation of the physics program [2]. After the Phase-I upgrade (2016) the luminosity will double to 2 x $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In the second phase, called Super-LHC (sLHC) starting around 2020, the goal of the ATLAS experiment is to collect data from an integrated luminosity of 3000 fb⁻¹. Coping with the increase in pile-up events and in radiation dose will require many changes in the ATLAS detector. This is of particular importance for the ATLAS Inner Tracking System (ID) which is located close to the interaction region. Below, the recent research and development (R&D) work concerning the ID are described.

P-type silicon sensor development

The most significant upgrade for ATLAS is the replacement of the whole ID, foreseen at the phase-II, in an all-silicon inner tracker. Simulation studies are in progress to define the layout [3]. It will use significantly shorter strips than the current Semiconductor Tracker (SCT) in order to minimize the occupancy. The layout of the new design in the barrel region has four pixel layers, three layers with short strips (2.4 cm) and two layers with long strips (9.7 cm). In the forward region, it has five strip discs per end-cap. A new generation of extremely radiation hard silicon detectors is required to remain operational under the severe conditions of the sLHC. An option being studied is the n-in-p sensor technology. These sensors are more radiation hard than the current p-in-n technology and also do not require full depletion which may not be achieved after high radiation doses. Performance of these sensors is described in Ref. [4].

Stave program

For the short strip region, the baseline for the module geometry is the singlesided module. It has two flex hybrids attached to the sensitive face of the silicon wafer, each hybrid carrying two rows of 10 ABCN CMOS ASICs [5]. The resulting four rows of 1280 channels are wire-bonded to the corresponding four rows of capacitively coupled polysilicon biased 2.4 cm length strips. These modules are then attached to either side of a lightweight carbon-fiber facing with an embedded cooling. It is the socalled stave concept. Before tests with modules, eight hybrids were delivered to Liverpool University and individually equipped with untested ABCN chips. Fully functional hybrids were produced and showed channel yield of >99%. Both hybrids and ASICs are therefore working extremely well. An average noise per channel of ~400 electrons was measured and a gain of 110 mV/fC [6]. More of the hybrids are in the process of being used to make modules.

An alternative approach to that of the stave is a double-sided silicon strip module [7] led by Geneva University and KEK. As a minimal modular unit, it will be assembled into larger structures. A local support structure for 12 modules is being developed. As a part of their R&D program a module prototype was irradiated at the CERN-PS

Irradiation facilities at an estimated fluence of ~5 x 10^{14} 1-MeV-n_{eq}·cm⁻². The module consisted of one fully qualified sensor, one mechanical grade sensor, two fully populated hybrids on one side and two carbon-fiber bridges on the other side [8]. With the sensor biased at -100V and the chips powered, the module survived the irradiation. The sensor current increased by 5-6 orders of magnitude to I_{si} = 2.3mA with a T_{hyb} = 5°C. All chips responded and the noise and noise occupancy are comparable with the noise characteristics of a similar but non-irradiated module.

Petal Program

The petal concept is the baseline for the end-cap region [9]. It is also based on single-sided modules sandwiched around a central structure with embedded cooling. But in this case, six sensor types will be necessary to equip the forward petals at the varius radii (adding one level of complexity compared to the barrel region where all sensors are the same). Another item to consider is the bonding angle, which due to the varying pitch in a sensor will be larger than on the barrel. Studies about the petal configuration are underway. Mechanical prototypes are being measured in LBL and Nikhef. The construction of the first forward prototypes modules is expected to start at the end of 2010.

Thermal simulations of forward modules are being carried out at IFIC-Valencia. The expected sensor power comsuption at 0°C under operation is nearly 1 mW/mm² being allowed for twice this to give a safety margin. According to simulations, the design has a good thermal behaviour with respect to thermal runaway and the sensors are calculated to operate at a maximum temperature of $\sim -20^{\circ}$ C [10]. Also at IFIC, end-cap simulations are being developed to establish the most suitable bus cable on the petal to deliver the power and TTC/Data [11] and related to the services routing and discs support schemes on the complete end-cap layout [12].

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