

The Digital Data Processing Unit for the HTRS on board IXO

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The Institute for Astronomy and Astrophysics in Tübingen participates in the development of two of IXOs instruments, the Wide Field Imager (WFI) and the High Time Resolution Spectrometer (HTRS). The soft- and hardware for the HTRS Data Processing Unit (DPU) is being developed and will be tested in Tübingen. We give a brief overview of the HTRS and the DPU with its main components and tasks. In particular we present simulation results of the DPU operations that show the ability to fulfill the data rate requirements. The two main solutions to this difficulty and thus the primary tasks of the DPU are then presented in more detail.

Fast X-ray timing and spectroscopy at extreme count rates

February 7-11, 2011

Champéry, Switzerland

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1. Introduction

IXO is an L-class astrophysics mission that has been conceived to study the X-ray universe, all the way from the earliest galaxies to our immediate cosmic environment to observe matter under extreme conditions. IXO aims to provide direct insight into some of the most important themes posed by ESA's Cosmic Vision 2015-2025 science objectives¹.

To enable these measurements, IXO will deliver a 100-fold increase in effective area for high-resolution spectroscopy, microsecond spectroscopic timing, and high count rate capability over a broad energy range.

2. The HTRS instrument and detector

The IXO science case calls for the capability to observe the strongest X-ray sources with count rates up to one million counts per second. This requires the HTRS ability to provide a good spectral resolution (about 150 eV at 6 keV) simultaneously with sub-millisecond timing, low deadtime and low pile-up (< 1 % at 1 crab).

In order to meet these performance requirements, the HTRS is based on a monolithic array of 31 silicon drift detectors (SDDs) in a circular envelope (as shown in Fig. 1) and a sensitive volume totaling $4.5\text{ cm}^2 \times 450\mu\text{m}$. The SDD principle uses fast signal charge collection on an integrated amplifier by a focusing internal electrical field. It combines a large sensitive area and a small capacitance with a fast readout, thus facilitating good energy resolution and high count rate capability.

The HTRS is a non-imaging device and will be operated out of focus, in such a way that the focal beam from the mirrors is spread almost uniformly over the 31 SDDs to reduce deadtime and pile-up and therefore increase the overall count rate capability of the instrument.

Overview of the key capabilities of the HTRS

- high precision timing measurements up to 1 million counts per second
- operating bandwidth in the range of 0.3 keV – 15 keV
- spectral resolution of 150 eV FWHM @ 6 keV
- event losses due to pile-up and deadtime < 1 % @ 1 crab

While the HTRS instrument is being studied by an international consortium led by the French Space Agency and the Centre d'Etude Spatiale des Rayonnements (Toulouse), the detector chip itself was developed by the Halbleiterlabor of the Max-Planck-Institute (MPI) in Neuperlach.

The 31 silicon drift detectors are capable of performing an event-triggered readout completely independent for each cell in parallel, thus allowing for very high count rates up to 1 million counts per second. Event separation in one cell is possible up to 200 ns. Only after a number of events have been detected (Fig. 2), the anode (part of each cell) is cleared thus minimizing the deadtime.

¹Cosmic Vision: Space Science for Europe 2015-2025, ESA BR-247

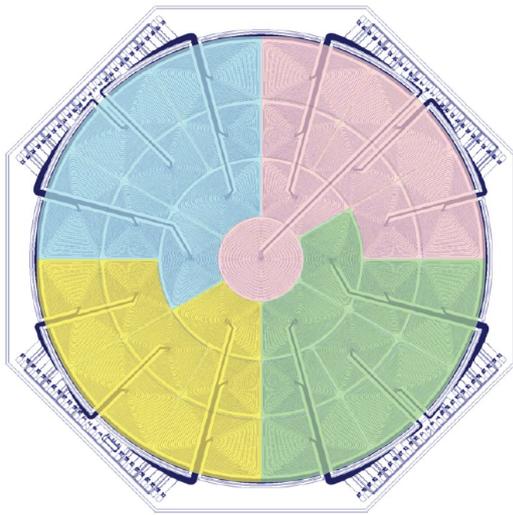


Figure 1: Layout of the HTRS detector chip.
(Peter Lechner, HLL)

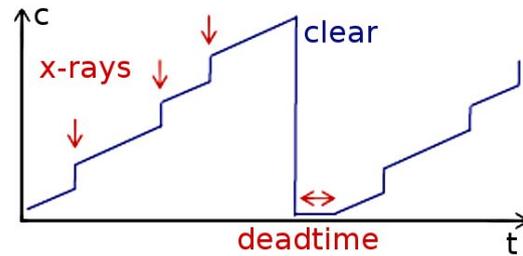


Figure 2: Anode charge in one cell over time. Note the constant increase due to dark currents. The arrows mark charge increases caused by X-ray photons. At a certain threshold the anode is cleared and inoperable for a short time.

3. The Data Processing Unit

Reducing the data rate to a value given by the available telemetry rate (0.75 Mbit/s) is achieved in two steps. First (described below) the data handling FPGA will implement several highly configurable detector operation modi to reduce the amount of data while enabling the observer to optimize the scientific output of the observation. The second step is lossless on-board data compression and intelligent wrapping of the data done by a Leon3 CPU additionally implemented in the FPGA. Both units form the DPU of the HTRS instrument which is being developed in a two-part design as is shown in Fig. 3.

A fast and specialized FPGA (e.g. Virtex 4) will receive events from all 31 cells in parallel and generate the required observation mode products. These include a single-event-mode where each individual event is time-tagged and transmitted to earth as well as several highly configurable spectrum-modes where a spectrum with given energy resolution is integrated onboard the DPU over a given time.

While the raw data rate (event energy information + time of detection) can already be reduced by applying spectrum-modes, further reduction is required (Fig. 5). Therefore, a Leon3 VHDL microprocessor model integrated into the same FPGA will reduce the data by applying a lossless bzip2 compression algorithm. The Leon3 is also used to configure and operate the instrument and to wrap the data and hand it to the main satellite bus via SpaceWire.

Leon3 is a VHDL model of a 32-bit microprocessor with SPARC V8 architecture developed by Aeroflex Gaisler for the European Space Agency. We develop the DPUs operating system using RTEMS², a real-time executive that has a POSIX³ API⁴ which is required to build the bzip2 (compression) library.

²Real-Time Executive for Multiprocessor Systems

³Portable Operating System Interface for Unix

⁴Application Programming Interface

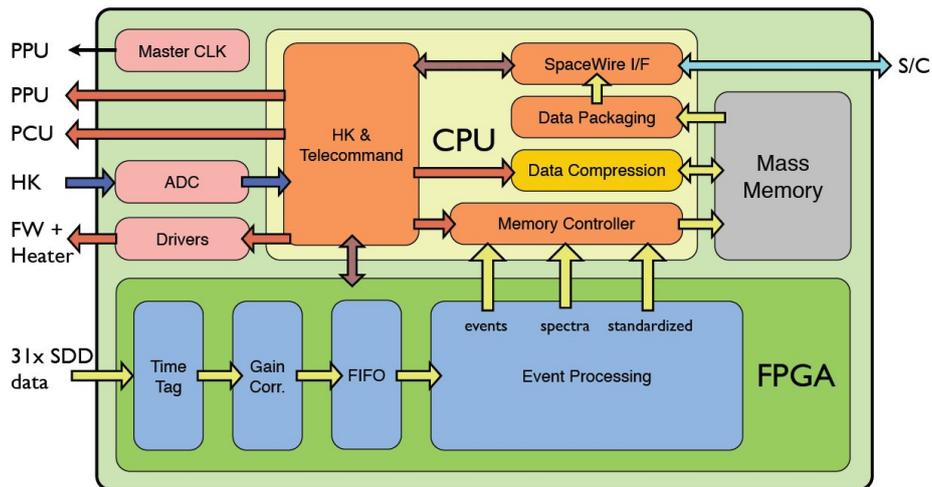


Figure 3: The two parts of the Data Processing Unit of the HTRS.

Gaisler also provides an RTEMS implementation for the Virtex 4 and a Leon3 multiprocessor version. Since the bzip2 compression speed scales linearly with the number of processors this provides the possibility to further increase the DPUs performance if necessary.

Both parts of the DPU are being developed at our institute in Tübingen and a prototype board will be built to prove the feasibility of the proposed data handling procedures, and to identify the performance of the data compression.

4. Data Rate Reduction

A single event that is detected in one of the detector chips 31 cells basically contains energy information and an ID for the cell it was detected in. When this information is transferred from the readout electronics to the DPU a time stamp is associated with the event and together these three informations form the event package.

Size of a single event package

24 bit time information
 + 5 bit pixel id
 + 12 bit energy information

Resulting data rate

$$2 \cdot 10^6 \text{ cts/s} \cdot 41 \text{ bit} \\ = 82 \text{ Mbit/s}$$

Available net telemetry rate for the HTRS

0.75 Mbit/s

Since the resulting data rate for a source with 10x the brightness of the crab is too high by a factor of 100 data reduction is indispensable. In Figs. 5 and 6 data rates are shown for different configurations of the implemented spectrum-mode. The mode itself produces a constant data rate that is independent of the sources brightness. Applying a bzip2 block compression to the data enables the HTRS to operate within the required telemetry limit.

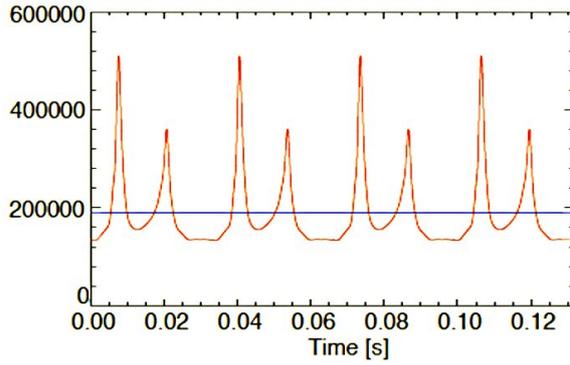


Figure 4: Light curve of the crab pulsar; avg. brightness $2 \cdot 10^5$ cts/s. (Jörn Wilms, Bamberg)

All data rate estimations are based on simulations of the detection of the crab at 10x its brightness ($2 \cdot 10^6$ cts/s) done at the IAAT in Tübingen. For the simulation of the mirror and detector properties the work of Michael Martin was used (PhD Thesis, Tübingen 2009).

channels	spectra per second					
	128	256	512	1024	2048	4096
4	0,01	0,02	0,03	0,06	0,13	0,25
8	0,02	0,03	0,06	0,13	0,25	0,50
16	0,03	0,06	0,13	0,25	0,50	1
32	0,06	0,13	0,25	0,50	1	2
64	0,13	0,25	0,50	1	2	4
128	0,25	0,50	1	2	4	8
256	0,50	1	2	4	8	16

Figure 5: Uncompressed data rates in different spectrum-mode configurations. Rates are given in Mbit/s.

channels	spectra per second					
	128	256	512	1024	2048	4096
128	0,05	0,08	0,13	0,21	0,32	0,47
256	0,08	0,13	0,20	0,31	0,46	0,64

compression factor

channels	128	256	512	1024	2048	4096
128	5,3	6,3	7,7	9,7	13	17
256	6,4	7,8	9,9	13	17	25

Figure 6: Data rates in spectrum-mode with bzip2 compression. Rates are given in Mbit/s.

5. Channel-Bit-Width in spectrum-mode

The bit-width of the channels in a spectrum is an important decision when the instrument is operated in spectrum-mode. A large bit-width prevents integer overflows in the event-counter of a spectral channel at the cost of a linearly higher data rate.

To study the effect of the bzip2 compression on the bit-width of the spectral channels, we simulated source-spectra with constant energy distribution and a completely randomized, but limited, count rate per channel. By limiting the count rate, only a given amount of bits per channel is used to store the random number of counts. The remaining, unused 'upper' bits are all zero. The compression was applied to blocks of spectra and the resulting data reduction is given in the table.

Random Bits	Unused Bits	Unused Bits	Compression Strength
32	0	0 %	0 %
28	4	13 %	3 %
24	8	25 %	14 %
20	12	38 %	35 %
16	16	50 %	49 %
12	20	63 %	62 %
8	24	75 %	75 %
4	28	88 %	87 %
1	31	97 %	96 %

The first two columns in the table give the used and unused bits (always totaling 32). Ideally the compression (4th column) is the same as the relative amount of unused bits (3rd column).

As can be seen from the table, the achieved data reduction is generally comparable to the direct cutting of the unused bits (i.e. using a smaller bit-width). The bzip2 compression thus allows the use of up to 32 bits per channel while still preserving a very efficient use of the available data rate. This large bit-width will enable the HTRS to observe highly variable sources over a wide range of intensities.

6. Conclusions and Outlook

We simulated the DPU operations (esp. spectrum generation) and concluded that the requirements on the telemetry rate can be met using the bzip2 compression algorithm. We also compared the performance of several other compression algorithms (such as gzip, zlib, lzma, paq9a) and found bzip2 well suited for several reasons such as compression strength and speed, data integrity verification, and possible parallelisation. Right now we are implementing a fully operational prototype to determine the exact performance of the compression.

We also implemented and successfully completed an exemplary test run of the compression on our Leon3 development board. An important next step here will be to experimentally operate a mass memory and to determine the resulting time constraints on DPU operations. We assume that I/O operations will have a significant impact on the compression speed.