Review of Square Kilometre Array LNA Technologies and Topologies

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Abstract. The paper concentrates on summarizing significant worldwide developments in the Low Noise Amplifier domain for the Square Kilometre Array telescope. Several technologies, design topologies and noise measurement techniques of LNAs for SKA have been proposed and analysed since the commencement of the project in 2000. Transistor technologies including GaAs mHEMT, GaAs pHEMT, SiGe HBT, CMOS, InP pHEMT have been extensively studied and characterised at multiple institutes around the world. The proposed site of SKA is either Western Australia or South Africa. Both sites experience a very significant physical temperature variation even over a 24 hour period. Hence temperature dependant studies on the DC, small signal and noise characteristics of different transistors have been carried out. Cryogenic characterisation down to 15K physical temperature of certain types of transistor technologies has also been performed. Both hybrid and MMIC LNAs based on the above technologies have been designed and measured. Depending on the antenna topology and impedance, both single ended and differential LNAs with various input impedances have been explored. Performance of LNA integrated with the antenna has been simulated and the effect of the variation of antenna impedance on the overall performance of the before mentioned components have been studied. Design, development and comprehensive analysis of measured data of both variations of LNA and their pros and cons have been portrayed in this paper. Due to system architecture requirements, differential input-single ended output LNA configuration has been designed and measured. In this paper their advantages, disadvantages and their sources will be identified. Some interesting theories and techniques of differential noise measurements have been proposed during SKA project and will also be explained as part of this paper.

1. Introduction

Engineering aspects of SKA telescope design and construction are in an important phase at present. Several innovative and robust design concepts have been proposed in SKA pathfinder projects globally. All these concepts proposed by engineering teams are being implemented in separate system architectures. LNA development and its interface with the antenna are of utmost importance and priority in SKA system engineering. In this paper most of the significant developments in LNA design and measurement have been reviewed. From fundamental principles of LNA design it is apparent that, along with achieving low noise figure, maintaining sufficiently high gain is a basic requirement. Hence noise measure and not only noise figure of devices from semiconductor foundries should be taken into account (Weinreb 2009). LNA design and development is of critical importance and very much application specific. The specifications for LNA in SKA is strict at room temperature and demands best possible response for all the key parameters like noise temperature (NT), gain, bandwidth (BW in GHz), Input and output return losses, linearity, power consumption and chip

area. Bhaumik & George (2009) has proposed two figure-of-merits which take into account all these factors of MMIC LNA design comprehensively. Higher numerical value of these FOMs signifies better performance. BW is bandwidth, NF is the noise figure, Pdiss is in mW, k equal to 25 is a constant to eliminate negative F-o-M values, D is the dimension in sq. mm and fc is the central frequency.

$$FOM_{IN} = \left[\frac{(S_{21})_{dB} - (S_{11})_{dB}}{NF \times D_{mm}^2} \right] \times \frac{BW}{f_c} \qquad (1)$$

$$FOM_{OUT} = \left[\frac{((S_{21})_{dB} - (S_{22})_{dB})(k + OP1dB)}{NF \times D_{mm}^2 \times P_{diss}} \right] \times \frac{BW}{f_c} \qquad (2)$$

2. Semiconductor Technologies studied for LNA development

The first step towards LNA design involves a detailed survey of available low noise semiconconductor processes which has the potential to cater to required specifications of a project. Though the noise budget of SKA projects a 30% noise contribution from LNA, achieving LNA noise specification of 16K (Bij de Vaate 2009) is very challenging at room temperature. Low noise foundries based on Gallium Arsenide (GaAs), Indium Phosphide (InP), Silicon and Silicon Germanium (SiGe) have

been extensively characterized by various LNA development teams in America, Australia and Europe. Technologies like pseudomorphic High Electron Mobility Transistors (pHEMT), metamorphic High Electron Mobility Transistors (mHEMT), Heterojunction Bipolar Transistors (HBT) and Complementary metal-oxide-semiconductor (CMOS) have been covered in this study. This comprehensive study has included noise and small signal modelling of 70nm GaAs mHEMT, 100nm InP pHEMT, 130nm GaAs mHEMT, 150nm GaAs mHEMT, 150nm GaAs pHEMT, 1m InP pHEMT, commercially available off-the-shelf wide gate length GaAs pHEMT, 90nm CMOS (Belostotski & Haslett 2007, 2008) and 250nm, 180nm, 170nm, 150nm, 130nm and 120nm node SiGe HBT (Bardin & Weinreb 2009; Weinreb et al. 2009).

HEMT technology has evolved into primary choice for low noise technology over past few decades. With the advent of InP pHEMTs and GaAs mHEMTs noise resistance and minimum noise figure of devices has been dramatically reduced. But they are in general expensive processes. On the contrary, there has been enormous industrial investment in radio frequency CMOS because of its inexpensive nature. With investment in CMOS, SiGe based low noise RF technologies have also experienced significant development in recent times. SKA aspires to operate in a wide range of frequency from 70MHz to 30GHz (Dewdney et al. 2009). Each of the above mentioned processes have their own advantages over others in particular sections of this vast range of frequency. HEMTs have a very high cut-off frequency (ft) and transconductance (gm) with very low minimum noise figure and parasitic resistances. But the nanoscale gate length pushes the optimum noise impedance and maximum available gain impedance far apart when plotted on a Smith chart at low frequencies. The high impedance nature of the differential antennas developed for SKA favours noise matching at low frequency but at the cost of return loss. Wideband noise and impedance matching is also comparatively difficult with GaAs and InP processes with respect to SiGe. CMOS and HBT processes are much more power effective but minimum noise figure is significantly higher than HEMTs (Bardin & Weinreb 2008). Figure 1(a) shows the normalized transconductance of six different HEMT processes against power consumption.

3. Importance of Physical Temperature Stabilisation of LNA

The proposed site of construction of SKA telescope is either Western Australia or South Africa. Australia experiences not only 50^0C variation of temperature in a calendar year but also a significant temperature swing during a single day. South Africa also experiences more than 40^0C temperature fluctuation in a calendar year. Hence a study of the variation of transconductance from -50^0C to 60^0C temperature of several HEMT processes mentioned earlier has been carried out in the MACS research group in The University of Manchester. Figure 2 shows the change in transconductance at different temperatures with the same bias to achieve peak transconductance at room temperature. Transconductance is an indication of the gain of a device with DC characteristics. Hence a variation of this DC parameter signifies gain fluctuation which has an enormous ef-
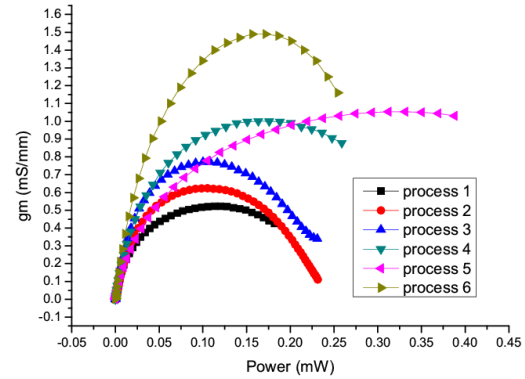

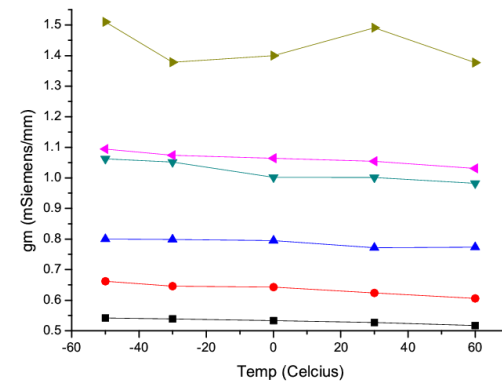Fig. 1: Normalised gm against power for six HEMT processes

Fig. 2: Normalised gm variation with temperature with bias for peak gm at room temperature

fect on system calibration. There is a necessity of temperature stabilization to avoid this problem.

4. LNA Topologies

For the purpose of reducing noise figure to ultra low levels at room temperature, LNA topologies have experienced a wide variety of innovation and creativity. Single ended input and output LNA is a mature and time tested topology. Extremely low noise figures have been measured at room and cryogenic temperatures. 14K noise temperature with 15dB associated gain at room temperature based on 90nm CMOS technology has been reported in Belostotski & Haslett (2007). ASTRON and University of Manchester have reported 35K noise temperature with 42dB and 25dB gain respectively. Low loss baluns have been developed to cater to the interface between differential antennae and single-ended LNA. But in SKA the noise temperature allotted to LNA is 16K. Due to a lossy passive structure, noise contribution of baluns is much higher than 16K. With the elimination of a balun and insertion of appropriate low noise element the overall receiver noise can be reduced

significantly. Though differential amplifiers have matured in digital and amplification applications, their credibility and acceptability is yet to be established authoritatively in LNA development for ultra low noise applications. The crucial design aspect of differential LNA is to keep the common mode rejection ratio (CMRR) very low. 25K differential noise has been measured by (Belostotski & Haslett 2008). FG-IGN in collaboration with ASTRON has also reported a fully differential LNA based on commercial off-the-shelf components with TLNA 35K. Moreover due to the system architecture, differential input and single ended output LNA topologies has been investigated. Out of this necessity novel LNAs have been designed (Bhaumik et al. 2009) and fabricated successfully. The primary challenge of the design described in Bhaumik et al. (2009) was to eliminate practical imbalances in the two arms differential stage of LNA. A different approach has been developed by transforming the differential output of a truly differential LNA to single ended with a RF transformer. CSIRO has reported such LNA based on off-the-shelf components with 35K NT and 28dB gain. Another important aspect of all the LNAs developed is the input impedance which depends directly on the impedance of antennae. Impedance mismatches give rise to standing waves at the input of LNA which effects noise performance (Lera-Acedo et al. 2009). Single-ended LNAs with input impedance of 50Ω and 85Ω and differential LNA of 100Ω, 120Ω, 150Ω, 270Ω and 300Ω input impedances have been developed.

5. LNA Performances

LNA development teams across the globe have designed and measured an exhaustive set of diverse amplifiers with very competitive and promising performance. In the following sections, a brief summary of reported measured data of different LNA teams involved in SKA has been stated.

I. **ASTRON APERTIF LNA and FG-IGN** (Bij de Vaate 2009; Garcia-Perez 2010)

ASTRON has concentrated on developing single ended LNA with Avago Technology's GaAs pHEMT devices and 70nm GaAs mHEMT process of OMMIC. As a part of APERTIF, ASTRON has measured a 50Ω hybrid LNA which operates from 0.9GHz to 2GHz. The LNA displays a flat gain of over 40dB, average return loss below -10dB and noise temperature of 35K. At 1.4GHz the LNA exhibits an OIP3 of 25dBm.
The collaborative work between ASTRON and FG-IGN has produced a hybrid LNA with GaAs pHEMT devices of Avago Technology. The differential 150Ω impedance 0.3-1GHz LNA has a NT below 40K with gain over 26dB and average input return loss of -10dB.

II. **CSIRO ASKAP LNA** (Shaw 2009)

In CSIRO, a differential input single ended output hybrid LNA with GaAs pHEMTs supplied by Avago Technology. The LNA operates from 0.7GHz to 1.8GHz with a differential gain of 28dB gain and 35K noise temperature across the band. The input and output impedances of the LNA are 300Ω (differential) and 50Ω (single-ended) respectively.

III. **University of Calgary** (Belostotski & Haslett 2007, 2008)

Both single ended and purely differential MMIC LNAs based on 90nm CMOS technology operating from 0.8GHz to 1.4GHz band have been reported in (Belostotski & Haslett 2007, 2008). The differential LNA displays 15dB differential gain with 25K NT. The LNA has a differential impedance of 100Ω with input return loss less than -12dB in the band of interest. The single ended 85Ω impedance LNA displays 14K NT with 17dB gain and -11dB return loss. The input third order intercept point of the LNA is -18dBm and power dissipation of 43mW.

IV. **California Institute of Technology TDP** (Bardin & Weinreb 2009; Pandian et al. 2006)

The SKA relevant work on LNA within the Technology Development Programme has primarily concentrated on SiGe HBT processes and cryogenic temperatures. 250nm, 180nm, 170nm, 150nm, 130nm and 120nm node SiGe HBT has been characterized at cryogenic temperatures down to 18K. At 300K ambient temperature, a 0.1-5GHz single ended MMIC LNA has a measured performance of 77K NT and 27dB gain. The average return loss is -10dB with a power dissipation of 76mW. The same LNA at 15K ambient temperature has 4K NT with gain and input return loss of 30dB and -14dB respectively. It has OP1dB of -10.5dBm with 20mW power consumption (Bardin & Weinreb 2009). A InP based balanced LNA with 10K average NT and 40dB gain over 1-12GHz frequency range at 12K ambient temperature has been reported in (Pandian et al. 2006). The power consumption of this MMIC LNA is 24mW.

V. **University of Manchester LNA Group**

The Microwave and Communication Systems (MACS) research group has successfully designed and characterized a single ended MMIC LNA using 70nm gate length mHEMT process supplied by OMMIC. A 50Ω input impedance LNA of 1.5mm by 1mm dimension has average gain of 23dB with 35K NT. At room temperature the bandwidth of the LNA is from 0.7GHz to 4GHz with input return loss of -1.5dB.

VI. **University of Manchester InP process development** (Boulay et al. 2009)

The Microelectronics and Nanostructures research group has developed a 1m InP pHEMT process. A single stage 0.2-2GHz LNA with 10dB average gain and -2dB return loss has been measured with 45mW power consumption. It has 12dB gain at 1GHz and 8dB gain at 2 GHz. At 75mW power dissipation the LNA has average noise temperature of 123K in 1-2.5GHz (Boulay et al. 2009).

Table 1: SUMMARY OF MEASURED LNA DATA

LNA Data	ASTRON & FG-IGN	CSIRO	University of Calgary		OPAR		University of Manchester (M&N)	CalTech(TDP)		University of Manchester (MACS)
Gain (dB)	42 & 26	28	7	15 21	27	4	10	40	27 30	25
NT (K)	35 & 35	35	14	25	65	56 10	123	10	77 4	35
Frequency (GHz)	0.9-2& 0.3-1	0.7-1.8	0.8-1.4 0.4-1		0.3-1.9		0.2-2	1-12 0.1-5		0.7-4
Technology	GaAs pHEMT	GaAs pHEMT	90nm CMOS		0.25μm SiGe HBT		1μm InP pHEMT	InP SiGe pHEMT HBT		70nm GaAs mHEMT
Topology	SE&Diff	Diff	SE	Diff	Diff	SE	SE	Diff	SE	SE
Impedance (Ω)	50&150	300	85	100	100	50	50	270	50	50
Temperature (K)	RT & RT	RT	RT	RT	RT	RT 22	RT	12	RT 12	RT

VII. **OPAR**

OPAR has developed differential 100Ω input impedance MMIC LNA based on 250nm SiGe HBT. Noise temperature of 65K of a 100Ω input impedance differential LNA with gain and input return loss of 27dB and -17dB from 0.3GHz to 1.9GHz has been reported. It displays output 1dB compression point of -1dBm with 73mW power consumption. A single ended 0.3-1GHz 50Ω LNA with noise temperature and gain of 56K and 24dB respectively has also been reported. The LNA has OP1dB of -2dBm with 69.3mW power consumption. At 22K ambient temperature this LNA has a NT of 10K with 21dB gain and 37mW power consumption.

6. Differential LNA Measurement Techniques

S-parameter and noise characterization of single-ended LNA is very much well established. There are highly accurate instruments for noise measurement. Characterization of differential LNA is more challenging. Primarily there are two concepts of differential LNA measurement. First method is to characterize a fully differential LNA with baluns at both ends and then use de-embedding techniques to take account of the baluns. In the second procedure, the LNA is characterized without baluns at each end. Using a four port network analyzers the difficulty in S-parameter measurement of differential LNAs is not only reduced but the measurement accuracy is also improved. However noise characterization is still immensely difficult and challenging. A comprehensive and theoretically sound differential noise measurement procedure has been demonstrated by (Belostotski & Haslett 2009). With this method 25K noise temperature of a differential LNA has been measured successfully. A second approach has been developed at CSIRO and NT of

35K of a hybrid differential LNA has been measured. This measured LNA has differential 300Ω input impedance and single ended 50Ω output impedance. The novelty of the measurement method lies in the test fixture calibration procedure. At first the noise temperature of the sample LNA is measured with a cold head. This is followed by Y-factor measurement of the same LNA in the test fixture. THOT is calculated and hence the ENR of the test fixture is determined. The noise figure of several similar samples of the same LNA can be measured subsequently. The advantage of this differential noise measurement method is that LNAs of same production series can be characterized with single calibration. This procedure is non-repeatable if the production LNA design is changed.

7. Conclusions

LNA design, development and measurement procedures have made a significant forward leap. Measured data of 6 single ended and 5 differential LNA based on diverse technology and topology has been stated as part of this paper. However there are few issues and scopes of discussion on them. Firstly, a trade-off between power consumption and linearity should be quantified so that optimum balance between LNA performance and expenses can be struck. First tests State-of-the-art GaAs mHEMT has shown better power efficiency than InP pHEMTs. Process 6 in figure 1 is a very advanced GaAs process which displays much superior transconductance than all other processes which includes state-of-the-art InP pHEMT process. The choice of semiconductor process, could be different for different bands, is very crucial. Secondly, requirement of temperature stabilization is a necessity to capture information for long time spells. Figure 1(b) shows a clear trend of variation of transconductance with temperature. Alternative option is to design temperature dependent LNAs, but it might come at the

cost of noise performance. Lastly, if temperature is stabilized at cryogenic temperatures down to 15K then though performance would enhance dramatically, the system would become very expensive. (Weinreb et al. 2009) has reported a reduction of 51.5K NT (55K to 3.5K) and 4.3dB (36.5dB to 32.2dB) gain along with 78mW (83mW to 5mW) reduction in power consumption when ambient temperature has been reduced to 17K from 300K. Hence it can be clearly perceived that though there is a increase of expense to cryogenically cool, expenses can be reduced significantly due to much less power consumption with the added bonus to minimum possible noise and linearity. But for cryogenic systems, each foundry should be modelled at cryo temperature to generate reliable designs.

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