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Low Frequency Broadband InGaAs/InAlAs Low Noise Amplifiers for SKA

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Abstract. A new high breakdown InP pHEMT has been used in the design, fabrication and testing of wideband Low noise amplifiers for use in the aperture array concept of the SKA. This optically defined 1 μm gate, 800 μm gate width process has permitted the realisation of low noise transistors with NFmin < 0.4 dB (28K) at 2GHz and lower NFmin values at lower frequencies. The large gate width has been instrumental in realising low noise resistances.
We report here on DC, RF and noise performances of novel MMIC Low Noise Amplifiers based on InGaAs/InAlAs pHEMTs, with a full coplanar waveguide (CPW) technology designed specifically for use in the SKA and fabricated using conventional optical lithography.

1. Introduction

The Square Kilometre Array (SKA) is the next generation of radio telescope and will have 100 times more sensitivity than any of the largest telescope to date (Dewdney et al. 2009). For the low frequency spectrum of the SKA, cost-effective Ultra Low-Noise Amplifiers are required at frequencies spanning the range of 300MHz to 2GHz (Hall 2004). InP-based HEMTs have previously demonstrated superior noise performances at millimetre-wave frequencies using short-gate length and are indeed commonly used in high performance LNAs, albeit at cryogenic temperatures. However, in the low frequency range, matching the LNA for wide band, low noise performance becomes a critical issue as it requires adding large passives into the design, which can act as sources of added noise if integrated in the LNA. This can be circumvented by using off-chip components (Belostotski & Haslett 2007), but at the expense of both cost and complexity. Thanks to a novel high-breakdown, low-leakage InGaAs/InAlAs pHEMT structures, developed at Manchester (Bouloukou et al. 2006), and which enables the use of large periphery gate transistors, both low NFmin and low Rn, which are key point for a better impedance matching across the ultra-wide band, can be simultaneously obtained. In addition for low frequency applications, the requirement for extremely high cut-off frequencies is relaxed and larger gate lengths ($\sim 1\mu$m), as opposed to sub-micron, are perfectly adequate in terms of noise performance and stability of the LNA.

2. RESULTS AND DISCUSSIONS

Precise material engineering of the epilayers and doping profile results in on-state leakage Ig < $0.09A/cm^2$ (Figure 1). In order to verify the foundry process, a single stage LNA, based on a 1x800 μm^2 periphery gate transistor has been designed and measured across the whole frequency band of 0.3 to 3 GHz. The design and fabrication of an LNA was based on measurements and modelling of all single elements in the circuit, namely, pHEMTs, inductors, capacitors and resistors.

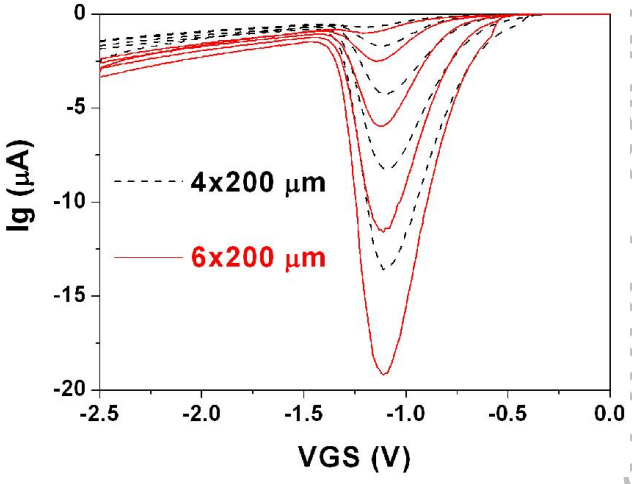

Fig. 1: Typical InGaAs/InAlAs pHEMTs experimental gate current curves for two large gate periphery transistors as a function of drain and gate voltages

LNA Designs (2nd Generation) New LNA designs, based on the latest InGaAs/InAlAs epitaxial structures have been chosen for MMIC fabrication. These had more emphasis on low noise figure, input and output reflection coefficients across the ultra-wide frequency band (0.2 to 2 GHz).

Compared to the 1st generation LNA, this generation of LNAs consisted of new layouts designed to accommodate a range of probe configuration. The LNA 2nd Generation also had designs based on 4x200 μm pHEMTs using the 1 μm gate InGaAs/InAlAs/InP technology, but presented major improvements compared to the 1st generation:

- New resistors designed using 50 $\Omega/\square$. This leads to more accurate values across the sample and more stable fabrication process.

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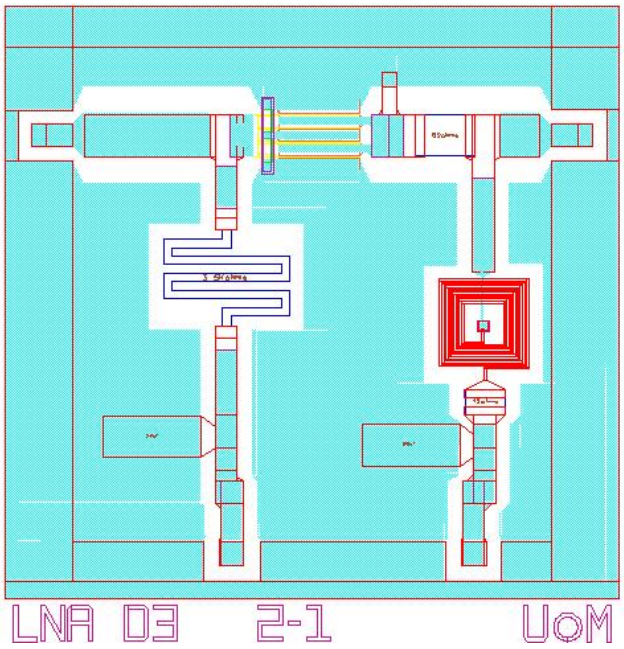

Fig. 2: Schematic picture of MMIC single-stage. The fabricated LNA was 1.52x1.46 mm2

- Each LNA had a unique label identification based on design number, column-row position on the die which made probing easier.
- The interconnects consisted of a double-metal layer which reduced the resistance variation in the connection.
- The RF pads were designed for RF probes with pitches varying from 100 μm to 300 μm.
- The ground metal plane was extended all around the MMIC. This would minimise the chances of generating oscillations.
- The DC feeds were modified accordingly to our probe pin configuration.
- New process control monitors and RF de-embedding structures were carefully designed and placed on 7 locations on the die.

MMIC Single-Stage LNA A full MMIC single-stage LNA was designed using on-chip integrated input and output matching, as shown in Figure 2. This LNA was successfully measured at MC2 for both RF and noise. The DC was supplied by multi-DC probes, including decoupling capacitors, and designed accordingly with our layout specifications.

These completed first trials MMIC, which have power gain of 15 to 9dB across the band (Figure 3) have noise figures of 1.5dB, larger by some 0.5dB than expected by simulation (Figure 4). The reasons for the discrepancies are being addressed in a new run where improvements have been brought to the next generation design with better grounding. Also double stage LNA designs have been implemented which should reduce the broad band noise to 0.5 dB. A likely reason for the increased noise compared with simulated ones can also be attributed to the fact that during full MMIC fabrication, the temperature depositions of the Silicon Nitride capacitors might

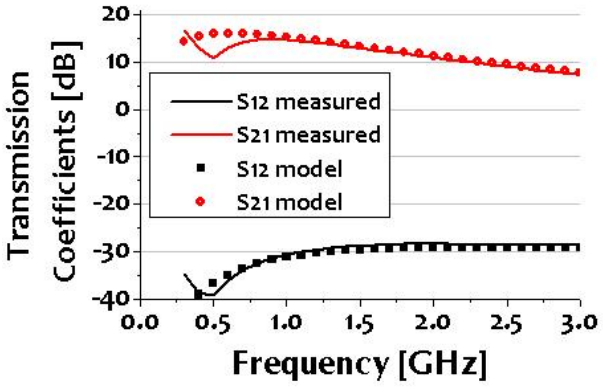

Fig. 3: Measured and modelled S-parameters for a single stage LNA based on a 1 μm gate length 4x200 μm InGaAs/InAlAs transistor

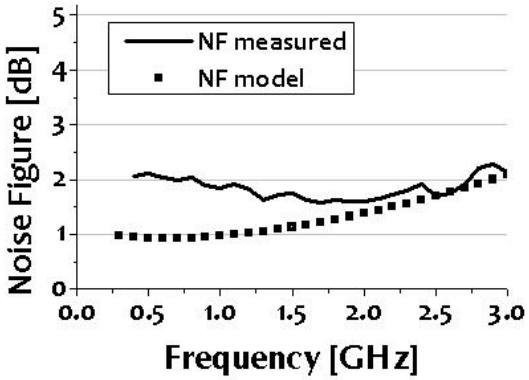

Fig. 4: Noise measurements at 25 mA drain current on a single stage LNA based on a 1μm gate length 4x200 μm InGaAs/InAlAs transistor

have been too high which caused the transistors to have leakages much higher than those shown in figure by a factor of 5 which will certainly contribute to the noise figures observed.

The key features of these stable single stage amplifiers are the very low power dissipation of 75 mW, well within the power requirements of SKA. The purpose of this work was also to demonstrate that CPW can be used at these frequencies for low noise designs and yet still meet size limitations necessary for low cost production. The attractive features of this process include reduced back side processing, no vias, and suitability for flip chip mounting.

MMIC Double Stage LNA Design With Off-Chip Components A double-stage LNA design was developed using off-chip components for reducing parasitic losses at the input path. The design was simulated in ADS using the nonlinear models of the fabricated pHEMT and the passive components. The input matching was achieved using off-chip inductors in order to preserve the LNA noise figure from being affected by the large series resistance (about 20-30 Ω) usually found in integrated inductors. The two-stage LNA operating from a 3V power supply was designed to include the on-chip

output matching network. It consists of two common source amplifiers. The first stage was designed to provide a simultaneous noise and impedance match by carefully adjusting the two off-chip inductors at the input using a 4 200 μm gate width pHEMT as a building block. Simulation results for this LNA design are shown in Figure 5.

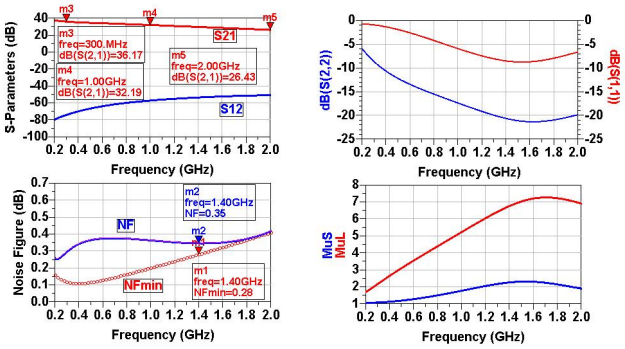

Fig. 5: Simulation results of double-stage MMIC LNA design with off-chip components

The noise figure remains below 0.45 dB between 0.3 and 2 GHz, while the gain is above 26 dB below 1.4 GHz. The input and output return losses S11 and S22 were below -9 dB and -14 dB, respectively at 1.4 GHz. The third order intercept obtained from LNA simulations was 14 dBm. The circuit also showed unconditional stability up to 30 GHz with a total power dissipation of about 100 mW. Table 1 conveys the main simulations results compared with those reported in the literature at this frequency band. The LNA presented in this paper shows noise characteristics amongst the best published to date especially when considered in the light of the relatively large, optically defined gate length of the transistor used here (1 μm). The high gain LNA presented in (Rosenbaum et al. 1993) was obtained using a three-stage circuit which would dissipate large amounts of power but would probably have higher IP3.

Clearly, this design would be a very strong contender for the low frequency band of the SKA. This LNA has successfully been fabricated and is being measured now.

Fully Integrated Double-Stage LNA Design Another full MMIC double-stage LNA was prepared with on-chip components for input and output matching. As expected, the gain was higher than 30 dB across the band, while dissipating a total power of about 110 mW. The overall noise figure was expected to be lower than 0.7 dB between 0.2 to 2 GHz, and less than 0.5 dB across most of the frequency band, as shown in Figure 6.

Double-Stage Differential to Single-Ended MMIC LNA Design Considering the interfacing requirements of the LNA in the receiver chain of SKA, a differential to single-ended MMIC LNA design has been prepared. This design comprises two stages where the first stage is fully differential, optimised for noise performance with reasonable gain, while the second stage is a gain and stability boosting stage with differential input and

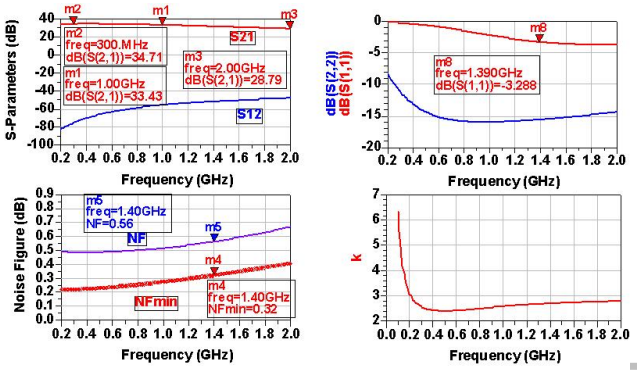

Fig. 6: Simulation results for double-stage MMIC LNA design

single-ended output interfaces. The noise performance of the first fully differential stage is considerably better as compared to the second differential to single-ended conversion stage due to the balanced topology. Due to the considerable high gain of the first stage (12-15 dB), the relatively degraded noise performance of the second stage has minimal effect on the amplifier's noise characteristics, as expressed by the Friis' expression for noise figure of cascaded microwave networks (Friis 1944). The designed LNA optimised for noise figure and power consumption with reasonably high gain of 302 dB for the low frequency band of SKA (0.3-1 GHz). A noise figure of less than 0.6 dB with unconditional stability for the entire frequency band of interest is predicted for this design with power dissipation of 300mW. The simulated results presented in Figure 7 show high losses at lower frequencies for the input because of the absence of input matching network. Reasonable output SWR S22 and good reverse isolation S12 are predicted for the design. Layouts and masks are currently being prepared for this design.

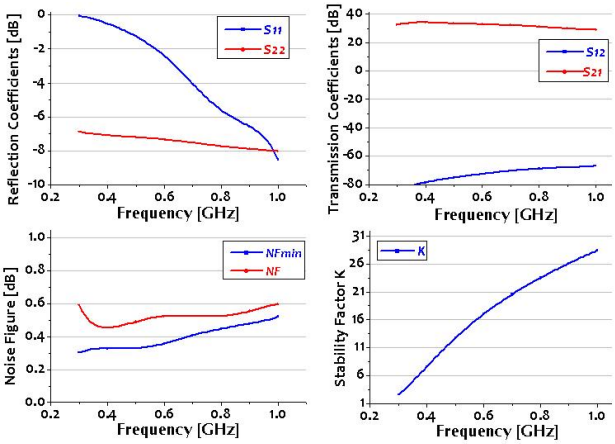

Fig. 7: Simulation results for double stage differential input single-ended output MMIC LNA design

Table 1: Summary of the main ultra low noise amplifiers below 2.5 GHz, at room temperature

Bandwidth (GHz)	NF (dB)	Technology	Power (mW)	IP3 (dBm)	S21 (dB)	Ref.
0.7 - 1.4	0.35	90 nm-CMOS	45	7.5	20.5 - 16.3	Belostotski & Haslett (2007)
0.6 - 1.6	0.5	0.5 μm GaAs pHEMT	852	15.4	29.3 - 20.9	Xu et al. (2005)
2.25 - 2.5	0.5	0.15 μm InGaAs/InAlAs HEMT	?	?	> 35	Rosenbaum et al. (1993)
0.3 - 2	0.45	1 μm InGaAs/InAlAs pHEMT	110	14	26	This work

3. Conclusion

LNA designs based on a newly developed high breakdown, large gate periphery (and hence low noise resistance) transistors have been implemented and successfully fabricated in the 2nd generation of LNAs. These were based on work carried out on accurate modelling of passives and pHEMTs using the 1μm gate InP technology developed at the University of Manchester. Major improvements have been made on these LNAs which mainly concentrated on achieving low noise figure across the ultra wide frequency band (0.2 to 2 GHz). The best LNA is expected to exhibit less than 0.4 dB noise figure at room temperature across the whole band, still using a cost-effective 1μm gate technology. This shows great promises for future development using sub-micron gate lengths.

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