

Low-power LVDS driver using InP HBT ECL circuits for SKA

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Abstract. Indium phosphide Heterojunction Bipolar Transistors (HBTs)-based, low power, Low Voltage Differential Signalling (LVDS) driver to interface digital circuits operating at varied logic levels is designed using Emitter Coupled Logic (ECL) circuits operating at 2 GHz clock speed. The core of the ECL circuit is based on a voltage to current converter/buffer. The total power dissipation of the driver with LVDS compatible output levels is less than 15mW. This is achieved with a relaxed geometry of $5 \times 5 \mu\text{m}^2$ area HBT devices fabricated on Molecular Beam Epitaxy (MBE) grown wafers. The circuit makes use of dynamic switching of output transistors without using any complex circuitry, which reduces total power consumption without appreciably compromising on speed or area. These results are better than those reported on $0.35 \mu\text{m}$ CMOS technology and is comparable with designs built on $0.35 \mu\text{m}$ BICMOS technology.

1. Introduction

Indium phosphide Heterojunction Bipolar Transistors (HBTs) offer cut-off frequencies as high as 450 GHz at $0.5 \mu\text{m}$ feature size and digital circuits based on InP HBT technology using Emitter Coupled Logic (ECL) operating at frequencies above 150 GHz have been demonstrated (Rodwell et al. 2008a). f_{max} as high as 750 GHz with 250 nm emitter length has also been recently reported (Rodwell et al. 2008b). In addition to higher speed operation its input turn-on voltage is much lower than that of GaAs based HBTs, since InP HBTs use low-band gap material of InGaAs for the base, resulting in low-power dissipation for circuits built on InP technology.

System-level integration invariably requires interfaces between circuits operating at different frequencies and at varied logic levels. For short range mediums, Low Voltage Differential Signalling (LVDS) is a very popular interface because of its small voltage swing and its immunity to cross-talk as it is based on differential signalling and good EMI performance (LVDS Manuel 2008; Abugharbieh et al. 2008) due to less current switching as emitter-coupled logic is a non-saturating logic requiring almost constant supply of output current (Jaeger & Blalock 2007). This is also why its power dissipation is not a strong function of frequency unlike CMOS.

In this work, InP single heterojunction bipolar transistors (SHBTs) with relaxed geometry of $5 \times 5 \mu\text{m}^2$ are used to design a very low-power LVDS driver proposed to be used in the receiver chain of SKA (Square Kilometre Array)-a phase array based, largest radio telescope that is being planned at the moment (Schilizzi et al. 2008) which requires very small power budget and extensive back-end digital signal processing.

2. Growth and Fabrication

The wafers were grown on a RIBER V100+ solid source Molecular Beam Epitaxy (MBE) on $\langle 100 \rangle$ oriented, semi-insulating Fe-doped InP substrates. The relaxed geometry devices of area $5 \times 5 \mu\text{m}^2$ were fabricated using a triple mesa, wet

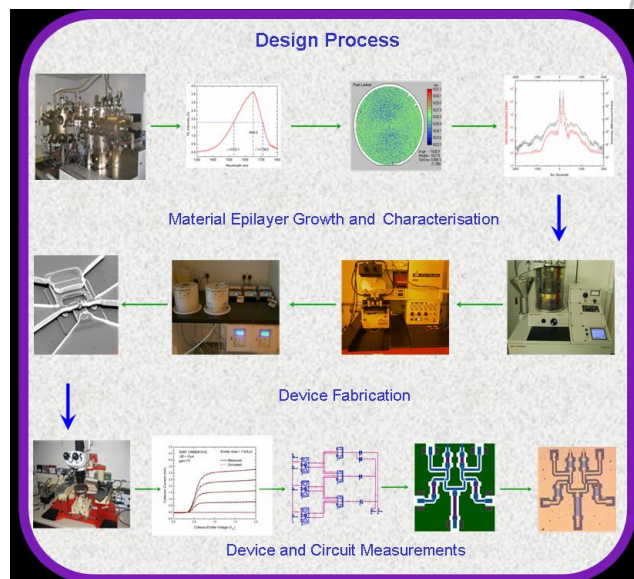


Fig. 1: Design cycle from wafer growth to MMIC fabrication

etching process. Epitaxial layers were first etched using a non-selective ortho-phosphoric based etchant $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (3:1:50). This was followed by a short selective etch of $\text{HCl}:\text{H}_2\text{O}$ (1:1) to expose the InGaAs base and sub-collector layers. Non-alloyed Ti/Au contacts to the emitter, base and sub-collector layers were then thermally evaporated to complete the devices. The process uses standard i-line based optical lithography because of very relaxed minimum feature size of $5 \mu\text{m}$.

InP based single heterojunction bipolar transistors (SHBTs) used in this work are grown, characterised, fabricated, and measured at The University of Manchester as depicted in Figure 1.

3. Device and Circuit Modelling

Agilent HBT device model (Agilent Technologies 2006) is developed using parameter extraction routines specifically designed for this proprietary model by Agilent Technologies.

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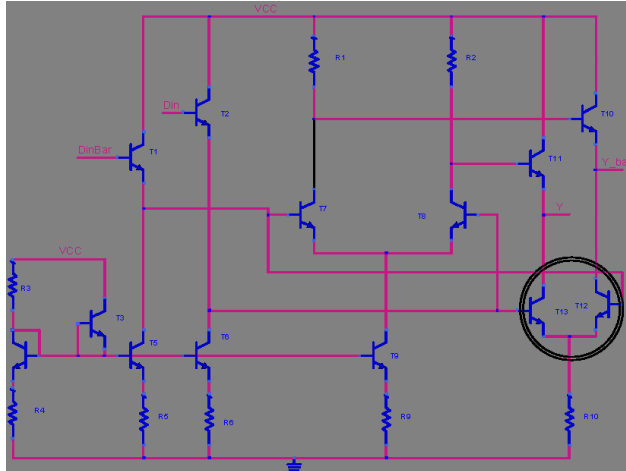


Fig. 2: LVDS driver with voltage to current converter.

This non-linear, parametric model is based on the University of California, San Diego (UCSD) model (UCSD High Speed Devices Group 2000) which takes into account Kirk effect, velocity modulation effect, large knee voltage and other typical features of III-V HBTs.

The circuit implementation of LVDS driver comprises two additional output transistors (encircled in Figure 2) than the conventional ECL stage.

These additional criss-cross connected transistors are used to switch off current between the differential output circuits. Dynamic switching off of the output transistors without using any extra circuitry conserves considerable power (Abugarbieh et al. 2008), which in our designs was up to 20% reducing total power dissipation from 19 mW to less than 15 mW. Tail current for the differential pairs are provided using Wilson current mirror configuration to improve the output impedance of the basic current mirror design. Emitter resistors are used to reduce the temperature sensitivity of the circuit by offsetting the reduction in the turn-on voltage of the transistors as the temperature goes up.

Voltage to current translators are used at the output stage to meet stringent load termination requirements of the LVDS standard. ECL input as shown in Figure 3 is the simulated random data which is fed to a simple master-slave D-latch stage (not shown). This stage gives input to the LVDS driver, which translates ECL levels to LVDS compatible levels as described below and as shown in Figure 3.

LVDS standard requires the following typical output values: Voltage swing of 250 to 400 mV Offset voltage of $1.2 \pm 0.2V$ Termination resistor of 100 Ohm differential

4. Conclusion

In this work, a complete low voltage differential signalling (LVDS) driver is designed and simulated to work with ECL circuits operating at 2 GHz clock speed. The total power dissipation of the driver complete driver circuit is less than 15 mW. The driver is designed to interface Analogue to Digital

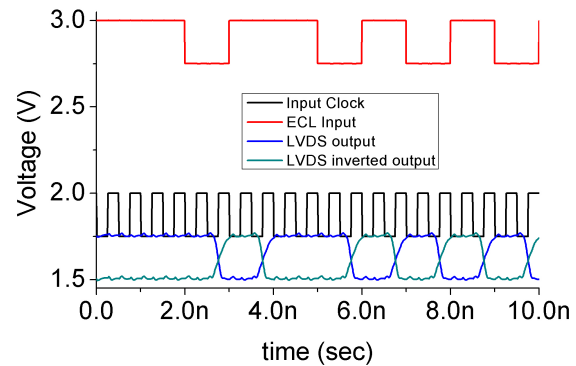


Fig. 3: LVDS driver input and output waveforms

Converter (ADC) with emitter coupled logic levels to the back-end digital signal processing block of a radio telescope receiver chain through its built-in LVDS receiver.

This power consumption is lower than that of designs reported using $0.35\mu\text{m}$ CMOS technology and is comparable with designs built with $0.35\mu\text{m}$ BICMOS technology. This reported InP HBT design has the added advantage of compatibility with the mainstream high speed InP technology.

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