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Low Power, High-Speed ADCs and Digital Circuits for SKA

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Abstract. The design of ultra low power (< 300 mW), high-speed analogue to digital converter (ADC) is an essential element for the Square Kilometre Array (SKA). This paper describes the design and simulation of a low-power high-speed (4GS/s) analogue to digital converter (ADC) based on two designs of InP/InGaAs Single heterojunction bipolar transistor (SHBT) ($5 \times 5\mu m^2$ and $1.5 \times 5\mu m^2$ emitter area device). The essential difference between these two devices was the process reliability (yield), and thus the overall unit cost. Both devices provided DC and RF performance characteristics ideally suited for the low-power IC design, with high current gain of 70-80. The high-frequency performances differ due to the device geometry with an ft/fmax=78GHz/38GHz for the $5 \times 5\mu m^2$ and ft/fmax=91GHz/83GHz for the $1.5 \times 5\mu m^2$ emitter area device.

1. Introduction

Logic gates that are based on current mode logic (CML) and emitter coupled logic (ECL) circuits are an ideal choice for applications with high clock rates Nah et al. (1993); Montgomery et al. (1991); Hafizi et al. (1992); Yinger et al. (1993). CMOS technology is limited in high precision applications, such as ADCs due to the stringent requirement of device matching. Also to achieve high-speed (fT > 100 GHz) CMOS requires deep sub-micron gates (90nm or less) where expensive phase shift masks are required. HBTs on other hand offers high power handling capability, high current drive capability, low 1/f noise characteristics, excellent threshold voltage control and high speed performance with low power dissipation for the digital circuits.

2. Growth and Fabrication

The technology was developed at the University of Manchester (UOM) and used molecular beam epitaxy (MBE) growth which relied upon two novel developments. Firstly stoichiometric conditions permitted growth at a fairly low temperature of 420oC while conserving extremely high quality materials. Secondly, dimeric Phosphorus was generated from a gallium Phosphide (GaP) decomposition source leading to excellent RF device properties. The epitaxial layer structure of SHBT is shown in Table 1. The relaxed geometry devices of area $5 \times 5\mu m^2$ and $1.5 \times 5\mu m^2$ were fabricated using a triple mesa, wet etching process. Epitaxial layers were first etched using a non-selective Ortho-Phosphoric based etchant H3PO4:H202:H20 (3:1:50). This was followed by a short selective etch of HCl:H20 (1:1) to expose the InGaAs base and sub-collector layers. Non-alloyed Ti/Au contacts to the emitter, base and sub-collector layers were then thermally evaporated to complete the devices.

Table 1: Epitaxial structure of SHBT sample

Layer	Material	Doping (cm^{-3})	Thickness (Å)
Cap	$In_{0.53}Ga_{0.47}As$	$n = 1 \times 10^{19}$	1350
Emitter 1	$In_{0.53}Ga_{0.47}As$	$n = 1 \times 10^{19}$	1350
Emitter 2	InP	$n = 1 \times 10^{17}$	400
Spacer	$In_{0.53}Ga_{0.47}As$	-	50
Base	$In_{0.53}Ga_{0.47}As$	$p = 1.5 \times 10^{19}$	650
Collector	$In_{0.53}Ga_{0.47}As$	$n = 1 \times 10^{16}$	6300
Sub-Collector	$In_{0.53}Ga_{0.47}As$	$n = 1 \times 10^{19}$	5000
Buffer	$In_{0.53}Ga_{0.47}As$	-	100
Substrate	Semi-Insulating InP		

3. Device Modelling

The measured common-emitter characteristics and cut-off frequency verssus the collector current of the two devices are shown in Figure 1 and Figure 2, respectively. As depicted in Figure 2, SHBT_$1.5 \times 5\mu m^2$, devices were the most suitable for the low-power high-speed applications because of demonstrating high frequency characteristics at relatively low values of collector current. However, SHBT_$1.5 \times 5\mu m^2$ were not fabricated because of the poor yield (30%). On the other hand, SHBT_$5 \times 5\mu m^2$ showed a good yield of over 90% and thus were favourable from fabrication point of view. The simulations were carried out for both of the samples and a comparison study is made.

Transistor parameters were extracted Maas et al. (1992); Lee et al. (2005) from the transistor for non-linear modelling in Agilent's ICCAP and Advanced Design System (ADS) software. This software includes the small-signal University of San Diego (UCSD) model (standard SPICE Gummel-Poon modified model) for the HBT UCSD (2000). The modelled and measured common emitter characteristics of SHBT_$5 \times 5\mu m^2$ and SHBT_$1.5 \times 5\mu m^2$ are shown in Figure 3 and Figure 4, respectively.

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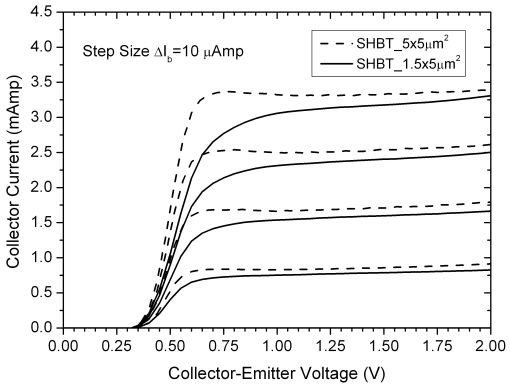

Fig. 1: IV Characteristics of two samples

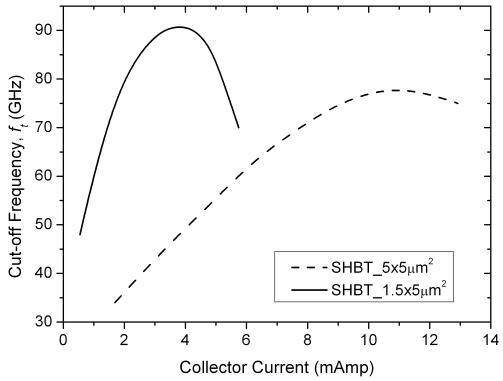

Fig. 2: Ic vs ft comparison of two samples

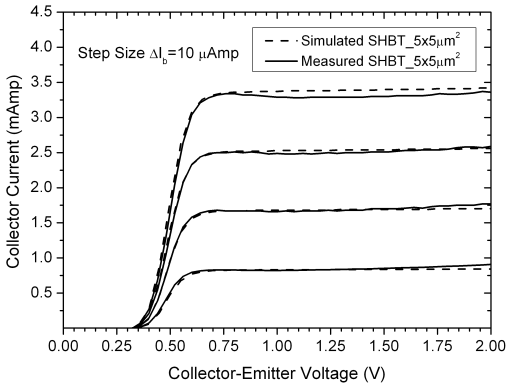

Fig. 3: Modelled and Measured SHBT_5 × 5μm^2

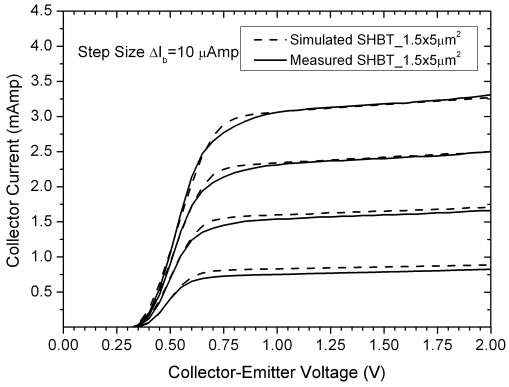

Fig. 4: Modelled and Measured SHBT_1.5 × 5μm^2

4. Circuit Simulations

4.1. Comparator

The most important building block of the flash ADC is the differential latching comparator (Figure 5). The speed of the latching comparator is determined mainly by its recovery time, t_r, which can be expressed Hotta et al. (1986) by

$$t_r = C_L R_L \equiv C_L \frac{\Delta V_0}{I_L} \quad (1)$$

where CL is the collector load capacitance, RL is the collector load resistance, IL is the tail current and VO is the output voltage swing.

The tail current for sample SHBT_5 × 5μm^2 is chosen to be 720μA with the recovery time of 166ps and which is well under the Nyquist frequency (500ps divided by 2 as level triggered clocking) for 1GHz input signal. The performance was acceptable for 333MHz input signal and up to 600MHz but there was a large slew rate that was comparable to 1GHz input signal and thus the circuit required further optimisation. The slew rate can be decreased by increasing the tail current and reducing the collector resistors. However, this exceeds significantly the power

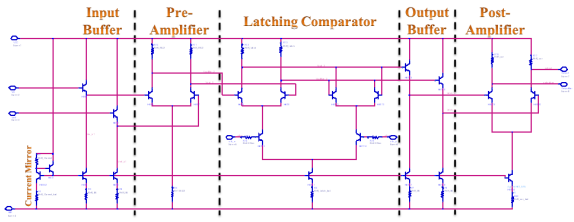

Fig. 5: Circuit Diagram of Differential Latching Comparator

limits - designing a 4-Bit ADC with power consumption less than 300mW.

The device was replaced by SHBT_1.5 × 5μm^2 which has improved ft and fmax at much lower collector current. The circuit was re-optimized (resistors and current mirror) and simulations were conducted on the latched comparator to decide on suitable load currents for this transistor at the clock frequency of 4GHz. The higher clock rate helps in tracking the signal more accurately. The recovery time of 125ps is the upper limit for the latching comparator clocked at 4GHz. To reduce the impact of meta-stable states, and improve sensitivity, a maximum

recovery time of 60ps was chosen, setting the tail current to be 520μA.

The simulated differential latched comparator results for two devices are shown in Figure 6. It can be easily observed that device SHBT_1.5 $\times$ 5μm^2 has given much better output characteristics as compared to SHBT_5 $\times$ 5μm^2 and thus chosen for 4-Bit Flash ADC simulation. The improved results were mainly due 4 times lesser CBC of SHBT_1.5 $\times$ 5μm^2 as compared to SHBT_5 $\times$ 5μm^2.

4.2. Flash 4-Bit ADC

The full 4-Bit flash ADC includes 15 comparators, 15 XORs, 32 diodes and resistor ladder producing a low-power consumption of 240mW for 2GHz clock and 290mW for a 4GHz clock.

5. Conclusion

The continuing research into the design an ultra low-power 4-Bit A/D converter for use in the upcoming Square Kilometre Array (SKA) is presented in this paper. One design currently under investigation is the flash folding ADC, which has demonstrated a power consumption of $\sim$ 150 mW. With further optimisation of the transistor epilayer design, an ultra-low power, GHz class ADC is possible using this technology.

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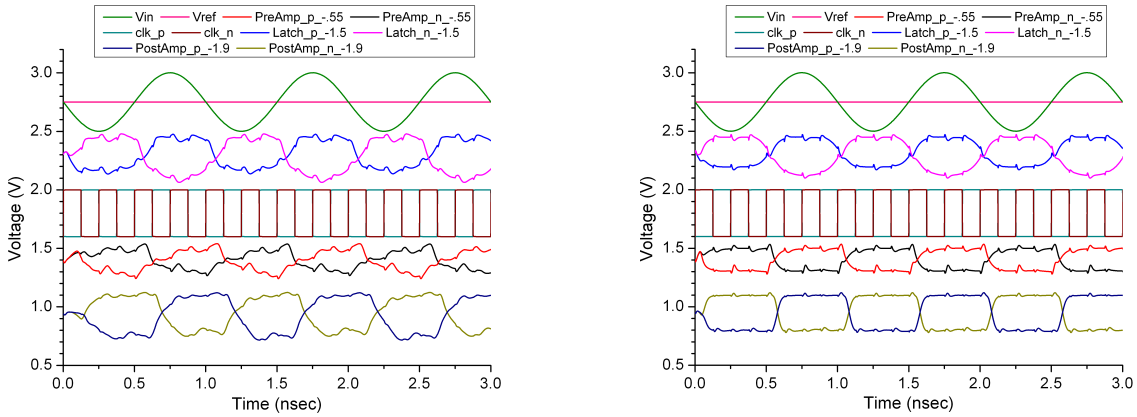

Fig. 6: Comparison of Simulation Results of Different Samples left: 4GHz Clock, 1GHz Input Signal SHBT_5 $\times$ 5μm^2 right: 4GHz Clock, 1GHz Input Signal SHBT_1.5 $\times$ 5μm^2