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Integrated receivers for mid-band SKA

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Abstract. A new System-on-Chip (SoC) receiver is proposed utilising an advanced Silicon on Sapphire CMOS process, to be developed as a collaborative venture between CSIRO Australia Telescope National Facility and an industrial partner. This receiver is targeted for mid-band SKA pathfinder use, covering an RF tuning range in excess of 700 to 1800 MHz, with a 300 MHz instantaneous bandwidth. The receiver features high dynamic range and low noise temperature. The Silicon on Sapphire process promises high reverse isolation and good device matching, allowing the use of a quadrature I/Q downconversion scheme. This paper summarises research to date on integrated receivers at CSIRO, as well as an overview of the proposed receiver design.

1. Introduction

The simultaneous requirements for mid-band SKA of wide RF tuning range and instantaneous bandwidth, large Field of View (FoV) and large collecting area pose significant challenges, not least of which is the number of receivers required to achieve the specifications.

A representative mid-band SKA design (Schilizzi et al. 2007) is shown in table 1, utilising Phased Array Feeds (PAFs) to extend the FoV of a conventional 15 m dish.

The FoV specification of 20 deg^2 with a 15 m dish necessitates a dual-polarisation PAF incorporating approximately 400 elements. When multiplied across the 2500 dishes required to meet the sensitivity specification, approximately 1 million receiver elements will be required. Increasing the dish diameter necessitates a larger PAF in order to maintain the same FoV, but a smaller number of dishes. Decreasing the dish diameter requires a larger number of dishes, each with a smaller PAF, so the actual number of receiver elements stays relatively constant.

Table 1: Representative PAF mid-band SKA design.

Collecting area	1 km^2
FoV (at 1.4 GHz)	20 deg^2
Sensitivity	7000 m^2/K
Survey speed	1×10^9 m^4/K^2.deg^2
Observing frequency	500 – 2000 MHz
Processed bandwidth	300 MHz
Dish diameter	15 m
Number of dishes	2500
PAF elements	~ 400
PAF data rate [a]	~ 2.5 terabits/s
Total no. of receivers	~ 1 million

[a] 8 bit digitiser.

Previous dish-based telescopes in this frequency range have utilised single feeds per dish, or at the most a relatively small number of narrow-band discrete feeds. The total cost of the receivers is generally swamped by the cost of metalwork. The high NRE costs associated with integrated receiver development, along with the performance obtainable by discrete designs, firmly tips the scales in favour of lower levels of integration for these telescopes.

Even the Australian SKA Pathfinder (ASKAP) telescope currently under development by CSIRO (DeBoer et al. 2009), with some thirty-six 12 m dishes equipped with 188 element PAFs utilises a discrete receiver built with commercial off-the-shelf components. In this case, the weight of the discrete receiver, as well as concerns about radiated RFI from LO and sample clocks, has necessitated that only the LNA and RF filter are located at the feed, with the downconverter and sampler for each channel located in the dish pedestal.

In order to achieve the per-unit weight, power and cost savings necessary for construction of mid-band SKA, a significantly higher level of integration than that achieved to date is clearly required. Monolithic IC processes, most notably RF-CMOS, SiGe, and Silicon-on-Insulator (SoI) CMOS processes offer good performance in the frequency ranges of interest, at significantly lower per-unit cost than both discrete designs and III-V processes such as InP and GaAs. The NRE costs associated with these processes would be amortised over the massive number of receivers used in the SKA.

2. RF-CMOS proof-of-concept receiver

While there are numerous examples of RF-CMOS being used for 2.4 GHz and 5 GHz wireless networking (Valla et al. 2005; Li et al. 2003) and mobile telephone handsets (Song et al. 2005), radio telescope receivers have heretofore not made significant use of RF-CMOS. Until recently, this has made good sense; the unusual requirements of extremely low noise, very wide bandwidths, and the relatively modest numbers of receivers in most radio telescopes tip the scales firmly in favour of more costly high performance GaAs and InP processes, or indeed hand-crafted discrete designs. It is only very recently that the performance of RF-CMOS processes, most notably in

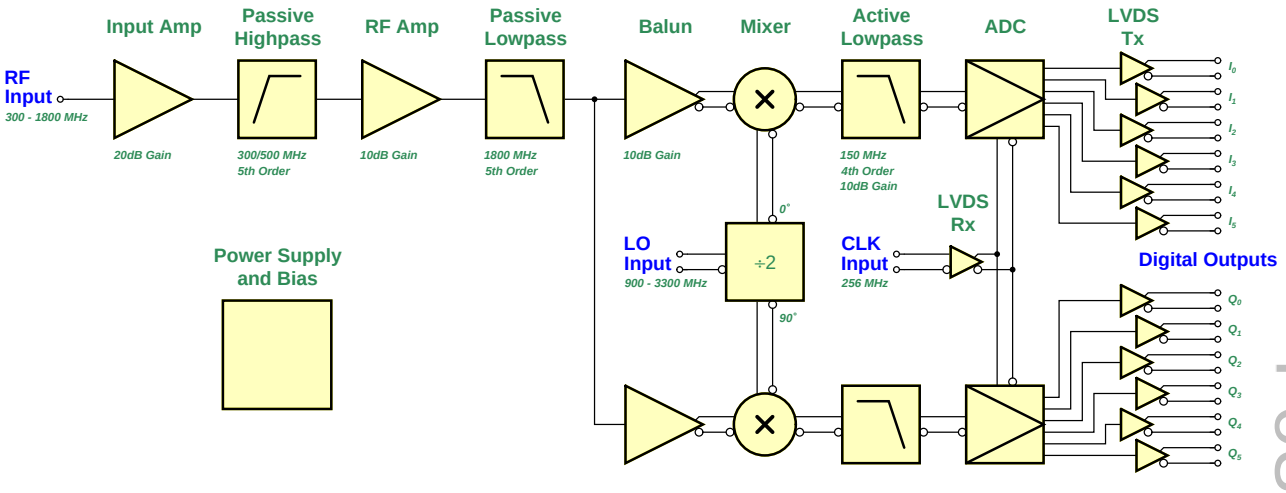

Fig. 1: A simplified block diagram of the proof-of-concept integrated receiver. The RF filter features a bypassable 300 MHz high-pass filter. A direct quadrature downconversion topology is used, with 300 MHz instantaneous bandwidth achieved using a pair of 500 Msps six-bit ADCs.

terms of f_T, has approached that of these more traditional methods, such that we may contemplate building radio telescope receivers in RF-CMOS without incurring a significant performance penalty. The increasing use of PAFs and aperture array receptors, made possible in part by advances in digital CMOS processing, with their large number of receiver elements has made the traditional discrete and partially integrated receivers less attractive due to their relatively high per-unit costs.

Whilst the potential cost advantages of RF-CMOS are clear and the raw performance metrics extremely encouraging, questions remained regarding what level of performance could be achieved in practice from low-cost RF-CMOS processes. A proof-of-concept RF-CMOS System-on-Chip (SoC) receiver has been developed using a representative 0.18 μm RF-CMOS process in order to gain further familiarity with RF-CMOS. Developing a receiver using RF-CMOS allowed us to make a much better informed judgement as to the applicability of RF-CMOS for radio astronomy than would be achieved by simply evaluating designs intended for consumer electronics.

The high levels of integration afforded by a monolithic process make possible techniques that are not common in discrete designs; most notably the use of a direct quadrature downconversion topology, as depicted in Fig. 1. The direct downconversion topology allows us to dispense with the second conversion found in a typical dual-conversion heterodyne receiver, whilst maintaining a high degree of image rejection. It has the added benefit of allowing the use of a pair of half-rate samplers, in addition to only requiring low-pass anti-aliasing filters, in place of the band-pass IF filters of a conventional design.

The effective image suppression afforded by a quadrature downconverter is predicated upon an accurate phase and amplitude relationship being maintained between the two LO signals, as well as matched phase and amplitude characteristics in all baseband components (Razavi 1997). The degree of image rejection for a quadrature downconverter with a given amplitude and phase imbalance at the I/Q outputs may be calculated trigonometrically, and is given by:

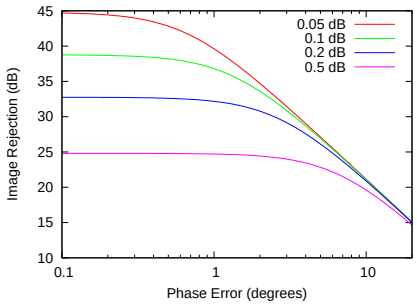

Fig. 2: The effect of a number of amplitude imbalances combined with phase imbalance on image rejection.

$$\text{Rejection} = 10\log_{10}\left(\frac{1+2\left(10^{\frac{\delta}{10}}\right)\cos(\theta)+\left(10^{\frac{\delta}{10}}\right)^2}{1-2\left(10^{\frac{\delta}{10}}\right)\cos(\theta)+\left(10^{\frac{\delta}{10}}\right)^2}\right)\text{ dB},$$

where δ represents the amplitude error between I and Q outputs in dB, and θ represents the phase error from 90 degrees. This relationship is shown graphically in Fig. 2. In order to achieve 35 dB image suppression, phase imbalance must be constrained to better than 1 degree, and the amplitude imbalance to better than 0.1 dB.

Referring again to Fig. 1, the signal flow through the receiver is from left to right. The receiver takes an RF input from the antenna element, as well as a two-times LO signal, and performs RF amplification, filtering, downconversion and sampling, with the output being in the form of two six-bit LVDS digital signals. By incorporating both an LNA and an ADC on the chip, we are able to evaluate the effects of high levels of integration, most notably the degree of isolation achievable between the digital circuitry and the sensitive RF front end.

RF filtering is performed using passive lumped-element L/C filters, separated into high-pass and low-pass sections due to the wide fractional RF bandwidth specification. The mixers are a conventional Gilbert cell design, utilising a high-speed

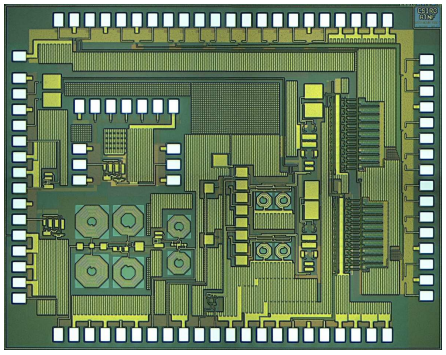

Fig. 3: A photomicrograph of the proof-of-concept receiver. The receiver measures 3.5 mm by 2.75 mm, and is packaged in a 56 pin 8x8 mm QFN package.

Current-Mode Logic (CML) divide-by-2 flip-flop to generate an accurate 90 degree offset LO signal. The baseband anti-aliasing filter is an active design, utilising differential high-speed op-amps.

A photomicrograph of the proof-of-concept receiver is shown in Fig. 3. The entire receiver fits easily on a 3.5 mm by 2.75 mm 0.18 μm CMOS die. The design is pad-limited, due to the large number of pads required to output the 12 LVDS bits. Spare space on the die is used for test circuitry, including a second input amplifier and RF amplifier. The passive RF filter occupies as much die area as both the ADCs, chiefly due to the size of the inductors.

The input amplifier is a noise cancelling design (Bruccoleri et al. 2004), making use of a shunt-feedback matching stage and conventional cascode common-source amplifying stage to match the input over a decade bandwidth while achieving low T_n.

Results from the proof-of-concept receiver show the promise of CMOS in radio-astronomy receiver applications. The RF circuitry performs well. Measured results for the packaged input amplifier are compared with simulated values in Fig. 4 and Fig. 5. The amplifier has more than 20 dB gain across the RF band. The measured noise temperature mid-band is 170 K. As a comparison, the mid-band figure for the shunt-feedback amplifier alone (as used in the second stage RF amplifier) is 250 K, indicating 80 K of noise cancellation. The input amplifier is extremely well matched. Input return loss is better than 20 dB across most of the RF band, with an output return loss of better than 16 dB. The amplifier has an output-referred 1 dB compression point of +2 dBm, and +13 dBm OIP3.

The performance of the passive RF filter is extremely promising, despite the inherent losses from implementing such large structures in bulk CMOS. As shown in Fig. 6, the complete filter has a mid-band gain of 2 dB, as a result of a 10 dB amplifier interposed between the high-pass and low-pass sections. The filter has better than 30 dB attenuation below 120 MHz. Substrate coupling limits the attenuation to around 30 dB above 3200 MHz. The filter is well matched, with better than 10 dB input and output return loss across the filter passband.

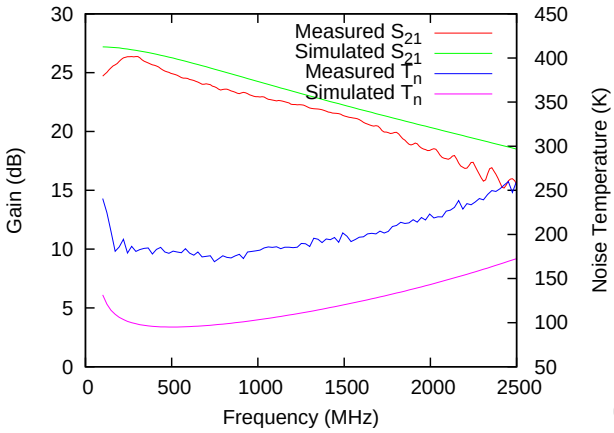

Fig. 4: Input amplifier forward gain and noise temperature.

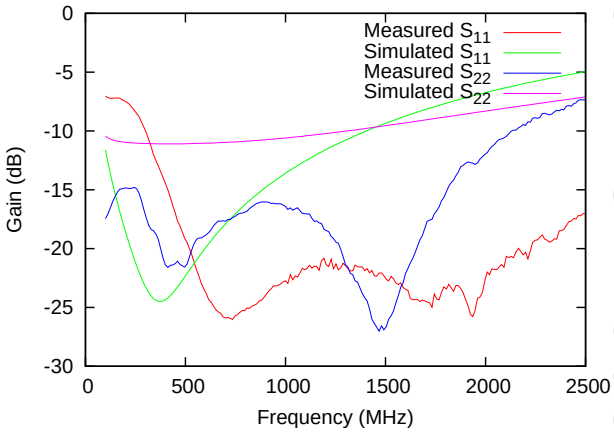

Fig. 5: Input amplifier input and output match.

I/Q phase and amplitude match are similarly encouraging. As can be seen in Fig. 7, the paths are matched to within 1 degree, after a constant 2 degree offset (due to differences in the

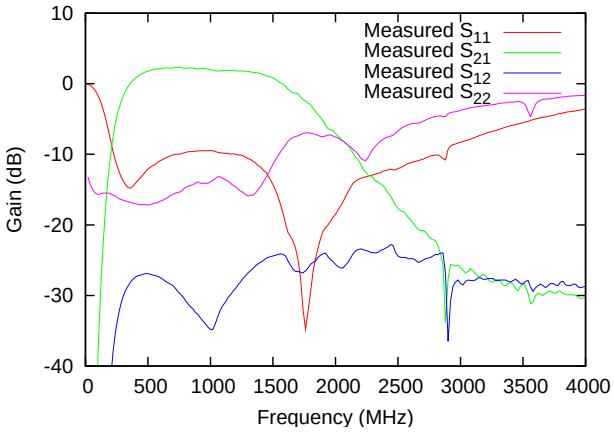

Fig. 6: RF filter measured response - 500 MHz lowpass disabled.

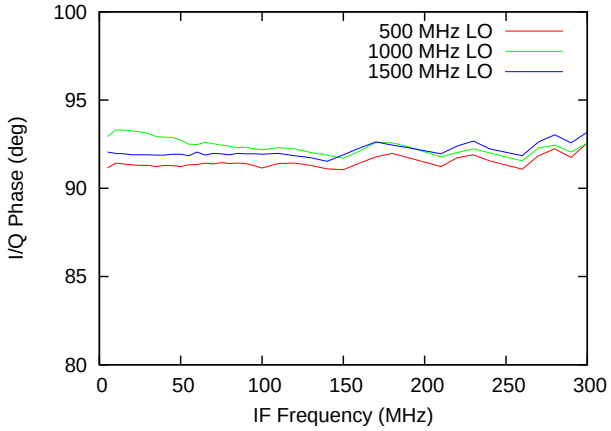

Fig. 7: Gilbert cell mixer measured I/Q phase balance.

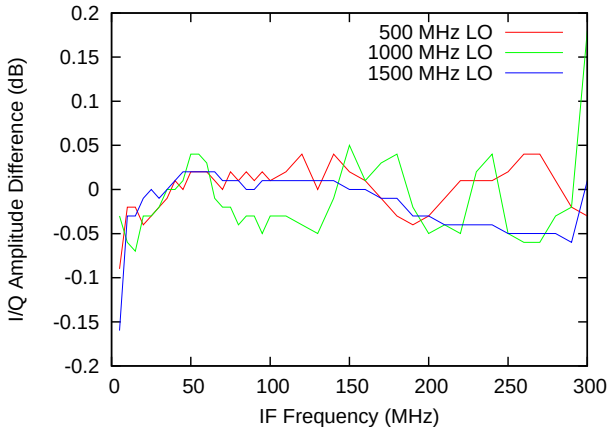

Fig. 8: Gilbert cell mixer measured I/Q amplitude balance.

capacitive and resistive parasitics for the I and Q monitoring subsections) is removed. The amplitude balance between the I and Q outputs is shown in figure 8. The two channels are matched to within 0.1 dB over the entire baseband frequency range.

The ADCs are a six-bit design, utilising two stages of averaging termination and interpolation, with distributed sample and hold (Scholtens & Vertregt 2002). Rather than using comparators, the ADCs use fixed gain error amplifiers. The output of each error amplifier is averaged with those of neighbouring amplifiers to reduce systematic offsets caused by process variations. The thermometer-to-binary encoder uses a fat-tree topology, with two stage pipelining to increase speed. Operation of the ADCs was hampered by coupling between the digital outputs and the sample clock input, limiting the maximum sample rate to 150 Msps on the I channel, and 80 Msps on the Q channel. Notwithstanding this problem, which may be rectified by a simple layout change, operation of the ADC at reduced sample rates was encouraging. A 16,384 point FFT of a 1.01 MHz sinewave, as shown in Fig. 9 shows a clear 40 dB SFDR for the SoC receiver from the mixer forwards. This measurement was

Table 2: Sample clock feedthrough at LNA input

Frequency	Clock leakage power
256 MHz fundamental	-82.6 dBm
512 MHz 2nd harmonic	-91.5 dBm
768 MHz 3rd harmonic	-83.2 dBm
1024 MHz 4th harmonic	-81.9 dBm
1280 MHz 5th harmonic	-77.9 dBm
1536 MHz 6th harmonic	-76.4 dBm

taken with a 100 MHz sample clock, using an RF input to the mixers of -25 dBm at 501.01 MHz, and a 500 MHz LO.

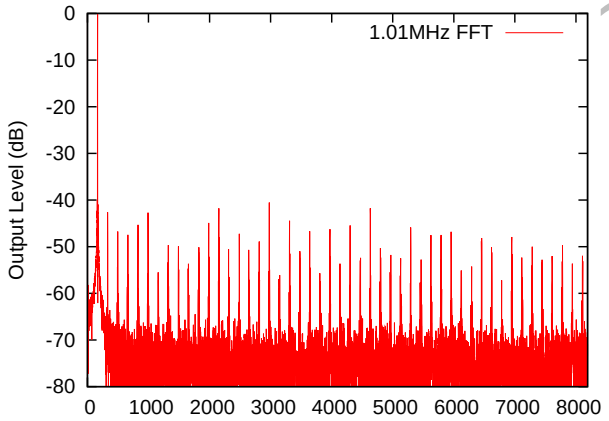

Fig. 9: SoC receiver ADC FFT

A final important measurement is the degree of sample clock feedthrough back into the analog and RF sections of the SoC receiver. A 0 dBm 256 MHz sample clock was supplied to the ADC, and measurements made of the power at various harmonic frequencies at the LNA input port. As shown in table 2, the clock is suppressed by more than 76 dBm across the entire operating range of the receiver.

The proof-of-concept receiver shows the applicability of commercial RF-CMOS processes for radio-astronomy receivers. RF performance was promising, and the degree of matching possible between circuits on the same die allows the use of topologies that have generally been shunned previously. The receiver shows the value of implementing the LNA as a separate circuit, both in order to minimise physical heating of the LNA by 'power-hungry' later stages and to minimise LO and sample clock leakage into the front-end. Separation of the LNA allows this component to be fabricated in the fastest available CMOS or InP process, to achieve lowest T_n.

3. Proposed Silicon on Sapphire receiver

A new Silicon on Sapphire receiver is proposed as a collaboration between CSIRO and industry, utilising an advanced

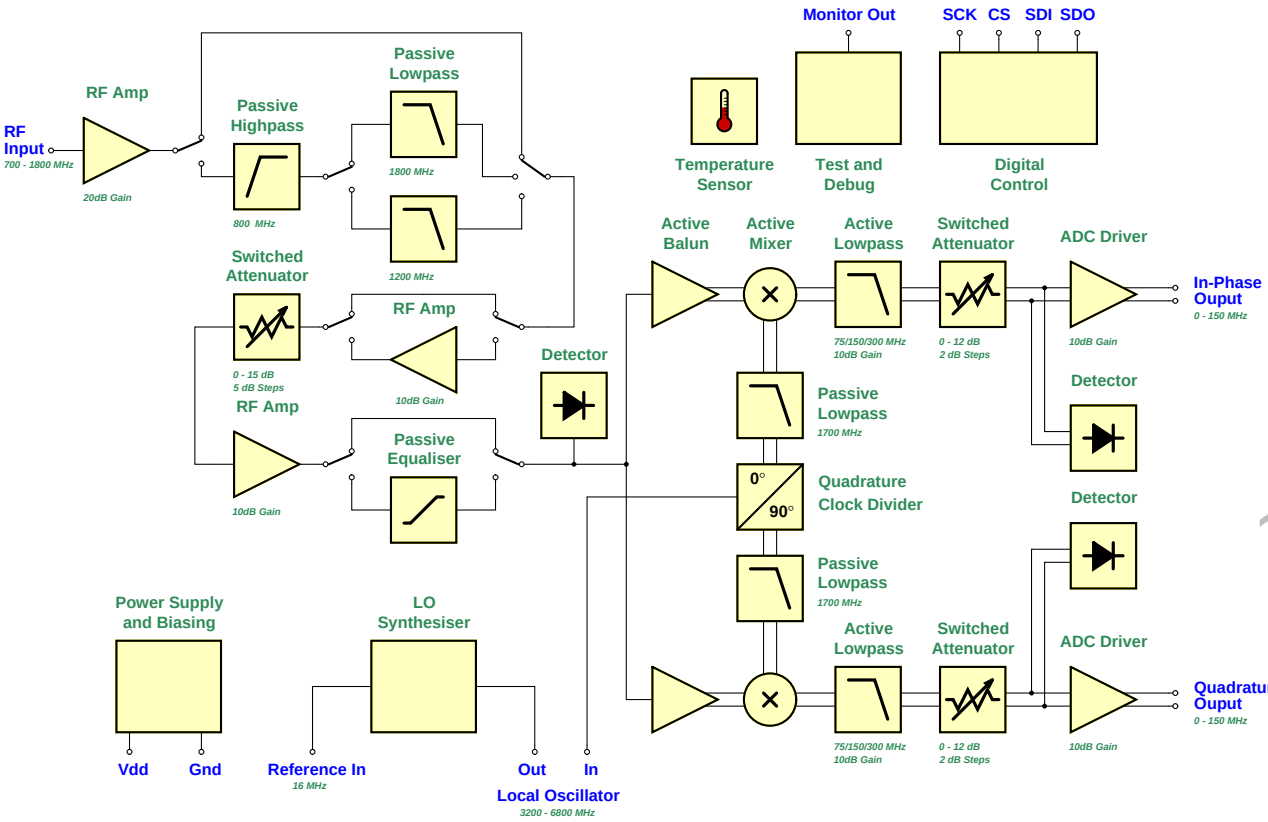

Fig. 10: A simplified block diagram of the proposed Silicon on Sapphire integrated receiver. The LNA and ADCs from the proof-of-concept receiver have been omitted in favour of off-chip parts. The receiver features an on-board LO synthesiser, as well as a high degree of configurability in terms of RF and baseband gain and filtering.

0.25 μm CMOS process, built on a thin layer of silicon grown on a sapphire wafer. The sapphire substrate is an extremely good insulator, making for very high-Q passive devices, as well as a significant reduction in substrate-borne coupling, making possible the design of components with high levels of reverse isolation. The proposed receiver will integrate all components from the LNA output to the ADC input, and will include an LO synthesiser. A separate LNA is being developed in the same process, utilising an inductively degenerated common-source amplifier, with a capacitively coupled cascode stage to improve input bandwidth (Belostotski & Haslett 2007). It is intended that the receiver will utilise a commercial off-the-shelf ADC, such as the e2v AT84AD001B dual 1 Gbps unit.

As with the proof-of-concept RF-CMOS receiver, the new receiver is based on a direct quadrature downconversion topology, as depicted in Fig. 10. The new receiver will operate over the frequency range 250 MHz to 2.5 GHz. It will have on-board, bypassable passive L/C RF filters to suit the ASKAP PAF; a 700 MHz high pass and a selectable 1200 or 1800 MHz low pass, to ensure that RF at the LO second harmonic is suppressed when working at the bottom of the RF band. The new receiver makes good use of the high performance RF switches available in the Silicon on Sapphire process, with a high degree of gain adjustability in the RF section, of 34–59 dB in 5 dB steps (including off-chip LNA gain of 25 dB), and 8–20 dB in the baseband section, selectable in 2 dB steps.

It is planned to synthesise the LO directly on chip, utilising a number of switchable VCOs in order to cover the necessary LO tuning range whilst maintaining good phase noise. The LO will be divided digitally in order to generate the quadrature signal to drive the mixers, ensuring an accurate 90 degree phase relationship for good image rejection.

The baseband sections will also be designed with a view to flexibility. In order to accomodate a wide range of instantaneous bandwidths, the active baseband anti-aliasing filter will be switchable between 75, 150, and 300 MHz, for 150, 300, or 600 MHz instantaneous bandwidths respectively. As with the RF section, a degree of gain adjustability is included in the baseband section, of 8–20 dB in 2 dB steps. The differential baseband outputs will be buffered to suit an off-chip COTS ADC, with an adjustable DC offset servo, so that the entire baseband section may be DC coupled, minimising the size of the mid-band hole necessitated with an I/Q topology.

To make best possible use of the RF and baseband gain and bandwidth adjustability, detectors are included in both the RF path and each baseband path. It is envisaged that these detectors will be implemented using a series of cascaded limiting amplifiers and rectifiers, in order to provide 60 dB of useful range.

Table 3: Proposed Silicon on Sapphire receiver specifications

RF frequency range	700–1800 MHz (250–2500 MHz with RF filters bypassed)
Instantaneous BW	150/300/600 MHz selectable
Dynamic range	> 40 dB
RF input T_n (dB)	170 K (2 dB)
RF gain range	14–39 dB, variable in 5 dB steps
RF & LO input	Single-ended 50 Ohms
Baseband output	0 to 75/150/300 MHz DC coupled quadrature buffered differential I and Q signals suitable for direct connection to ADC
Baeband gain range	8–20 dB, variable in 2 dB steps
I/Q mismatch	< 1 degree & < 0.05 dB over baseband frequency range
Power consumption	< 5 W

The receiver will include a temperature detector on-chip, and will be housed in a 28 pin plastic QFN package. The design power dissipation for the receiver is less than 5 W.

Proposed specifications for the receiver are summarised in table 3.

4. Conclusions

In order to meet the simultaneous bandwidth, FoV, and sensitivity requirements for the SKA, whilst minimising cost, weight, and power requirements, some form of highly integrated receiver will be necessary. Development of a proof-of-concept RF-CMOS receiver by CSIRO has shown this process to be well suited to the fabrication of high-volume, low-cost, low-power, and high-performance receivers for mid-band SKA.

CSIRO proposes to continue the development of receivers for the SKA with a new Silicon on Sapphire CMOS receiver, as a collaboration with industry, targeted around the ASKAP requirements, but with wide applicability to other PAF and aperture array designs.

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