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Recent Experimental Results from the NA62 Gigatracker Prototypes: an Hybrid Silicon Pixel Detector with 100 ps Time Resolution

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The Gigatracker (GTK) is the upstream detector developed for NA62, the experiment that will study the rare decay of a kaon into a pion and neutrino-antineutrino pair at the CERN Super-Proton-Synchrotron (SPS) accelerator. The GTK, besides performing the momentum and angular measurements of the incoming particles, will provide a time information with a precision of 100 ps (rms) in order to obtain a tight time coincidence between the kaon and the pion tracks [1]. The required time resolution can be achieved by compensating for the discriminator time-walk. For this purpose two complementary architectures have been explored. The complete separation between the analog and the digital sections is the key feature of the first solution. The discriminator output of the simple pixel cell is sent to Time-to-Digital-Converters (TDC) shared by a group of pixels in the end of column [2]. In the second option the signal processing inside the pixel is maximized, implementing a Constant-Fraction-Discriminator (CFD) followed by a TDC in each cell [3]. The two architectures have been designed and produced as small-size prototypes in 130 nm CMOS technology. The results obtained from laboratory and beam tests of the ASICs bump-bonded to 200 μm thick silicon sensors are described in this paper.

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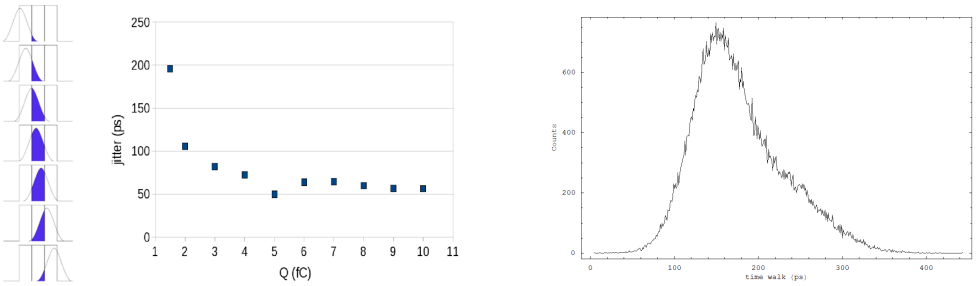
1. The NA62 experiment and the GTK detector

The NA62 experiment will exploit the CERN SPS to measure the branching ratio of the very rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$. This channel is extremely attractive since its theoretically very clean character allows to make a decisive test of the Standard Model. The data coming from two spectrometers, one for the beam and one for the decay products, will be used to reconstruct the tracks of 80 interesting events having a signal to background ratio of 10%. Particle identification, momentum measurement and photon vetoing are used in order to suppress the background.
The momentum and angular measurements of the incoming particles and the timing information are provided by the GTK. It consists of three stations of hybrid silicon pixel detector, each formed by a 60x27 mm^2 and 200 μm thick sensor bump-bonded to ten front-end chips. The GTK most critical issue is the time resolution which should be better than 200 ps (rms) on the single station. The jitter induced by noise and the time-walk are the main factors affecting the timing precision. Given its systematic nature, it is possible to correct the time-walk off-line using the Time-over-Threshold (ToT) technique. The signal amplitude is measured by recording the times at which the leading and the trailing edges of the discriminator pulse cross the threshold. Besides increasing the amount of data to be transmitted, a very precise calibration of the time-walk vs ToT curve must be performed for each pixel to get the required timing accuracy. Alternatively a self-ompensating method, such as a CFD circuit, can be used. A bipolar signal with a zero crossing time independent from the signal amplitude is obtained by comparing a delayed copy of the signal with an attenuated one. Drawbacks are a more complex architecture, higher space occupation and power consumption.
Two complementary architectures have been explored. Off-line data correction and a minimal pixel cell are the key features of the first one. Each cell consists of a transimpedence amplifier followed by a leading-edge discriminator. The discriminator output is sent downstream to the end of column where a Delay-Locked-Loop based TDC shared by a group of pixels provides the ToT information. The second architecture uses the relatively big area of the pixel (300x300 μm^2) to perform time-walk compensation, using a CFD, and digital conversion, with on-pixel TDCs. Prototypes of both solutions have been designed and produced in 2009 and bump-bonded and tested in 2010.

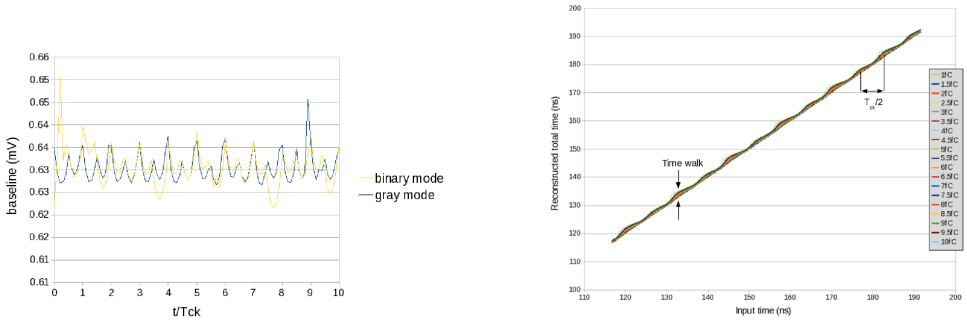
2. Test results from TDC-per-Pixel Demonstrator

The TDC-per-Pixel demonstrator consists of a matrix of three columns and two spared pixels for analog testing. Since almost all signal processing is performed already at pixel level, each cell contains a significant digital section which causes the substrate noise to be a critical issue.
The jitter was measured moving the phase of 10^3 synchronous signals in steps of 20 ps (Fig 1(A)) and calculating the rms of the count distribution obtained for each TDC bin. A jitter lower than 100 ps (rms) was observed at 2.4 fC.
Monitoring the analog output of the CFD in test pixels with the clock switched-off a time-walk vs charge curve was obtained which, convoluted with the expected Landau for the experiment, gives a the time-walk of 92 ps (rms). The same quantity measured from the end of column with the digital part active shows an average time-walk higher than 500 ps (rms). This deterioration is due to modulations on the baseline that corrupt the shape of the CFD bipolar signal. The modulation is synchronous to the clock (Fig. 2) and is mostly due to the digital drivers that propagate the clock



(A) (B)

Figure 1: (A) Jitter measured from a matrix pixel. (B) The convolution with the NA62 Landau gives 92 ps



(A) (B)

Figure 2: (A) Baseline modulation at the CFD output. (B) A Test Pulse delay scan was performed. The output times were reconstructed for charges from 1 fC to 10 fC. The spread of the curves represents the time-walk. Each hill corresponds to a clock transition, while the ideal curve would be a straight line

towards the pixel matrix. An improved design foresees to embed the drivers in a dedicated well. Furthermore an amplifier less sensitive to the digital noise pick-up has also been developed.

3. Test results from End-of-Column (EoC) Demonstrator

The EoC demonstrator consists of a single folded column surrounded by test pixels. Injecting charge at the pixel center with a laser, the time resolution resulted in 70 ps (rms) at 2.4 fC (Fig. 3). The concept of transmitting out of the pixel precise timing signals with an integrated

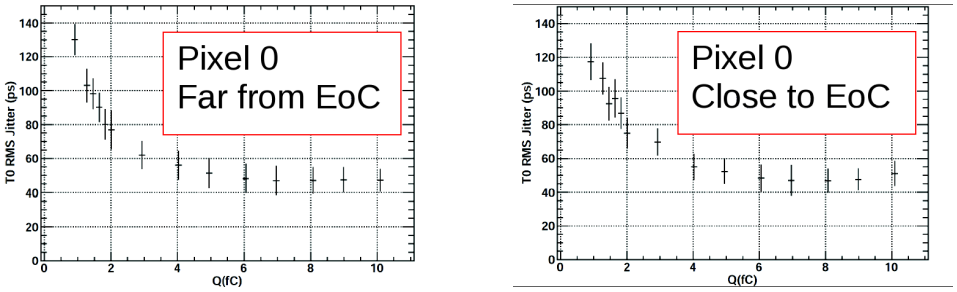


Figure 3: Time resolution measured for laser charge injection at the pixel center results in 70 ps at 2.4 fC

transmission line was confirmed. No particular issue with digital noise pick-up has been found. In the beam test the resolution obtained was 175 ps (rms). The deterioration of the resolution is

mostly due to the non uniform geometry of the electrical field in the pixel (Fig. 4) and to the charge straggling along the sensor. Both the phenomena cause a shape variation of the input signals and affect every architecture, however the CFD should be less sensitive to shape variations than the ToT.

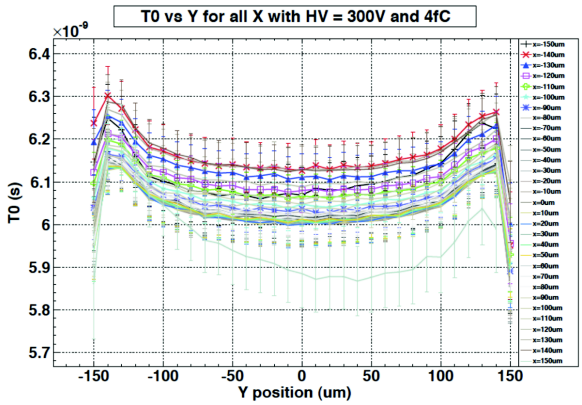


Figure 4: A complete laser scan of the pixel highlights the border effect contribution to timing error

4. Summary and Outlook

Two ASICs implementing two complementary architectures have been designed and produced in the R&D of the GTK for NA62 experiment. The first solution is based on a simple cell, which was crucial to minimize the digital noise pick-up, and on off-line time-walk compensation. While proving excellent performances at the electrical test, a time resolution degradation was observed in the beam test leading to 175 ps (rms). This value is still adequate for the purpose of the experiment, but is relatively close to the 200 ps (rms) limit specification. The challenge will then be in preserving the good performance measured with the prototype at the full system level.
All the blocks in the TDC per pixel architecture were functional, but the on-chip digital noise limited the global timing performance to 500 ps (rms). In principle a CFD based approach, besides reducing significantly the burden of the calibrations, could be less sensitive to the effect deriving from statistical shape variations
For these reasons a full-size version of the EoC is now in preparation and will serve as the baseline solution for the experiment, while an improved version of the CFD based architecture is under development as a possible back-up/upgrade solution.

References

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