

Design of the front-end digitization electronics for a G-APD-based Cherenkov telescope camera

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The First G-APD Cherenkov Telescope FACT is a project to demonstrate operation of Geiger-mode avalanche photo diodes for ground based Cherenkov astronomy in a full-scale camera. Currently in its commissioning phase, the camera will be used for gaining practical experience with operation of the novel light sensors in the environment of a Cherenkov telescope and for long-term monitoring of variable Gamma-ray sources. The analogue preamplifier and the digitization electronics of FACT are described in this contribution.

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1. FACT

The First G-APD Cherenkov Telescope (FACT) is a project using Geiger-mode avalanche photo diodes (G-APD) for ground based Cherenkov astronomy in a full-scale camera [1]. The first objective of FACT is demonstrating that these novel light sensors are a viable alternative to photomultiplier tubes. The second objective is to use the telescope for long-term monitoring of variable Gamma-ray sources.

FACT uses the refurbished former HEGRA CT3 telescope on La Palma (9.2 m² mirror). The camera has 1440 pixels, 4.5° field-of-view (0.11° per pixel), and will operate also under twilight or moon conditions (background rate up to 5 GHz per pixel). The power consumption is about 600 W, the weight 140 kg. The sensor gain will be stabilized to 5% using a feedback loop operating on light pulses emitted by an LED-based pulser. Solid PMMA light concentrators are used to extend the sensitive area of the G-APD by taking advantage of the uniform acceptance of G-APDs up to high inclination angles.

The camera has been installed on the telescope in October 2011 and is currently commissioned.

2. Front-end electronics design

Each pixel corresponds to a read-out channel, thus in total 1440 channels. For triggering, an analogue sum of 9 channels is used, which is discriminated and then fed into a majority logic. All digitization and triggering electronics has been integrated into the camera, data transfer to the counting room is over Ethernet fibers.

The electronics is arranged in 4 custom-designed, water cooled crates, with each one holding ten electronic board pairs. All fast digital signals, like for example the trigger and the read-out clocks, are transported over commercial Category 6 Ethernet cables.

Each board pair consists of an analog preamplifier and a digitizing board described in more detail below. Connection between the pairs is made with one mid-plane connector per crate, which carries additionally supply voltages and RS-485 slow communication lines.

The G-APDs used in FACT are from Hamamatsu, model S10362-33-50C (3x3 mm² area, 50x50 μm pixels). The gain is 7.5×10^5 at an operation voltage of about 70 V.

3. Preamplifier board

The preamplifier boards are completely custom designed. The pulse from a G-APD is passed through a current buffer (a BFR182 transistor in base configuration), and turned into a voltage pulse over two parallel 390 Ω resistors. The signal is then passed through an operational amplifier (OPA3691) and split into two branches, one fed into the analog summing of the trigger logic, the other into the digitizer board (see below).

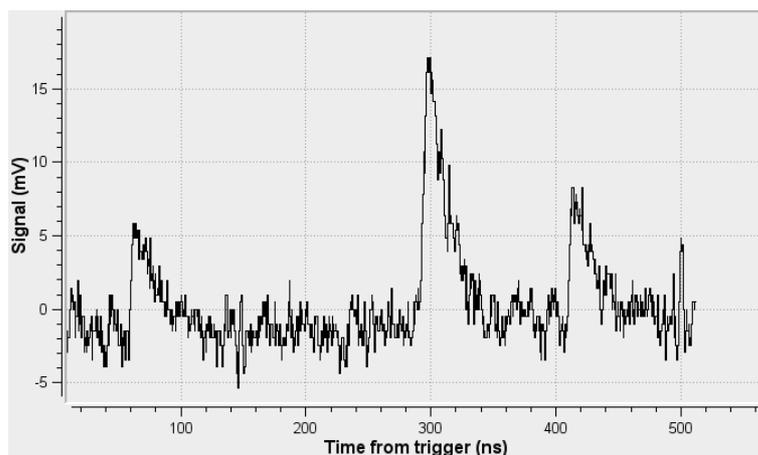
The trigger is formed from a nine-fold analog sum (channels can be disabled). Cable-based clipping is used to limit the length of the summed pulse to 10 ns. After further amplification, a trigger primitive is generated by a mezzanine board on the preamplifier and sent to the trigger master over coaxial cable, which finally decides on a valid trigger using an adjustable majority of the trigger primitives. The total gain for the trigger branch is 1.6 mV/μA.

4. Digitizer board

The digitization is based on the DRS4 analog pipeline chip, developed at PSI [2]. Each digitizer board has, as the preamplifier, 36 channels, sampled by 4 DRS4 chips at 2 GHz. Read-out of the DRS4 and the associated analog-to-digital converter running at 25 MHz is controlled by an FPGA (Xilinx XC3SD3400A). The Ethernet interface is implemented with a Wiznet W5300 chip, providing 8 TCP/IP sockets for downlinking data, one of them also used for the command uplink. Data transfer to the Wiznet is also controlled by the FPGA.

The singled-ended signals from the preamplifier are converted into differential form suitable for the DRS4 by an input buffer. The common-mode voltage is adjustable. A voltage for the amplitude calibration of the DRS is also fed into this buffer. Timing calibration of the DRS4 uses a 250 MHz clock generated by the trigger master that is capacitively coupled into one channel of each DRS4. LEDs on the FAD allow diagnosing the basic board status in case no communication over TCP/IP is possible.

All DRS4 chips on all FAD boards are locked using their internal phase-locked loop to a common frequency generated by the FTM. Precise relative timing of all channels to significantly better than 300 ps is therefore possible after the fixed aperture jitter of the DRS4 is calibrated. A high-precision time marker, generated by the trigger master, is imprinted on the analog signal, also capacitively coupled.



The Wiznet chips of all boards are connected to two Gigabit switches, connected in turn by optical fibers to the counting house. Data saturating the 100 MBit/s bandwidth of the Wiznets can be downlinked simultaneously (about 300 MByte/s).

The achievable resolution is illustrated by the graph with signals resulting from G-APD dark counts.

The gain of the digitizing signal branch is $1.8 \text{ mV}/\mu\text{A}$, a single avalanche has an amplitude of 7.5 mV. The double avalanche is due to optical cross talk within one G-APD. The noise level is about 2 mV root-mean-square, the dynamic range extends to 2 V.

References

- [1] H. Anderhub et. al, Nuclear Inst. and Methods A 628, 107 (2011)
- [2] S. Ritt, R. Dinapoli, U. Hartmann, Nuclear Inst. and Methods A 623, 486 (2010)