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The Silicon Vertex Detector of Belle II

M. Friedl*, **T. Bergauer, P. Dolejschi, A. Frankenberger, I. Gfall, C. Irmler, T. Obermayer, D. Smiljic, M. Valentan**

Institute of High Energy Physics (HEPHY), Austrian Academy of Sciences, Nikolsdorfer Gasse 18, A-1050 Vienna, Austria

E-mail: markus.friedl@oeaw.ac.at

Y. Onuki

Tohoku University, 6-3 Aoba, Aramaki, Aoba-ku, Sendai, Miyagi 980-8578, Japan

T. Tsuboyama

KEK, 1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan

The Belle experiment at KEK (Tsukuba, Japan) was successfully operated from 1999 until 2010 and confirmed the theoretical predictions of CP violation which led to the Nobel Prize in 2008. In order to precisely study rare decays, more statistics and thus a higher beam intensity are required. Consequently, a major upgrade of the KEKB collider is foreseen until 2014, aiming at a final luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which is about 40 times higher than the previous peak value. This also implies changes to the Belle experiment and its innermost subdetector, the Silicon Vertex Detector (SVD), in particular. The SVD will be completely replaced, as it had already operated close to its limits in the past. All other subsystems will also be upgraded, leading to the new Belle II experiment.

The future SVD will, like the old one, consist of four layers of double-sided silicon strip detectors, but located at higher radii, as a new, two-layer DEPFET Pixel Detector (PXD) will be inserted around the beam pipe. Thus, the total sensitive area of the SVD will increase and, in order to mimimize the number of structural elements, it will be entirely composed of double-sided silicon detectors made from 6" wafers. The sensors will be read out by APV25 front-end chips that were originally developed for the CMS experiment at the LHC and that fulfill all the requirements of Belle II.

A large effort has been devoted to the minimization of the overall material budget. The so-called "Origami" chip-on-sensor concept was developed to obtain a good signal-to-noise ratio despite of the large sensors and fast shaping time, yet keeping the overall radiation length at a very low level thanks to light-weight composite materials for the mechanical structure and a highly efficient CO_2 cooling scheme. Multiple samples along the shaped waveform will be recorded by the APV25 chip such that the peak of the shaping curve can be reconstructed with high precision, allowing to discard off-time background hits and thus reducing the overall occupancy significantly, what leads to a better track matching efficiency.

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*Speaker.

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1. Introduction

The Belle experiment [1] is located at the KEK laboratory in Tsukuba (Japan). It is the only experiment at the KEKB collider, an asymmetric electron-positron machine operating mainly at the $\Upsilon(4S)$ resonance in order to provide a large number of B mesons.

From its commissioning in 1999 until it was shut down in summer 2010, the KEKB collider delivered a total logged luminosity of $1.04\,\mathrm{ab}^{-1}$ to the Belle experiment, corresponding to more than a billion $B\bar{B}$ pairs. This huge number enabled the detailed study of CP violation and of related phenomena, confirming the theoretical predictions of M. Kobayashi and T. Maskawa [2]. Consequently, Belle was explicitly mentioned – as well as its American counterpart BaBar [3] – in the announcement of the 2008 Nobel Prize in Physics awarded to the aforementioned Japanese physicists.

Despite the successful physics program of the Belle experiment, there are various rare processes in the B system which need to be studied with higher precision. Therefore, the KEKB collider is now undergoing an upgrade until 2014 in order to eventually achieve a luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at the future Belle II experiment, 40 times more than before.

The existing Belle detector was originally designed for a luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, only half the rate which was finally obtained. It is obvious that it cannot cope with a further 40-fold increase, or 80 times the design value. Consequently, not only the KEKB collider needs a major upgrade, but also the experiment, leading to Belle II [4]. The Silicon Vertex Detector (SVD), which was the innermost part of the Belle experiment, will be superseded by a two-layer Pixel Detector (PXD) in DEPFET technology [5], surrounded by a completely new Silicon Vertex Detector.

2. The Previous Silicon Vertex Detector

The second version of the Silicon Vertex Detector (SVD2) [6] of the finished Belle experiment was installed in 2003 and was in operation until the termination in 2010. It was the innermost subdetector of Belle, arranged in four concentric layers at radii of 2.0, 4.35, 7.0, and 8.8 cm from the beam axis. Similar to other detector sub-systems, the SVD2 covered polar angles between 17° and 150°, an asymmetry which reflects the forward boost arising from the fact that the electron beam has a higher energy than its positron counterpart. The silicon strip sensors were all double-sided and manufactured from 4" wafers.

Up to three sensors were concatenated and read out by the VA1TA chip [7], a derivative of the Viking family, with a peaking time of about 800 ns. Naturally, the occupancy (fraction of hit strips at any given time) scales with the shaping (or integration) time, such that this scheme renders rather high hit rates. In fact, the occupancy became one of the limits of the SVD2 towards the end of the Belle experiment, when the luminosity reached levels twice as high as the design value. The fraction of hit strips in the innermost layer, which naturally experienced the highest rates, exceeded 10%, what can be considered to be the limit for efficient track matching.

Moreover, the readout scheme and speed of the VA1TA presented a limit to the data taking. As the amplifier does not have a pipeline, but simply engages a sample/hold circuit when data are read out, it cannot measure during readout. This inevitably creates a dead time which is inversely

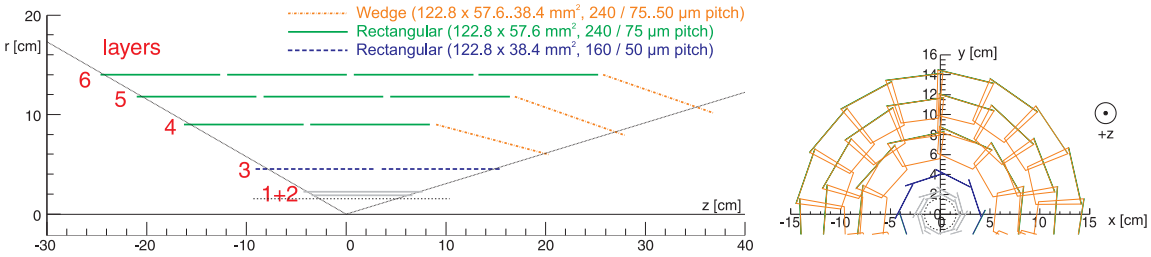

Figure 1: Layout of the Belle II Silicon Vertex Detector (SVD) including the two innermost pixel layers (gray). Drawings and dimensions only show the active areas of the sensors.

related to the readout speed. Toward the end of the experiment, this inefficiency was at the level of a few percent.

In order to overcome those limitations in view of a luminosity 40 times higher than in the past, the Belle II Silicon Vertex Detector requires

- fast shaping in order to keep the occupancy low,
- pipelined readout and a faster clock speed to avoid dead time.

This obviously implies a completely new readout system and thus a full redesign of the SVD.

3. The New Silicon Vertex Detector

The future Silicon Vertex Detector will, as the previous one, be composed of four layers of double-sided silicon strip detectors. However, they will be shifted towards higher radii, namely 3.8, 8.0, 11.5, and 14.0 cm. A new pixel detector, using the DEPFET technology [5], will be arranged in two layers around the beam pipe at radii of 1.4 and 2.2 cm. The pixel detector readout has a rather long effective integration period of 20 μs, but it obtains precise spatial data without ambiguities due to its individual pixel cell size of 50×50 and $50 \times 75\,\mu\text{m}^2$ for the two layers, respectively. In contrast, the silicon strip detector (SVD) provides very high temporal granularity of the order of 20 ns by a hit time reconstruction procedure described later, but it leaves spatial ambiguities due to ghost hits. Thus, it is essential to combine the data of PXD and SVD in order to take advantage of both systems.

The layout of the future PXD and SVD is shown in fig. 1. It has the same polar angle coverage as the previous experiment, from 17° to 150°, but the most forward sensor of the SVD in each of the outer three layers will be slanted (and thus trapezoidal). From the mechanical point of view, this arrangement is more complicated than a straight ladder, but is has obvious advantages: First of all, the precision is superior, because the particles created around the interaction point traverse the slanted sensors under a steeper angle, resulting in narrower clusters and thus in a better signal-to-noise ratio. Moreover, it also implies a lower effective material thickness for the benefit of less multiple scattering. Both arguments lead to an improved spatial (and impact parameter) resolution. Finally, using straight ladders would require an additional sensor in each layer, equipped with readout chips at the front-end, and requiring corresponding electronics in the back-end, what causes significant extra costs without benefit.

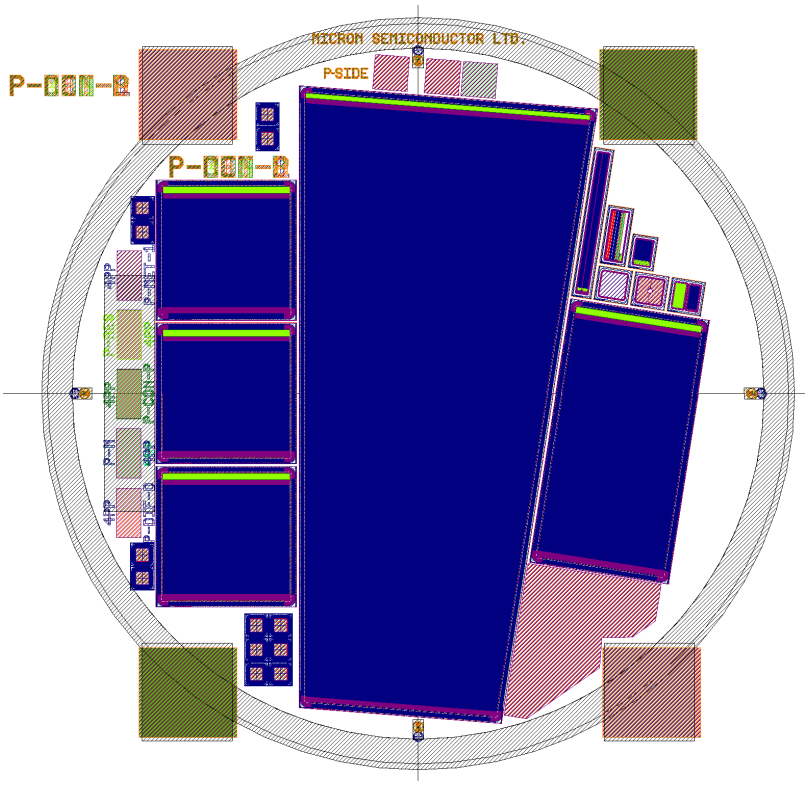

Figure 2: P-side wafer design of the slanted sensor (center) together with various baby sensors (left and right) and test structures (surrounding).

3.1 Double-Sided Silicon Sensors

In order to minimize the number of structural elements, all sensors are double-sided and made from 6" wafers. As indicated by different colors in fig. 1, there are only three different types of sensors, which all have the same length: two rectangular types (wide and small) and one trapezoidal type for the slanted parts.

Prototyping for the silicon sensors was started with two companies which can process 6" wafers to double-sided detectors: Hamamatsu Photonics (Japan) for the wide rectangular type and Micron Semiconductor (UK) for the trapezoidal type. To the latter, the complete wafer design was supplied by ourselves (fig. 2), so we had the opportunity to include baby sensors with various properties and smaller test structures on the wafer.

As these double-sided detectors are made from n-type bulk material, they need a p-stop strip insulation implant on the n-side in order to prevent a short circuit across all strips. There are different ways to design such implants, and three styles were implemented for the small square shaped baby sensors shown on the left side of fig. 2:

- common p-stop (one contiguous area surrounding all n-side strips);
- atoll p-stop (isolated circular lines surrounding individual strips);
- combined p-stop (a combination of both common and atoll types).

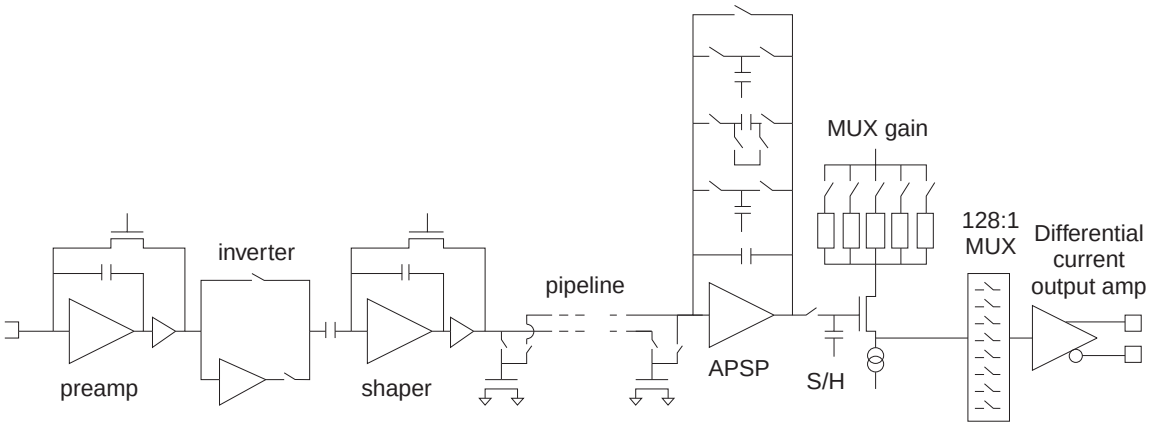

Figure 3: Building blocks of one of the 128 channels of the APV25 front-end readout chip.

Moreover, each of the baby sensors also features four variants of the actual geometry of the respective p-stop. Thus, there are twelve different p-stop patterns to be studied.

The baby sensors were tested in a high energy beam before and after irradiation with 700 kGy of ^{60}Co gammas [8]. The radiation led to a reduction in the signal-to-noise ratio depending on the actual type and pattern. In these tests, the atoll pattern with a specific geometry performed best before and after irradiation.

In total, there will be 187 silicon sensors arranged in 49 ladders. The overall active silicon area will be 1.24 m^2, almost twice as much as in the old SVD2 due to the increased radii of the four layers.

3.2 Front-End Electronics

The APV25 chip [9], originally developed for the CMS experiment at the LHC [10], was chosen for the Belle II SVD, because it has fast shaping and a pipelined readout, and it easily tolerates the expected total radiation dose of up to 100 kGy. Moreover, it is matured and well tested – about 70,000 such chips are in operation in the CMS Silicon Strip Tracker.

The APV25 is manufactured in an intrinsically radiation-tolerant 0.25 μm CMOS process which allows a maximum supply voltage of 2.5 V. Fig. 3 shows the core elements of one channel of the APV25. An optional inverter between preamplifier and shaper allows to select the polarity of the input signals, as the operating point of the shaper is not symmetric in order to make best use of the limited voltage range. The shaper output is sampled at the clock frequency and written into an analog pipeline of 192 cells, what enables the readout in parallel to accepting further triggers. Up to 32 cells can be labeled for pending readout in a FIFO, which implies that the usable pipeline is always at least 160 cells, or clock cycles, long.

Depending on the mode of operation, one, three or multiples of three consecutive samples are read from the pipeline upon reception of a trigger signal. The APV25 has a built-in "deconvolution" [11] processor (switched capacitor filter labeled "APSP" in fig. 3) which is used in CMS to narrow down the sensitive time window to a single bunch crossing. However, this feature requires clock-synchronous bunch crossings and thus cannot be used in Belle II because of its quasi-continuous beam. Nonetheless, the shaped waveform can be reconstructed from multiple samples

at a later stage in the back-end electronics. In order to allow some jitter of the trigger signal, the default mode of data recording in Belle II will be six samples, with the option to reduce this to three or even to one.

The APV25 is designed for the 40 MHz LHC clock, but is known to operate with similar performance in a wide range of clock frequencies. In general, there are two competing parameters related to the clock speed:

- trigger latency of 160 clock cycles at most (the slower the clock, the longer the latency),
- readout speed (the faster the clock, the lower the probability of a FIFO overflow condition due to pending data).

For practical reasons, two optional APV25 clock frequencies are foreseen in Belle II, which both are derived from the accelerator RF clock frequency: RF/16 = 31.8 MHz (default) or RF/12 = 42.4 MHz. The first case allows a trigger latency of about 5 μs, but also results in a certain dead time due to FIFO overflows at high trigger rates. With the default conditions (31.8 MHz clock, 6 samples) and at the expected maximum trigger rate of 30 kHz, detailed simulation [4] shows a dead time of 2.96% due to FIFO overflows. Increasing the clock speed to 42.4 MHz reduces the dead time to 0.51%, but also cuts down the maximum trigger latency to 3.8 μs. At default conditions, but with three samples instead of six read out for each event, the dead time disappears completely, but the hit time reconstruction may be impaired in case of inaccurate triggers. As the trigger precision is known online, we may consider a dynamic switching between three and six samples on an event-by-event basis in order to have all relevant information at a low dead time.

The full Belle II Silicon Vertex Detector needs 1902 APV25 chips with 128 inputs each, corresponding to a total number of 243,456 strips or readout channels. Each chip dissipates only about 0.35 W, which is small on the chip level, but adds up to a total power consumption of approximately 650 W in a rather small, confined space such that active cooling is mandatory.

3.3 Module Design

Due to its faster shaping, the APV25 has a higher noise slope than its slow predecessor, the VA1TA. Thus, a concatenation of strips across sensors as in the old SVD2 would result in an unacceptably poor signal-to-noise characteristics. In order to overcome this problem, it is necessary to

- read out each sensor individually (no concatenation),
- mount the APV25 chips as close as possible to the sensor strips.

At the same time, the overall amount of material must be kept low, as the Belle II experiment operates at relatively low energies where multiple scattering is a serious concern.

In order to fulfill those requirements together with active cooling on a double-sided silicon sensor, we developed a novel scheme which integrates sensors, mechanics, readout electronics and cooling: the “Origami” chip-on-sensor concept.

Depending on the layer, up to five sensors make up one ladder as shown in fig. 1. The structural elements of those ladders are two ribs made of a sandwich composed of an Airex [12] styrofoam

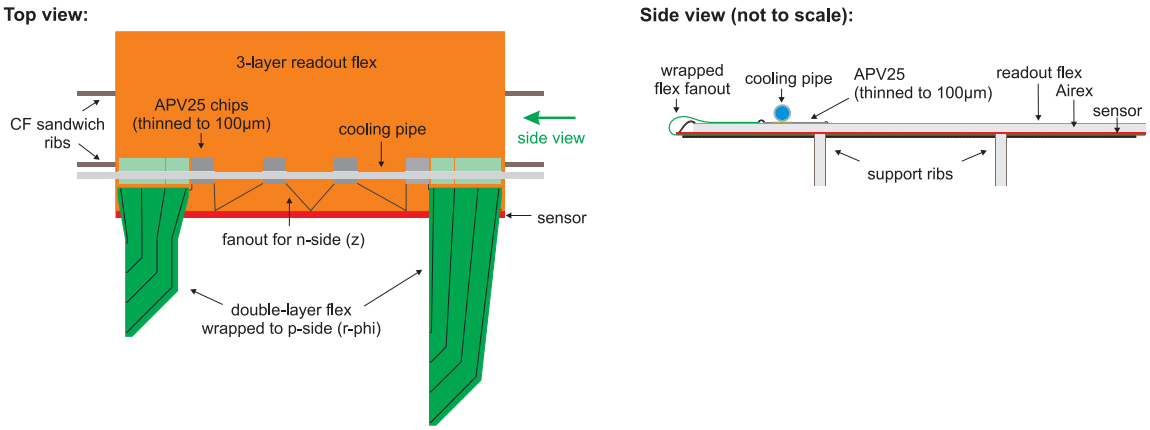

Figure 4: Top and side views of the Origami module scheme.

core with thin plies of carbon fiber laminated onto the sides. Such a composite is very light-weight, yet extremely stiff.

As sketched in fig. 4, the double-sided silicon sensors will be glued onto the ribs and read out with APV25 chips mounted on a flex circuit attached to the top of the sensors. This ensures short connections to the sensor strips and thus a high signal-to-noise ratio. In order to isolate the flex readout circuit from the sensor both electrically and thermally, a 1 mm sheet of Airex styrofoam is put in between. The connection of the sensor strips on the top side is obvious, while flex fanouts are attached to the strips on the bottom side and bent around the edge of the sensor in order to connect them to the APV25 chips on the top side. In this way, all chips can be aligned in a row and cooled by a single thin cooling pipe that serves the whole ladder. The APV25 chips used in the Origami module are thinned to 100 μm in order to reduce the material in the active volume.

Highly efficient CO_2 cooling will be used for the future SVD at a temperature of around -20° C, where some 20% of noise reduction is achieved compared to room temperature operation. Despite the operational pressure of approximately 20 bar, tiny stainless steel tubes with an inner diameter of 1.4 mm and a wall thickness of just 50 μm are sufficient and ensure good heat transfer.

The complete Origami ladder – including sensor, electronics, cooling and layers of glue – has an averaged effective thickness of 0.55% of radiation length, which is dominated by the silicon sensor contributing 0.32%.

Several full-size prototypes of Origami modules were already built. A photo of one such Origami module – before attaching the cooling pipe – is shown in fig. 5. The modules were tested both in the laboratory using a ^{90}Sr source and in a high energy beam. Typical cluster signal-to-noise values of 14 for the p-side readout (long strips with flex fanout wrapped around the edge) and 23 for the n-side (short strips on same side as the APV25 chips) were obtained at a temperature of -10° C.

On the ladder level, the sensors will be read out in the Origami scheme except for the ones at the very edges, which can be attached to hybrids located outside the acceptance at the side, using fanout flex circuits. Thereby, the total material in the active volume is further reduced without sacrificing the signal-to-noise performance. In total, about half of the readout chips are directly attached to the sensors using the Origami concept, while the other half is located at the edges

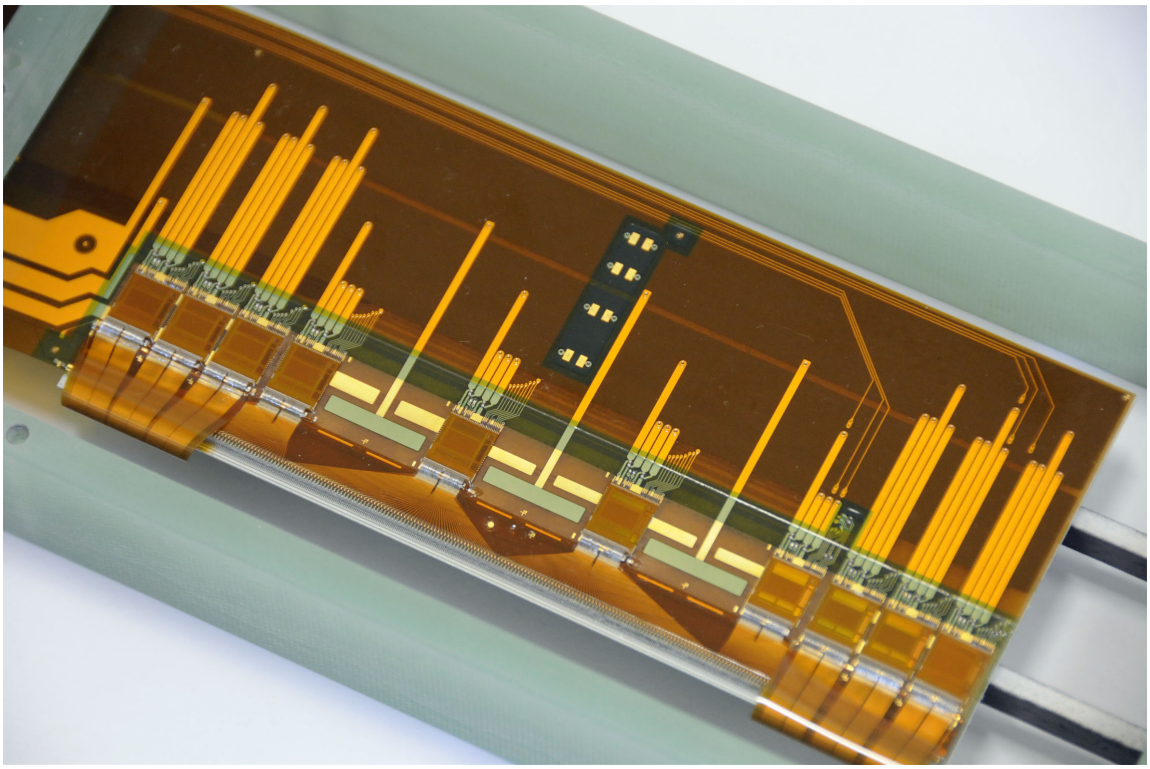

Figure 5: Top view of a functional full-size Origami module before attaching the cooling pipe.

outside of the acceptance region.

Fig. 6 shows a rendering of the fully installed Belle II Silicon Vertex Detector, where only the ladders of the outermost layer are visible. The APV25 chips of the Origami modules and the cooling pipe are clearly shown as well as the external readout Printed Circuit Boards (PCBs; green) at the edge of the slanted part. On the other end, the PCBs are mostly covered by the stacked Origami flex boards.

3.4 Back-End Electronics

In contrast to CMS, where the APV25 chips are coupled to the back-end electronics via optical links, copper cables are foreseen in the Belle II Silicon Vertex Detector [4]. Junction boxes will be placed at a distance of about 2 m from the front-end electronics, and the back-end 9U VME readout system will be about 10 m away. The signals can easily be driven over this distance by the APV25 chips without the need for any repeater or amplifier, which would raise concerns of radiation hardness. The only active part in the junction box close to the front-end (and thus in a moderately radiative environment) will be radiation resistant voltage regulators [13] which were originally developed for the ATLAS experiment at CERN.

The core of the VME back-end system will be a custom-built module called "FADC+PROC", indicating that it performs the digitization of the signals, but also processes them using high-end FPGAs. This processing involves various steps, starting with a digital Finite Impulse Response (FIR) filter [14] that compensates the frequency-dependent losses in the long cable as well as po-

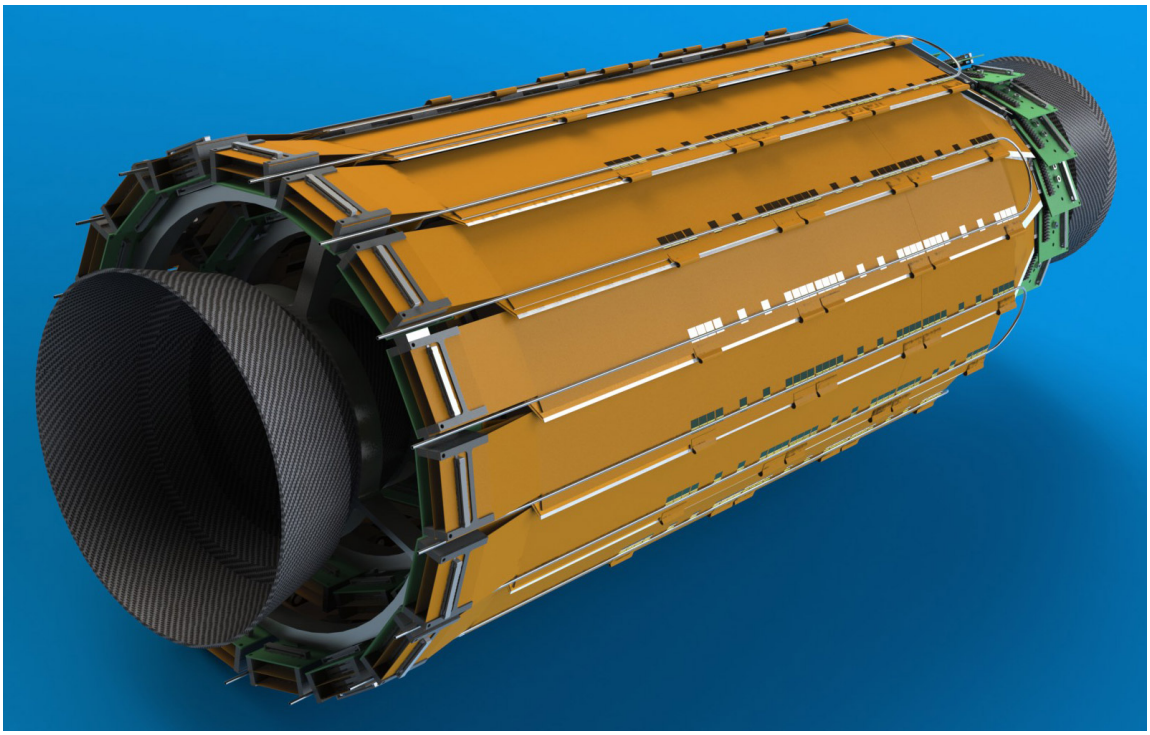

Figure 6: Drawing of the fully equipped SVD, revealing the Origami chip-on-sensor concept for the central sensors.

tential reflections. Then, the APV25 signals are extracted from the incoming data stream and treated with the usual procedure involving pedestal subtraction, a two-pass common mode correction and zero suppression (sparsification). When reading out three or six samples per event, the measured waveform will be compared with pre-loaded patterns using look-up tables in order to obtain the peak time and the amplitude. Finally, the reduced data are passed on to a transmitter board which is attached to the rear of the VME crate. This card distributes the SVD data to both the common readout platform of the DAQ system as well as to the pixel detector subsystem for online track matching and subsequent reduction of the pixel data. In total, about 80 FADC+PROC modules will be installed to read out the full SVD.

The hit time finding procedure, using multiple samples along the shaped waveform, was intensively studied in laboratory and beam tests. Using offline numerical fitting, a precision of 2 to 4 ns (RMS) was found, depending on the signal-to-noise ratio when comparing against a TDC reference [15]. Following the properties of a normal distribution, this implies that more than 99% of the hits belonging to the event under study can be collected within a time window of 20 ns, while outliers are most likely off-time background.

From our studies, it was evident that the essential information is basically contained within the three samples around the peak of the waveform, what eases the implementation of hit time finding in an FPGA using look-up tables. Simulations of such look-up tables in three different variants all showed that the results are sufficiently close to the numerically calculated values and thus allow online hit time reconstruction in real time. Together with the precise trigger timing, this enables the possibility of discarding off-time background hits on the fly, what might become necessary when

reaching full luminosity.

4. Summary

In the Belle II experiment, the Pixel Detector (PXD) and the surrounding Silicon Vertex Detector (SVD) will complement each other for vertexing: while the pixels deliver highly granular position information but only coarse timing, the strips return precise timing but potentially ambiguous spatial data – obviously, the data combination of both systems makes them extremely powerful together.

Despite some mechanical challenges, a slanted forward part was introduced in the three outer layers of the SVD in order to improve the data quality and, at the same time, to reduce the overall number of channels. Three different sensor designs are sufficient to equip the full SVD, and prototypes were successfully produced by two vendors. Various patterns for the n-side strip isolation of the double-sided silicon sensors were tested in a particle beam before and after their irradiation in order to optimize the sensor design. It was found that the atoll type isolation performs best both pre- and post-irradiation.

The Origami chip-on-sensor concept was developed to achieve a light-weight ladder construction with integrated readout electronics as well as CO_2 cooling, and at the same time to obtain a high signal-to-noise ratio. The complete ladder design accounts for only 0.55% of radiation length. Origami prototype modules were built and measured in a beam test, yielding cluster signal-to-noise ratios of 14 and 23 for p- and n-sides, respectively.

The APV25 chips will be operated in a mode where they deliver multiple samples along the shaped waveform for each event, what enables online hit time reconstruction in FPGA hardware. Together with precise trigger timing, this allows to discard off-time background hits. Numerical fitting of the sampled waveform revealed a precision of 2 to 4 ns, depending on the signal-to-noise ratio, and a detailed simulation confirmed that this process can be implemented in FPGA firmware using look-up tables.

References

[1] A.Abashian et al. (The Belle Collaboration), *The Belle Detector*, *Nucl. Instr. and Meth. A* **479** (2002) 117–232

[2] M.Kobayashi, T.Maskawa, *CP Violation In The Renormalizable Theory Of Weak Interaction*, *Prog. Theor. Phys.* **49** (1973) 652–657

[3] D.R.Marlow, *B-factory detectors*, *Nucl. Instr. and Meth. A* **478** (2002) 80–87

[4] Z.Doležal, S.Uno (editors), *Belle II Technical Design Report*, KEK Report 2010-1, `arXiv:1011.0352`

[5] S.Rummel, L.Andricek, *The DEPFET active pixel sensor for vertexing at ILC and Super KEKB*, *Nucl. Instr. and Meth. A* **623** (2010) 189–191

[6] H.Aihara et al., *Belle SVD2 vertex detector*, *Nucl. Instr. and Meth. A* **568** (2006) 269–273

[7] Gamma Medica – Ideas AS (Norway), `www.ideas.no`

[8] M.Valentan et al. *Optimization of Strip Isolation for Silicon Sensors*, *Physics Procedia*, in press

[9] M.French et al., *Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker*, *Nucl. Instr. and Meth. A* **466** (2001) 359–365

[10] The CMS Collaboration, *The CMS experiment at the CERN LHC*, *JINST* **3** S08004

[11] S.Gadomski et al., *The Deconvolution Method of Fast Pulse Shaping at Hadron Colliders*, *Nucl. Instr. and Meth. A* **320** (1992) 217–227

[12] Airex AG (Switzerland), `www.airexag.ch`

[13] RHFL4913A (previously LHC4913) by ST Microelectronics, `www.st.com`

[14] C.Irmler et al., *Efficient Signal Conditioning by an FIR Filter for Analog Signal Transmission over Long Lines*, *JINST*, in press

[15] C.Irmler et al., *Online data processing and hit time reconstruction for silicon detector readout*, *Nucl. Instr. and Meth. A* **617** (2010) 280–282