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The SuperB Silicon Vertex Tracker and 3D Vertical Integration

Valerio Re[1]

University of Bergamo and INFN, Sezione di Pavia
Department of Industrial Engineering, Viale Marconi 5, 24044 Dalmine (BG), Italy,
E-mail: valerio.re@unibg.it

The construction of the SuperB high luminosity collider was approved and funded by the Italian government in 2011. The performance specifications set by the target luminosity of this machine ($> 10^{36}$ cm^{-2} s^{-1}) ask for the development of a Silicon Vertex Tracker with high resolution, high tolerance to radiation and excellent capability of handling high data rates. This paper reviews the R&D activity that is being carried out for the SuperB SVT. Special emphasis is given to the option of exploiting 3D vertical integration to build advanced pixel sensors and readout electronics that are able to comply with SuperB vertexing requirements.

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1. Introduction

The SuperB project was approved in December 2010 by the Italian government and foresees the construction of a high luminosity (> 10^{36} cm^{-2} s^{-1}) asymmetric e^+e^- collider in the campus of the University of Rome "Tor Vergata". In the SuperB detector, the Silicon Vertex Tracker (SVT) is based on the BaBar vertex detector layout [1] with an additional innermost layer (Layer0) close to the interaction point, with a radius of about 1.5 cm. This Layer0 has to provide high position resolution (10-15 μm in both coordinates), low material budget (< 1% X_0), and tolerance to a high background rate (several tens of MHz/cm^2). Radiation hardness is also an issue, since the SVT will have to stand a total dose of ionizing radiation of about 3 Mrad/year and an equivalent neutron fluence (mainly due to electrons in the MeV energy range) of about 3.5 x 10^{12} n/cm^2/year. The baseline design of the SuperB SVT presently adopts the technically conservative solution of using short strip detectors (striplets) in the Layer0 [2]. However, the stringent experimental requirements stimulate an R&D program on low-mass pixel sensors, which is exploring CMOS MAPS (Monolithic Active Pixel Sensor) technology as well as 3D integration. The ambitious goal is to build a monolithic device with similar electronic functionalities as in hybrid pixel readout chips, such as pixel-level sparsification and time stamping.

This paper presents the status of the R&D activity that the VIPIX collaboration [3] is carrying out to achieve this goal by exploiting the potential of 3D integration. The effort is presently focused on the design of two different devices. The first one is a deep N-well active pixel sensor based on the interconnection of two layers fabricated in the same 130 nm CMOS technology. The second one is aimed at the ultimate goal of fabricating a 3D device based on heterogeneous technologies, i.e. a high resistivity sensor layer interconnected to a 2-tier CMOS readout integrated circuit. Both devices include a high performance readout architecture which is able to handle a very large data flow. The paper reviews the technical details concerning how these two different designs may fit the requirements of the SuperB SVT Layer0; the present status of VIPIX developments using 3D integration is also discussed.

2.Advanced pixel sensors for the SuperB SVT

With respect to the conservative baseline option of using short silicon strip detectors, the SuperB SVT Layer0 will obviously benefit from the higher granularity of a pixelated detector in terms of hit detection efficiency. An R&D program was started a few years ago, with the ultimate goal of proving the feasibility of a high resolution pixel detector system complying with the high background levels that Layer0 is expected to stand at the full luminosity operation of SuperB. Taking also into account the requirement of a low material budget, monolithic CMOS sensors can be considered as good candidates for this task. However, the standard readout architectures of MAPS are based on "rolling shutter" schemes that were devised for much lower hit rates with respect to the Layer0 specifications. Deep N-well (DNW) MAPS [4] have been the first effort in the direction of implementing advanced readout functionalities (as in hybrid pixel detectors) in a monolithic device. In DNW devices, the charge collecting

electrode is a deep N-well which is extended over a large fraction of the pixel area. This allows the pixel to use full CMOS analog and digital blocks, providing that the total area of the N-wells with PMOSFETs is small with respect to the DNW electrode. Exploiting the integration density of a 130 nm CMOS technology, it has been possible to design and test DNW MAPS with pixel-level analog processing, hit/no hit discrimination, sparsification and time stamping. The pixel size of these devices (50 x 50 μm^2) is compatible with the resolution specs of the Layer0. A continuous sparsified readout architecture was implemented in these devices, to make them compatible with the very short beam crossing time (the collision frequency is 233 MHz) and the very high background of SuperB.

Despite the successful test results on the first generation of DNW MAPS [5], R&D work is still needed to qualify these devices for a real experimental applications such as SuperB. There are several diverse issues that have to be tackled. Concerning the particle sensing properties, the beam test of the largest DNW device fabricated so far (APSEL4D) showed that the detection efficiency is limited to slightly more than 90% because of the PMOS N-wells inside the pixel. The nonnegligible amount of bulk displacement damage expected in the SVT Layer0 may impair the charge collection performance of the relatively low-resistivity, undepleted substrate of a standard CMOS technology [6]. The threat of interferences from full-swing logic signals running across the pixel matrix leads to operate the device at a digital supply voltage below the nominal value, which prevents to achieve the best speed performance from the digital readout. The readout architecture itself is based on macropixel cells (grouping 4x4 pixels). This macropixel structure was devised with the goal of minimizing the logic blocks inside a pixel, thereby reducing the area of PMOS N-wells. In a very high hit rate environment such as the Layer0, this may add inefficiency terms due to freezing the whole macropixel in the readout phase, and time-consuming scanning by the sparsification logic of non-fired columns in macropixels where a hit is detected.

3D integration may provide a very elegant solution to all these problems, with a technology leap which promises to overcome typical limitations of standard MAPS as well as of DNW MAPS [7]. First of all, most (if not all) PMOSFETs with their N-wells can be removed from the layer where the sensing electrode is located, improving the charge collection efficiency. Secondly, it appears possible to increase complexity and functionality in electronic readout circuits by exploiting the multilayer device structure. Both analog and digital pixel-level electronics can largely benefit from this. Moreover, 3D integration also opens up the possibility of using a high resistivity, fully-depleted bulk as the sensing region, with obvious advantages in terms of signal-to-noise ratio and radiation hardness. In the framework of a consortium between Fermilab, IN2P3 and INFN, the first step in the 3D direction has been the design of two-tier devices by the face-to-face bonding of two 130 nm CMOS wafers with the vertical integration process by Tezzaron Semiconductor [8]. In the following sections, the paper will review the two main 3D designs that are targeting a possible application in the SuperB Layer0, that is, a 3D DNW CMOS pixel sensor and a 3D CMOS chip for the readout of high resistivity pixel sensors.

3.Evolution of MAPS devices from 2D to 3D

The evolution of a DNW MAPS from a standard 2D CMOS process to a 3D technology is schematically shown by Figure 1. In the 3D device, the basic idea is to keep the DNW charge collecting electrode and the analog electronics section in the first layer, whereas the digital readout section is located in the second CMOS layer. The resulting 3D MAPS will be called "3D APSEL" in the following, since it is a direct evolution of the APSEL chips that were previously developed in a standard 2D CMOS process.

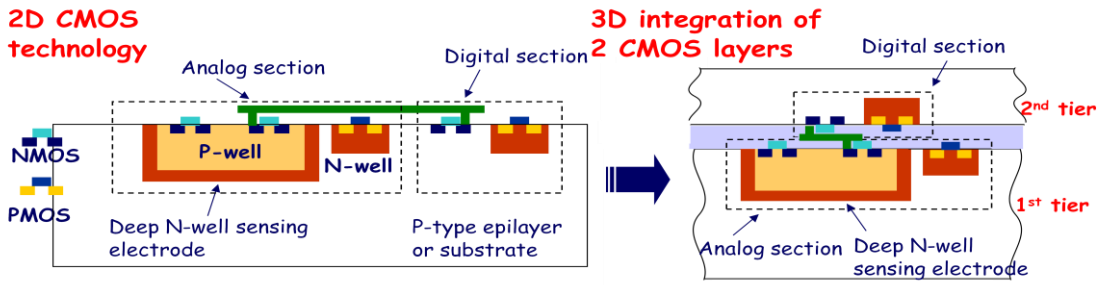

Figure 1. Concept for the evolution of DNW MAPS from a standard 2D CMOS process to a 3D vertical integration technology.

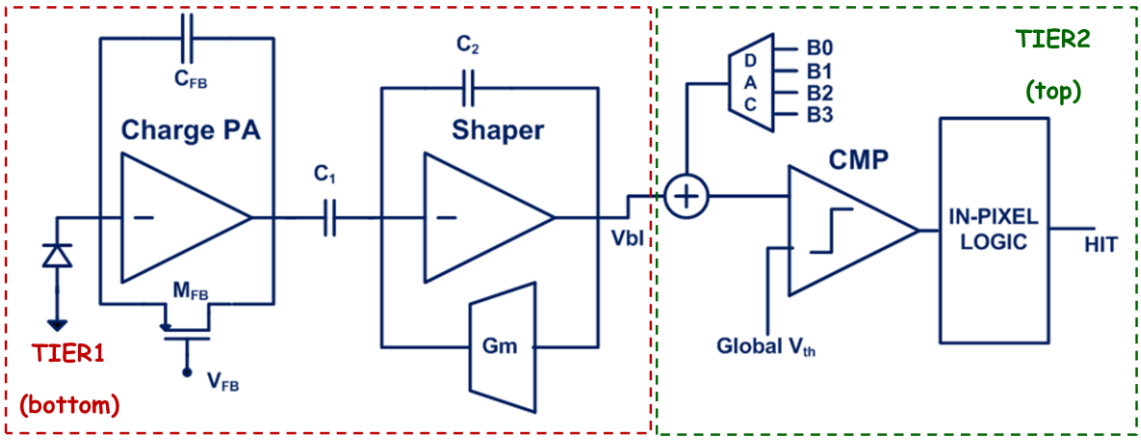

Figure 2. Circuit schematic of the pixel cell in a DNW MAPS designed in a 3D vertical integration technology.

In the 3D APSEL, there are obvious advantages associated with the fact that the analog front-end and the digital readout blocks are located in two different layers ("tiers"). Almost all PMOSFETs and their N-wells are removed from the tier with the DNW sensor, and it is reasonable to expect a drastic reduction of digital-to-analog interferences. There are also additional benefits that derive from the factor of two increase in the area that is available for electronic blocks inside a 50x50 μm^2 pixel. In some versions of 2D DNW MAPS [9], a "shaperless" front-end was devised with main goal of making room in the pixel cell for logic blocks and their interconnection to the chip periphery. In the 3D version, it is possible to include

a shaping stage in the analog processing chain, as shown by Fig. 2. This allows the designer to optimize independently noise and threshold dispersion [9] and to achieve a small gain dispersion, since it is no longer necessary to use a very small preamplifier feedback capacitor to attain an adequate charge sensitivity. For a further reduction of the threshold dispersion, a 4-bit digital-to-analog converter (DAC) can now be added in the second tier of the pixel cell for a local fine adjustment of the discriminator threshold voltage. Table 1 shows the main simulation parameters of this 3D MAPS cell.

The removal of layout constraints related to efficiency problems also has a beneficial impact on the digital readout architecture, adding more complex functionalities and increasing flexibility. In the 3D APSEL, the macropixel organization of the matrix is removed. The new sparsified readout architecture [10] performs time stamp latching at the pixel level (rather than in the periphery as it is done in 2D DNW MAPS), so that a time-ordered event readout is made possible. This is accomplished by including a time stamp comparator in the pixel cell, where the time stamp that is freezed in the cell when the pixel is hit is compared with a time stamp provided by the readout logic along a horizontal bus. Only pixels where the two time stamps are the same send a "data out" bit to the periphery, where their address is formatted and sent off-chip. This architecture can operate in a "data push" fashion, extracting all the hits from the matrix. A triggered mode can be also achieved in a straightforward way: in this case, when a trigger arrives, the chip sends out the hits within an appropriate interval of time stamps which occurred one trigger latency before.

VHDL simulations of this architecture demonstrate that in the data push mode a very high efficiency (> 99 %) can be achieved even at the background rate of 100 MHz/cm^2 that is expected (with a factor of five safety factor) in the SuperB Layer0. These results are relevant to time stamp clock periods ranging from 0.2 to 2 μs and to a 50 MHz read clock. The triggered mode has the advantages of drastically reducing the required bandwidth for the off-chip bus interconnection system. However, an efficiency loss is expected in dependence of the trigger latency, since in the present version each pixel can store only one hit. For example, at a 6 μs trigger latency (the presently expected value in SuperB), the simulated efficiency is about 98 %. The possibility of storing multiple hits associated to different time stamps is presently being investigated [10].

4.Design of a 3D CMOS readout chip for high resistivity pixel sensors

The design of a 3D CMOS chip (called Superpix1) for the readout of fully-depleted pixel sensors for the SuperB Layer0 follows similar guidelines as the 3D MAPS discussed in the previous section. The block diagram of the pixel-level electronics is the same as in Fig. 2. However, the internal circuit details of the preamplifier and the shaper are optimized in a different way, according to the different parameters of high-resistivity pixels with respect to CMOS sensors. Considering a fully-depleted detector thickness of 200 μm, the collected charge for a hit from a minimum ionizing particle is expected to be more of a factor of 10 larger than in a CMOS MAPS, where the actual sensing thickness is 15-20 μm at best. This allows the

designer to relax the specifications on noise, threshold dispersion, charge sensitivity and power dissipation, as it is apparent from Table 1.

	3D Apsel	**Superpix1**
Charge sensitivity	850 mV/fC	48 mV/fC
Peaking time	320 ns	260 ns
ENC	34 e rms	130 e rms
Threshold dispersion before/after correction	103/13 e	560/65 e
Analog power consumption	33 μW/pixel	10 μW/pixel
Detector capacitance	300 fF	150 fF
Matrix size	128x100	128x32
Pixel pitch	50 μm	50 μm

Table 1. Main simulated performance parameters for a 3D MAPS (3D APSEL) and a 3D CMOS chip (Superpix1) for the readout of high-resistivity pixel sensors.

The logic readout architecture for Superpix1 is also identical to the 3D APSEL one that was discussed in the previous section. Concerning the interconnection to a pixel sensor, it is worth mentioning that bump bonding was successfully performed between a 2D prototype of the CMOS chip (Superpix0) and FBK high resistivity sensors with the required 50 μm by 50 μm pitch [11]. The possibility of using more advanced, low-mass interconnection techniques is presently under study, following the development of 3D heterogeneous integration of layers in different technologies [12].

5.Next 3D submission status and future plans

The VIPIX group is getting ready for the submission of the two devices that were described in Sections 3 and 4. This multiproject wafer run will be handled by the integrated circuits brokers CMP, MOSIS and CMC. The deadline for this run is scheduled a few months after the delivery of 3D chips from a previous run in the same technology [13], where VIPIX submitted 3D MAPS prototypes with various architectures and pitches [14, 15]. The CMOS wafers with the two separate tiers of these CMOS sensors were delivered at the end of 2010. One of these wafer was diced before 3D bonding, and the resulting chips were successfully tested. In the layer with DNW sensing electrodes and analog front-end, response to both test signals and radioactive sources is very close to expectations, as well as the noise values [16]. The wafers from this submission were bonded by Tezzaron and one of the layers was thinned to expose Through-Silicon Vias and provide access to the two device tiers. Presently (August

2011) the first completed 3D wafers are being delivered by Tezzaron and finally, after wafer dicing, chip testing is expected to begin very soon. Fig. 3 shows the last steps of the 3D fabrication process, with thinning and backside deposition of metal for wire or bump bonding.

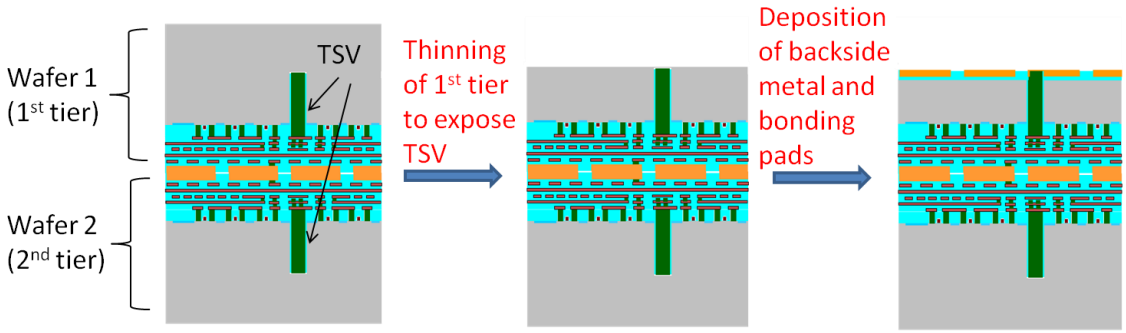

Figure 3. The last steps of 3D processing after wafer bonding by Tezzaron: wafer thinning and backside metal deposition.

The R&D on pixel sensors for the SuperB Layer0 will proceed to a technology choice in a couple of years from now, taking into account that an advanced pixelated system will be needed when the machine will operate at full luminosity, about two years from the first collisions expected in 2016. 3D integration may provide the solutions to the challenges of Layer0 in terms of both electronics and sensors. However, besides technical issues, an answer is expected from the 3D MPW runs about the possibility for the detector community of accessing this technology in a reliable and stable way. To this respect, it is worth mentioning that the community is also exploring alternative approaches to 3D integration with the support of the European AIDA project [17].

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