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# TCAD simulations of silicon strip and pixel sensor optimization

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Technology computer-aided design (TCAD), used in the semiconductor industry, simulates the semiconductor manufacturing process and the resulting device performance. We have used a device simulator to develop a highly radiation-tolerant n-in-p silicon strip and pixel sensors, both of which can operate at a very high voltage of up to 1000 V. We analyzed the electric field in the p-stop structures, novel punch-through-protection (PTP) structures, breakdown in the edge region, etc. and compared the analysis results with the measurement results of test structures; our findings contributed to the development of guiding principles for optimizing the critical structures. The TCAD device simulator is a valuable and effective tool as long as relevant semiconductor physics models and their parameters are implemented. We have yet to understand the modeling of the surface-bulk interplay after proton irradiation, the leakage current generation in the dicing edge, and other phenomena.

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## 1. Introduction

Computer-aided design (CAD) for semiconductor devices, referred to as technology CAD (TCAD), is an important tool for understanding the link between semiconductor physics and the electrical behavior of devices. The origin of the modern TCAD programs can be found in the work of Prof. Robert W. Dutton and his research group at Stanford University [1]. The programs consist of two different simulators: one for the semiconductor manufacturing process and the other for the device behavior. They are widely used in the semiconductor industry both to reduce the device development time and cost, and to understand the underlying physics (something that is often impossible to measure).

A brief history of TCAD programs over their 30 years of evolution is given in Table 1. Two major sources of this kind of program are Silvaco International [2] and Synopsys [3]. In Japan, a consortium of 10 semiconductor companies, called Selete [4], started development on a TCAD program for 2- and 3-dimensional (3D) geometries, HyENEXSS, in 1996.

**Table 1:** A brief history of major TCAD programs.

| Year | Institute | Process | Device |
|---|---|---|---|
| 1977 | R.W. Dutton, Stanford U. | SUPREM-I (1D) | PISCES |
| 1979 | Technology Modeling Associates (TMA)[1] | TSUPREM4 (2D) | MEDICI |
| 1989 | Silvaco International | ATHENA (2D) | ATLAS |
| 1989 | Integrated Systems Engineering AG (ISE)[2] | DIOS (2D) | DESSIS |
| 1992 | TMA | TAURUS (3D TSUPREM4/MEDICI) | |
| 1993 | M. Law, Florida U. | FLOOPS (3D) | – |
| 2002 | ISE[2] | FLOOPS (3D) | – |
| 2005 | Synopsys | SENTAURUS (3D TAURUS) | |

[1] TMA merged into AVANT! in 1998 and into Synopsys in 2001

[2] ISE merged into Synopsys in 2004

The process simulator simulates the semiconductor processing steps; such as oxidation, deposition, etching, ion implantation, and annealing; and generates inputs to the device simulator as realistically as possible based on the microscopic information. The program, however, is intended for use by experts who have access to the process and its parameters. The device simulator then calculates the macroscopic parameters by solving equations: the Poisson eq. of the electric potential $\psi(n,\ p)$, the current continuity equations of $J_n(\psi,\ n,\ p)$ and $J_p\ (\psi,\ n,\ p)$, and the drift diffusion and heat conduction equations as a function of $T_L$; where $n$ is the electron density, $p$ the hole density, and $T_L$ the lattice temperature. The device simulators incorporate semiconductor physics models for transport, mobility, generation-recombination (Shockley-Read-Hall (SRH), Auger, impact Ionization (II), trap, surface), etc., using default models and their parameters. The core of the calculation is the finite-element method that is the cutting-edge advantage of the TCAD.

3D simulation is usually very time consuming; whereas, 2D is reasonably accurate for most problems. In meshing the geometry for the finite-element analysis, the resolution and the computational time must be balanced. The process for finding the best procedures for mathematical methods, for physics models, and the convergence of calculation is usually trial and error. It should

be noted that the results are only relevant to the models in a given program. Although the semiconductor industry is trying to simulate systems as perfectly as possible, models for dicing edge, radiation-damaged surfaces, etc. are still missing.

We have been using a TCAD device simulator to optimize the structures both of silicon microstrips and pixel sensors (used for tracking charged particles in high-energy physics experiments). The goal of our research is to develop a highly radiation-tolerant n-in-p silicon planar sensor that can operate at very high bias-voltage , e.g., up to 1000 V. We have looked at the p-stop structures, punch-thru protection (PTP) structures, and edge structures, and compared the measurement of test structures to simulations. We used HyENEXSS5.5 to make a 2D device simulation.

## 2. P-stop structures between n-implants

The n-in-p silicon sensor, with n-type implants for readout in the p-bulk silicon, is a candidate for a highly radiation-tolerant silicon sensor with a low fabrication cost [5]. The built-in and radiation-induced positive charges in the interface of the silicon and the silicon oxides cause an inversion layer in the silicon that shorts the n-implants. In the n-in-p sensors, a p-type implantation in the silicon surface is used to isolate the n-implants. The p-implantation in a restricted region, the p-stop structure, which is separated from the n-implants, can minimize the electric field at the edge of the n-implants. The presence (and geometry) of the p-stop structures alters the electric field and may cause avalanche breakdown where the electric field exceeds the breakdown electric field, typically 30 V/$\mu$m in silicon. The breakdown most often starts at a location where crystal or structural defects exist and results in a sudden rise in leakage current that we will refer to as "microdischarge". The site at which the current flows becomes hot; infrared imaging can identify this hot spot. Observation of the problem and optimization of the p-stop structures were performed with a TCAD device simulator [6].

A number of miniature strip sensors with various p-stop structures were fabricated at sites #30-#57 and #77-#89 in wafter/batch#1 shown in ref. [7]. There were multiple lines of p-stops (1 p-stop (1p): common p-stop, 2 p-stops (2p): individual p-stop), with various pitches, p-stop widths, gaps between p-stops, and location of p-stops. Figure 1 shows a schematic of the strip section in which the 2p p-stop structure is shown; an aluminum probing metal senses the electric potential of the p-stop. Figures 2-4 show a comparison of the electric potential in the non-irradiated and TCAD simulated samples. The bias voltage applied (the full depletion voltage) was about 200 V (200 V) and 233 V (200 V) in the measured samples and the TCAD simulations, respectively. Figure 2 shows the potential as a function of the pitch, where the width of p-stop (6 $\mu$m) and the p-stop gap (4 $\mu$m) were fixed. Figure 3 shows the potential as a function of the "p-stop" width divided by the pitch, where the pitch was fixed to 75 $\mu$m and the "p-stop" width is the outer edge-to-edge width, i.e., including the p-stop gap in the case of 2p. Figure 4 shows the potential as a function of the asymmetry of the p-stop location defined by the abs((left n-p gap)-(right n-p gap)) divided by the pitch. In general, the TCAD simulation reproduces the measurement well, qualitatively. In most cases, the measured values were worse than the simulated ones by 10-20 V. Thus, we have verified the validity of the TCAD simulation of the electric field, with the provision that the real values could be slightly worse.

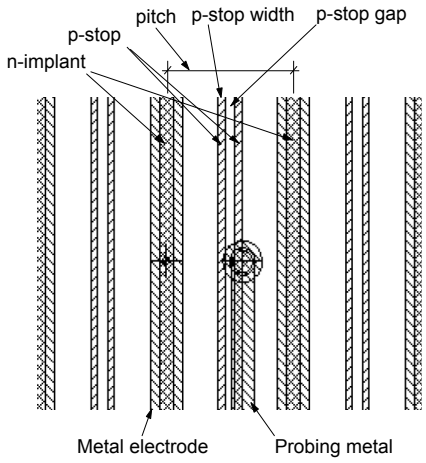



**Figure 1:** A section of a miniature strip sensor with individual p-stop structure (2p).

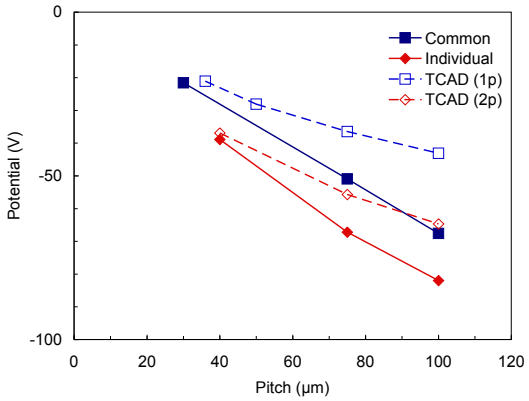



**Figure 2:** Pitch dependence of p-stop potential: common = 1p (square) and individual = 2p (diamond), measurement (solid) and simulation (dash).

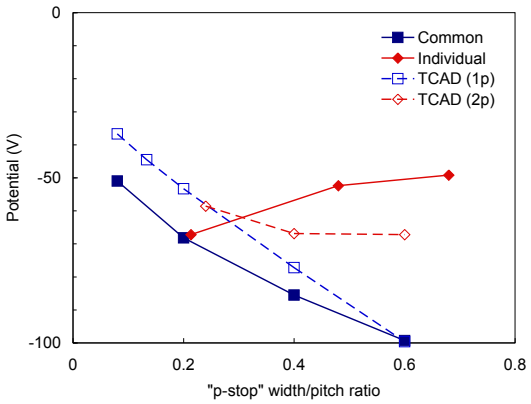



**Figure 3:** Width dependence of p-stop potential: common = 1p (square) and individual = 2p (diamond), measurement (solid) and simulation (dash).

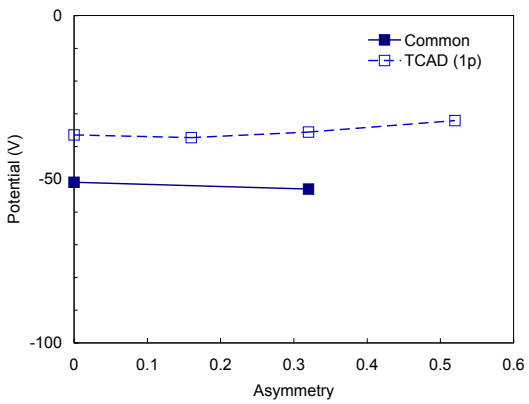



**Figure 4:** Asymmetry dependence of p-stop potential: common = 1p (square), measurement (solid) and simulation (dash).

## 3. Novel PTP structure

The AC coupling silicon microstrip sensor is made of integrated capacitors placed between n-implant electrodes and readout metals. The n-implants are connected to the ground potential of a high voltage power supply through a polysilicon resistor of approximately 1.5 MΩ [5]. In an accident in which a large number of charged particles pass through the silicon bulk, e.g., a beam splash, a large number of electron-hole pairs are generated and the current induced lowers the potential of the n-implant (that is, moves it toward the potential of the backplane of the sensor). To protect the AC coupling capacitors from the voltage drop, a protection mechanism, the punch-through protection (PTP) structure between the ground rail and the strip ends, can be considered to bypass the current once the voltage drop exceeds the punch-through onset voltage, thus keeping the voltage of the n-implant below the insulator breakdown voltage of about 150 V. For this protection, not only the onset but also the resistance at saturation and the saturation voltage are critical.

As the p-stop structure is a barrier for the punch-through (PT) function, we have proposed a novel PTP structure to lower the onset voltage, saturation resistance, and saturation voltage by introducing a "gate" from the bias ring (ground rail) [6]. Figure 5 shows an example of the PTP structure and an electric field distribution for the case of a PTP gap of 20 $\mu$m, a p-stop width of 6 $\mu$m with a surface concentration of $4\times10^{12}$ cm$^2$, an n-implant at 50 V, and a backplane at 200 V. The high electric field is generated at the right side of the p-stop toward the bias ring. Figure 6 shows the PTP current vs. voltage for the cases of without/with the gate, a narrow PTP gap of 12 $\mu$m of p-spray (no p-stop, but with a uniform surface p-concentration of $2\times10^2$), and a charge-up of $1\times10^{12}$ in the Si-SiO$_2$ interface positively. The onset voltage, the saturation resistance, and the voltage are reduced further as the cases progress in the sequence listed.

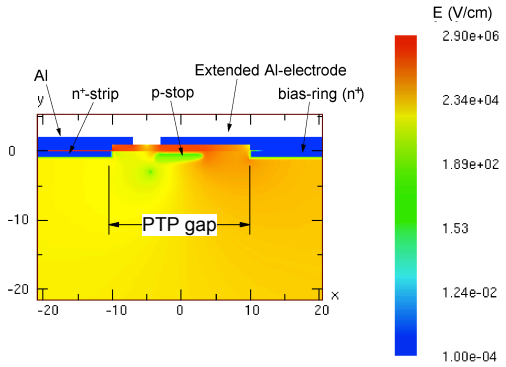



**Figure 5:** TCAD simulation of novel PTP structure of "gate over p-stop": n-implant at 50 V, bias ring at 0 V and backplane at 200 V.

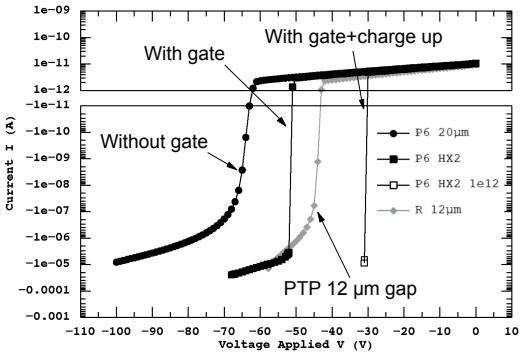



**Figure 6:** Simulated PTP behaviors (vertical axis is current).

The novel PTP structures were implemented on the miniature strip sensors at sites #58-#70 in wafter/batch#1 as shown in ref. [7]. Their schematics are given in Figure 7 and are classified as: BZ4, the miniature sensor type; B-D, "Atoll" type p-stop structures (B), "Compartment" type (C), and "Simple" type (D); 1-4 (for B-C) and 1-5 (for D) the gate type of "gate over p-stop" (1 (B-C), 2 (D)), "no gate" (2 (B-C), 3 (D)), "gate over p-stop #2" (3 (B-C), 4 (D)), and "gate full coverage" (4 (B-C), 5 (D)). BZ4D-1 is made for p-spray. These miniature sensors were irradiated with 70 MeV protons at CYRIC [8] to fluences of $5\times10^{12}$ to $1\times10^{16}$ 1-MeV neutron-equivalent particles ($n_{eq}$)/cm$^2$ [9].

Figure 8 shows the behavior of the novel PTP structures in non-irradiated samples, as measured at room temperature with a bias voltage of 200 V. The PT resistance is calculated as the PT voltage applied divided by the PT current measured. There are clear groupings in the behaviors of the structures: "no gate" (diamonds), "gate over p-stop" (triangles and circles), and "gate full coverage" (squares), where the onset voltage and the saturation resistance and voltage are reduced more in the progression of the grouping. The simple type with full coverage, BZ4D-5, seems to perform the best. In comparison with the simulation, the onset voltages measured are smaller than those simulated by approximately half.

Figure 9 shows the PTP behavior of the irradiated BZ4D-5 samples, measured at -20 °C with a bias voltage of 200 V. As the fluence increased, the onset voltage and saturation voltage increased, although there are minimal differences up to $1\times10^{13}$. The simulation in Figure 6 "With gate +

charge-up" reduces the onset voltage. The result of "no reduction of the PTP onset voltage" implies there is a larger effect caused by the radiation damage in the surface than the simple expectation that the radiation damage charges the Si-$SiO_2$ interface positively. As the PTP behavior reflects the electric field at the p-stop edge, the electric field at the p-stop edge after irradiation appears to be lower, which is also contrary to the simple expectation. The saturation resistance is about 20 kΩ, which was achieved at a PT voltage below 100 V and after irradiation at up to $1.2\times10^{15}$ $n_{eq}/cm^2$. The resistance is comparable to the n-implant resistance of 15 kΩ/cm, which then becomes the limiting factor if charge deposition occurs at the far side of the strips from the PTP structure [10] .

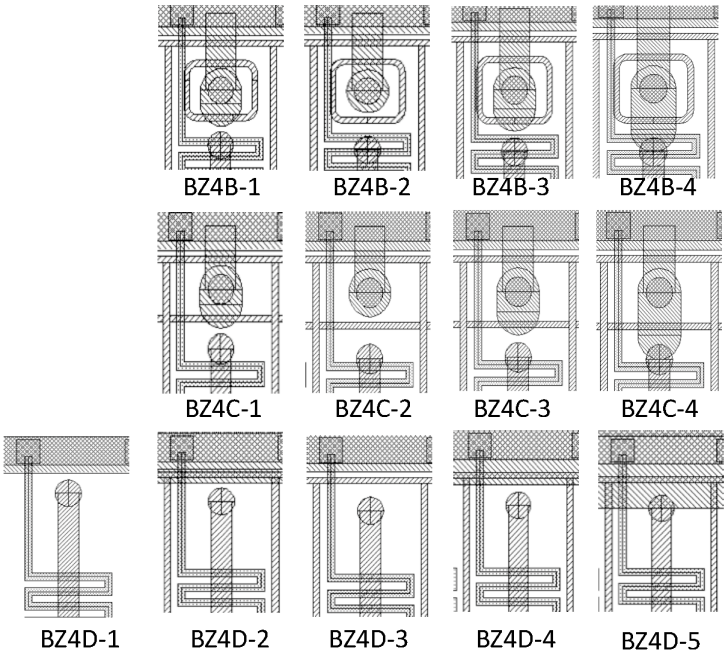



**Figure 7:** Novel PTP structures implemented in the Atoll (BZ4B), Compartment (BZ4C), and Simple (BZ4D) p-stop types.

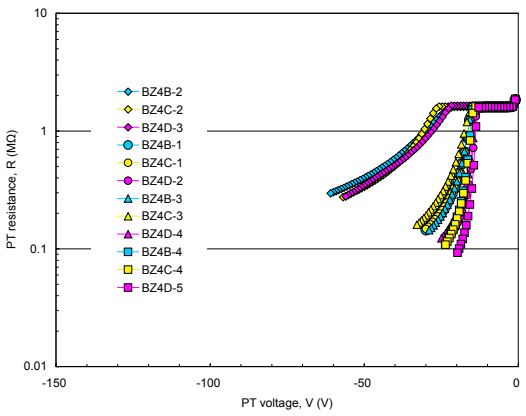



**Figure 8:** Behavior of novel PTP structures in non-irradiated samples.

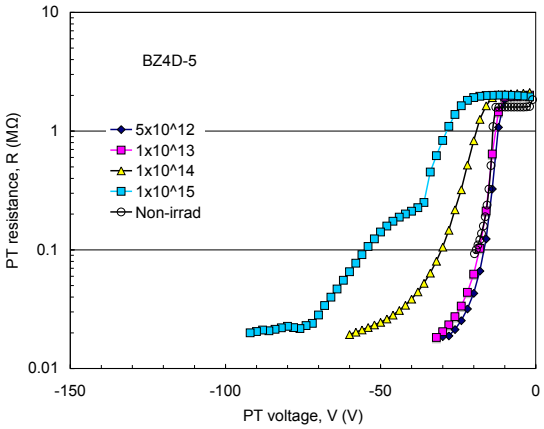



**Figure 9:** Behavior of novel PTP structure, BZ4D-5, after irradiations.

## 4. Protection against damage in the edge region

We have occasionally observed the onset of microdischarge after handling the sensors at a voltage (e.g., 500-600 V) much below the one we tested initially (1000 V). IR imaging revealed hot spots along the edge of the guard ring in the ATLAS07 main sensor, as shown in Figure 10. We should note that the hot spots are not on the edge of the bias ring, but in the guard ring. Protection against such post-processing damage is desired when designing the sensor.

An optimization to reduce the electric field at the guard ring to protect against microdischarge can be made by introducing another guard ring. A number of "multi-guard" diodes (4 mm square) were fabricated in batch/wafer #2 [7]. Figure 11 shows the schematics of the edge regions. The variation was made systematically such that the "field width" between the outer edge of the diode and the edge-implantation edge was the same (350 $\mu$m), where the "field width" is the surface region that has no implantation. The "width ($w$)" of the guard rings, from the inner edge of the inner-most ring to the outer edge of the outer-most one, was constant , e.g., $w$(1GR-M) = $w$(2GR-M), $w$(1GR-W) = $w$(2GR-W) = $w$(3GR-W). The TCAD simulation was modelled according to the geometry shown in Figure 12 using the typical parameters given in the table inset. A region of air (w3) is implemented to take into account the dicing edge at x3.

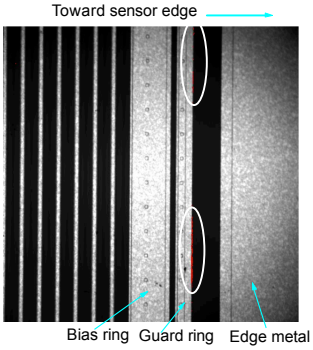



**Figure 10:** Hot spots observed in the edge region.

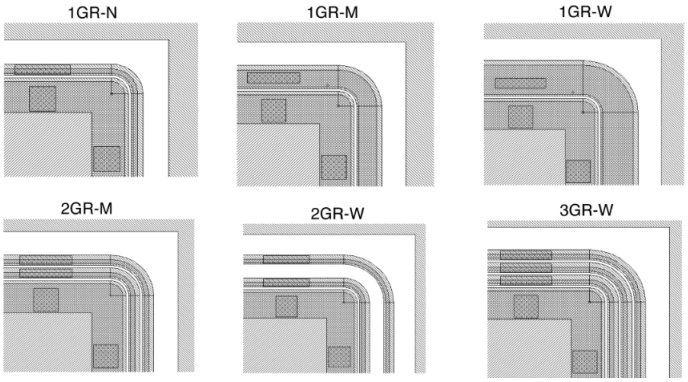
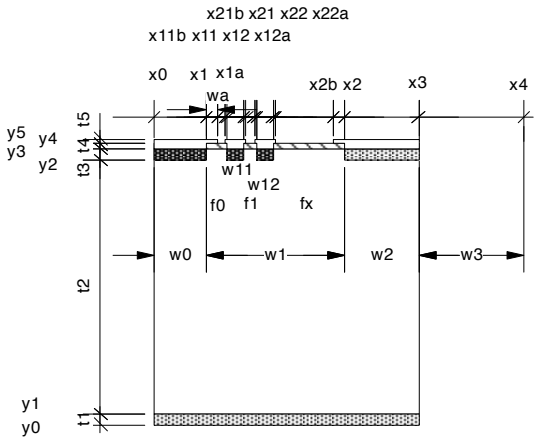



**Figure 11:** Schematic of edge region of multi-guard diodes.




| Case | w1 | w2 | f0 | f1 | f2 |
|---|---|---|---|---|---|
| 1 | 350 | 50 | 50 | 0 | 0 |
| 2 | 350 | 50 | 30 | 0 | 0 |
| 3 | 250 | 150 | 50 | 0 | 0 |
| 4 | 350 | 50 | 50 | 60 | 0 |
| 5 | 350 | 50 | 50 | 20 | 20 |

**Figure 12:** TCAD geometry of two guard ring layout and typical set of parameters.

Figures 13 and 14 show the simulation results for the electric field and the potential along the surface of the edge region at a depth of 1 $\mu$m with a bias voltage at 1000 V for the cases of one guard (Case 1) and two guards (Case 4), respectively. The results show that: (1) the existence of the guard implantation brings the potential along the surface less toward the backplane; (2) the highest electric field is at the diode (n-implant) edge; (3) the larger the number of guards, the lower the field at the diode edge, as a consequence of (1). Figure 15 shows the leakage current evolution as a function of bias voltage, where "1g30" is 1 guard with a gap f0 of 30 $\mu$m, "1g50" in Case 1, "2g50/60" in Case 2, and "3g50/20/20" in Case 5. The avalanche breakdown occurs when the bias voltage is larger than 1000 V, a point at which the electric field at the diode (n-implant) edge is over 30 V/$\mu$m. Narrowing the gap f0 reduced the electric field at the diode edge, thus allowing breakdown at a higher voltage. This, however, increased the electric field at the guard edge, which counteracted our optimization. We observed little degradation of leakage current while reducing the edge region (w1+w2). Thus, we find the TCAD we used to be incapable of modelling the generation of leakage current at the dicing edge.

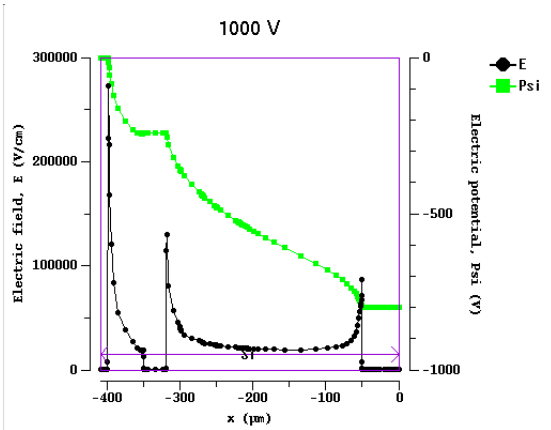



**Figure 13:** Electric field (circle, left axis) and potential (square, right axis) along the surface of the edge region: 1 guard (Case 1).

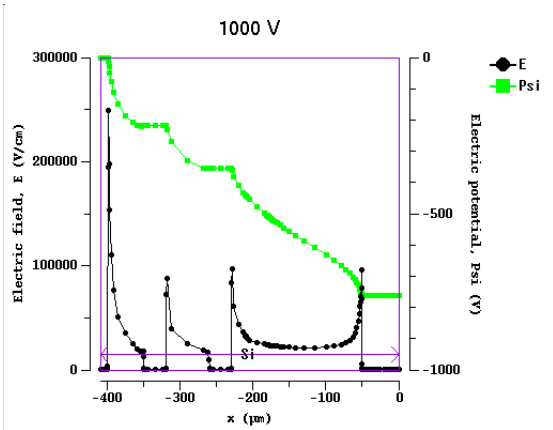



**Figure 14:** Electric field (circle, left axis) and potential (square, right axis) along the surface of the edge region: 2 guard (Case 4).

Figure 16 shows the measured values of the electric potential of the guard rings in the "multi-guard" diodes while applying a bias voltage of 1000 V. The result is consistent with the TCAD simulation. Figures 17 and 18 show the leakage current evolutions as a function of bias voltage of the non-irradiated and the irradiated samples, respectively, to a fluence of $1.1\times10^{14}$ $n_{eq}/cm^2$ of 70 MeV protons [9]. We observe in the non-irradiated samples: (1) that the breakdown voltage increases as the number of guard rings increases, although only a small increase is observed in the change from two guards to three guards; and (2) that the "width" of the guard rings has little effect on the breakdown. In the irradiated samples, we observe that (3) the breakdown occurs in an opposite way, i.e., one guard is the best and three guards is the worst. As yet, we have not found an explanation for the irradiated case using the TCAD simulation.

From the TCAD simulation and the measurement, we may derive a guiding principle for protection against damage in the edge region, i.e., one should reduce the electric field at the first guard ring by introducing a second guard ring at a reasonable distance such that the electric field at the

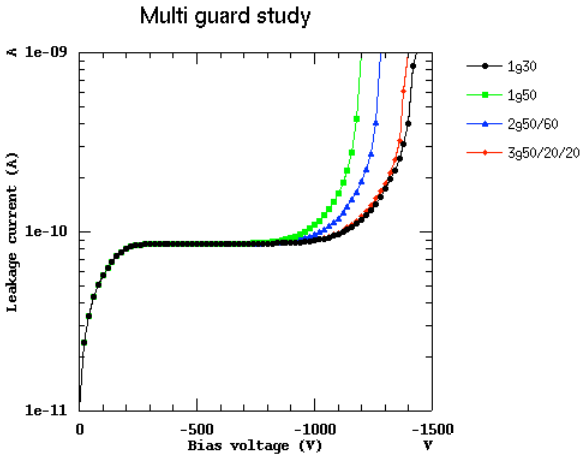



**Figure 15:** TCAD simulation of leakage current caused by avalanche breakdown.

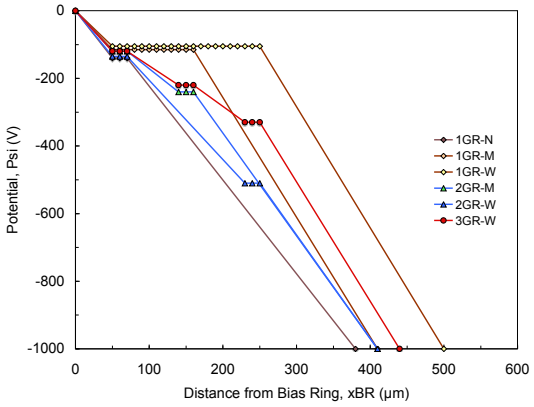



**Figure 16:** Measured electric potential of the guard rings.

second guard ring is minimized.

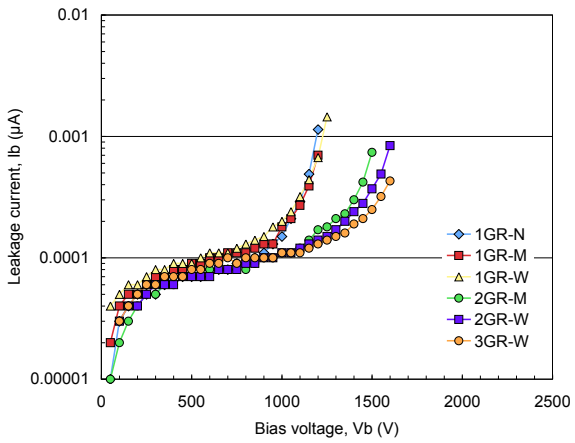



**Figure 17:** Leakage current behavior of multi-guard diodes before irradiation.

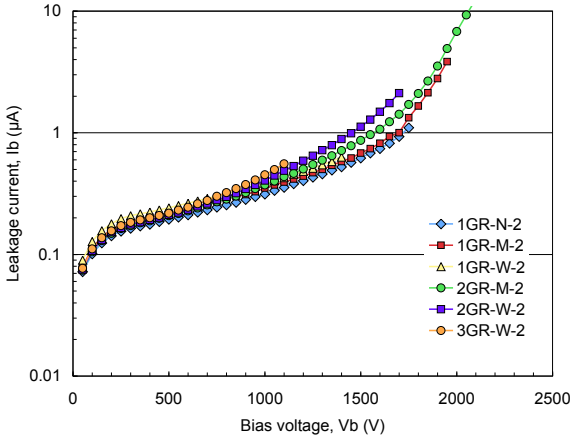



**Figure 18:** Leakage current behavior of multi-guard diodes after irradiation at $1.1\times10^{14}$ $n_{eq}/cm^2$.

## 5. Summary

TCAD for use in the semiconductor industry simulates the semiconductor manufacturing process and the resulting device performance. This technique is widely used to reduce the development time and cost and to allow better understanding of the underlying physics (something that is often impossible to measure). We have used a device simulator to develop an n-in-p silicon strip and pixel sensors that can operate at high voltages, up to 1000 V. Analysis of the electric field in the p-stop structures, novel PTP structures, breakdown in the edge region, etc., and comparisons with the measurement of test structures, have led to guiding principles for optimizing the critical structures. We have found that the TCAD device simulator is a valuable and effective tool, as long

as relevant semiconductor physics models and their parameters are implemented. In the highly radiation-tolerant silicon sensors we developed, we still have yet to accurately model either the surface-bulk interplay after proton irradiation (which is more complex than a simple charge-up in the Si-$SiO_2$ interface) or leakage current generation at the dicing edge.

## 6. Acknowledgements

We express our appreciation to the crew of CYRIC at the Tohoku University for the irradiation process, and to the detector development group at KEK for the use of their TCAD program. The research was partly supported by the Japan Grant-in-Aid for Scientific Research (A) (Grant no. 20244038), Research (C) (Grant no. 20540291), and Research on Priority Area (Grant no. 20025007).

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