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Latest developments in planar n-on-p sensors

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To further extend the ultimate physics reach of the experiments at the Large Hadron Collider (LHC), a series of accelerator and experimental upgrades are planned between 2014 and 2022. The final machine upgrade, called the High Luminosity-LHC (HL-LHC), is foreseen to increase the instantaneous luminosity by a factor ten with a targeted total integrated luminosity of 3000 fb^{-1}. To cope with the predicted high particle rates and intense radiation doses, n-in-p FZ planar technolgy has been developed with remarkable radiation tolerance. This technology might even be able to withstand the harsh environment at the innermost layers of the experimental upgrades for the HL-LHC.

This article summarizes the current understanding of the radiation tolerance of n-in-p FZ sensors. Plans and recent progress in prototyping silicon micro-strip and pixel devices at various foundries is shown. The different R&D efforts to reduce the inactive regions and to enhance the charge multiplication properties of such devices are also described.

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1. Introduction

The planned upgrades to the Large Hadron Collider accelerator complex (High Luminosity-LHC, HL-LHC) [1] provide many challenges to the silicon trackers of the experiments [2]. The factor of ten increase to the instantaneous luminosity requires much finer segmentation to retain efficient track finding. The targeted integrated luminosity of 3000 fb^{-1} over the ten year lifespan of the HL-LHC increases the needed radiation tolerance for the silicon sensors. The estimated end-of-lifetime fluence for the innermost layer of an experimental upgrade is approximately 2×10^{16} n_{eq} cm^{-2} [3], given in 1 MeV neutron equivalent particles per square centimeter (n_{eq} cm^{-2}). The need for much more radiation tolerant silicon sensors was foreseen, with the RD48 collaboration [4] and its successor (RD50 [5]) developing n-implant readout planar silicon sensors for the LHC experiments [6, 7, 8] and the HL-LHC experimental upgrades, respectively.

The current inner layers of the LHC experiments utilize segmented n-implant readout in n-bulk float zone technology (n-in-n FZ). Recent studies have changed focus to p-bulk FZ silicon (n-in-p FZ) as it has a number of advantages relative to n-in-n FZ technology: it always depletes from the segmented side; it is a single-sided production process with more foundries and more available capacity world-wide; it can be $\sim 50\%$ cheaper than n-in-n FZ devices; and it is easier to handle and test due to the lack of a patterned back-side implant.

This paper focuses on the development of planar n-in-p FZ sensor technology into experimental systems for the HL-LHC experimental upgrades. First, a short summary of the current understanding of the outstanding radiation tolerance of this technology will be given. Current and future prototype submissions of n-in-p FZ planar silicon devices to different foundries is presented. Finally, the R&D efforts to reduce the inactive regions and to enhance the charge multiplication properties of such devices are described.

2. Current Understanding of Performance After Irradiation

N-implant readout (n-in-n, n-in-p) was initially believed to be more radiation tolerant than the more standard p-in-n geometry due to the following: after irradiation, the dominant junction in the double junction field [9, 10] is located underneath the n-implant, which is also the location of the maxima of the weighting field; electron mobility is larger than hole mobility, which results in shorter collection times and bigger signals in regimes where charge trapping is significant; and the charge trapping constants for electrons are smaller than for holes [11, 12, 13, 14]. At lower fluences ($< 1 \times 10^{15}$ n_{eq} cm^{-15}), experimental measurements match simulations based on these assumptions and on the measured full depletion voltages [15].

At higher fluences, experimental measurements do not match the expectations from simulation. The collected charge of n-in-p FZ devices was shown to be much higher than expected, with a collected charge of over 8 ke^{-} measured after a fluence of 1×10^{16} n cm^{-2} at 1000 V [16]. Irradiated silicon devices using different bulk types (n-type and p-type doping) and growth techniques (floating zone and magnetic Czochralski) were studied. The collected charge for the different devices became very similar above 2×10^{15} n_{eq} cm^{-2} after reactor neutron [17] and 26 MeV/c proton irradiations [18], as shown in fig. 1. More than full charge collection efficiency was observed at large bias voltages in 300 μm thick n-in-p FZ devices irradiated up to 3×10^{15} n_{eq}/cm^{-2} [19].

Charge multiplication effects were then conclusively demonstrated in 100 μm and 150 μm thick high resistivity epitaxial diodes [20] and in 140 μm thick n-in-p FZ micro-strips [21]. Fig. 1 shows the collected charge as a function of voltage for 140 μm and 300 μm thick n-in-p FZ devices after irradiation with 26 MeV/c protons to a fluences of 5×10^{15} n_{eq} cm^{-2}; the collected charge is more than 2 times the expectations from minimum ionizing particle for the thinner device. These results imply that the electric field is much larger than previously expected over the entire volume of the devices (denoted active base) and that charge multiplication is enhancing the collected charge at these high fluences and large bias voltages.

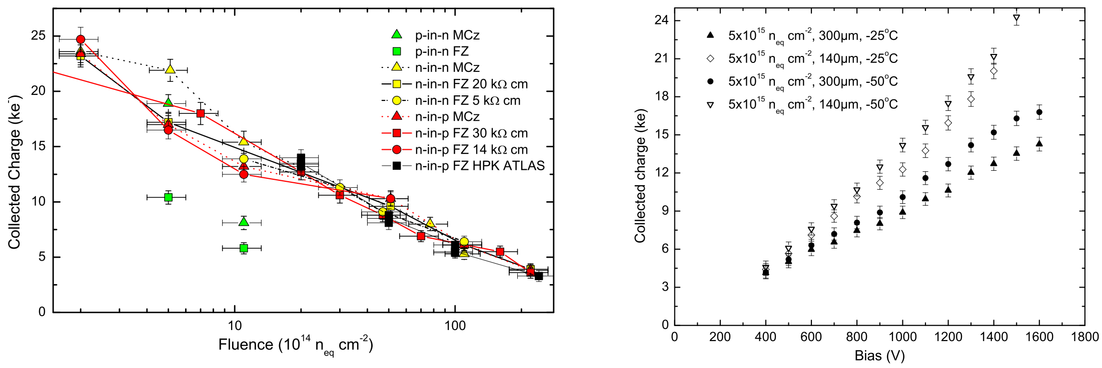


Figure 1: Left: The collected charge as a function of fluence after 26 MeV/c protons at a bias voltage of 900 V for different 300 μm thick substrate geometries [18]. Right: The collect charge as a function of bias voltage after irradiation with 26 MeV/c protons to a fluence of 5×10^{15} n_{eq} cm^{-2} for 140 μm and 300 μm thick n-in-p FZ micro-strip devices [21].

Edge-TCT measurements [22] show experimentally that both the active base and charge multiplication effects are presented; the effects determine the charge collection performance of planar silicon devices after 2×10^{15} n_{eq} cm^{-2}. In edge-TCT, a pulsed, narrow laser beam deposits charge at a known depth within a sensor. Fast electronics resolve the shape of the induced signal with sub-100 ps resolution. The left side of fig. 2 shows the drift velocity of charge carriers as a function of depth and bias voltage for a device irradiated to 5×10^{15} n cm^{-2}. The large drift velocities at all depths and bias voltages measured imply much larger fields throughout the device than would be expected from full depletion measurements. The right side of fig. 2 shows the induced current as a function of time and laser depth for the same device at a bias voltage of 750 V. The second peak in time is induced from holes produced by impact ionization of electrons near the n^+ implant. Additional edge-TCT measurements are needed to cover the full range of fluences, device thicknesses and implant geometries of interest for the HL-LHC in order to better determine the electric field configurations for simulation models.

3. Production Projects

This technology is rapidly becoming utilized with a large number of prototype n-in-p FZ devices already submitted or produced for pixel and strip upgrades of ATLAS, CMS, and LHCb. Table 1 gives an overview of these submissions; 8 different foundries are currently involved in planar n-in-p FZ productions, most for the HL-LHC upgrades. As shown in [16, 20, 21, 23], thinner

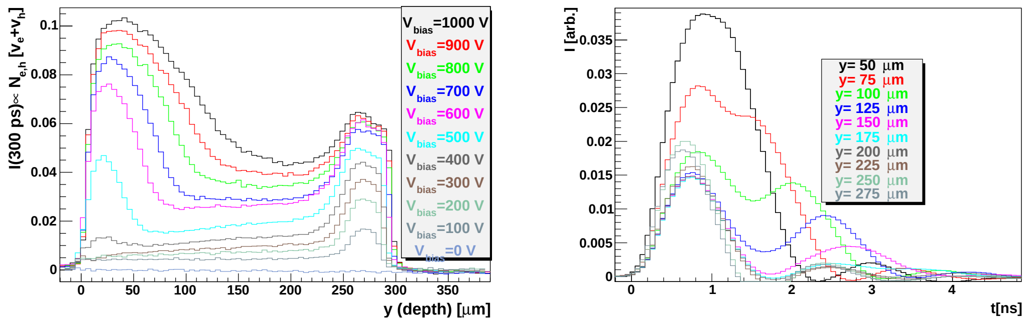


Figure 2: Left: The drift velocity of the charge carriers extracted from Edge-TCT measurements as a function of depth and applied bias voltage for a device irradiated to 5×10^{15} n cm^{-2}. Right: The induced current waveforms using Edge-TCT at different injection depth for a n-in-p FZ device with 750 bias irradiated to 5×10^{15} n cm^{-2} [22].

devices have larger collected charge at the high, end-of-lifetime fluences expected at the HL-LHC; therefore, many of these productions are studying multiple wafer thicknesses in order to optimize performance. Due to space-limitations, only a flavor of these production can be shown in next few sections of this proceeding.

Foundry	Wafer Sizes (Inch)	Thicknesses (μm)	Productions
CiS	4	150/200/285	ATLAS pixels, CMS pixels, RD50
IMB-CNM	4	150/300	ATLAS endcap strips, LHCb pixels, RD50
e2v	6	300	ATLAS barrel strips
FBK	4	200	ATLAS pixels
Hamamatsu	6	150/200/320	ATLAS pixels/strips, CMS pixels/strips, LHCb strips
Micron	4/6	150/300/500	ATLAS pixels, LHCb strips/pixels, RD50
MPP-HLL	6	75/150	ATLAS strips/pixels
VTT	6	100/200/300/500	ATLAS pixels, LHCb pixels

Table 1: Active n-in-p foundries with high-energy physics projects

3.1 LHCb Vertex Locator Sensors (Micron)

Currently, there is only one pair of n-in-p FZ sensors utilized at the LHC. The LHCb Vertex Locator (VELO) [8] predominately consists of modules with pairs of n-in-n FZ sensors (one R measuring, one phi measuring), produced by Micron Semiconductor, Ltd (United Kingdom). The module farthest from the rest of the experiment uses two n-in-p FZ sensors. As of now, the performance of the n-in-n and n-in-p FZ devices is identical [24], apart from the full depletion voltage as the n-in-p devices do not invert.

As the active elements of the VELO sensors are only 8 mm away from stable beams, an entire set of replacement modules is being produced using n-in-p FZ sensors. The p-type devices cost 30% less than the original n-type devices, even with the use of routing double-metal on the segmented n-implant side. The production has progressed well with half of the modules already delivered to CERN. The remainder of the modules are expected to be deliverd by autumn.

3.2 ATLAS Upgrade Strips Sensors (Hamamatsu)

For the strip regions of the planned all-silicon HL-LHC tracker for ATLAS [25], planar n-in-p FZ devices have already been chosen to be the baseline technology. In collaboration of Hamamatsu Photonics K. K. (Japan), ATLAS has developed 9.75×9.75 cm^2 sensors suitable for the short strip regions of the barrel, which use the maximal area of 6 inch silicon wafers. The devices, denoted ATLAS07 [26], are 310 μm thick, and are divided into four 2.39 cm long segments (2 axial and 2 stereo with a 40 mrad angle) with the 1280 strips each. 24 miniature (1×1 cm^2) micro-strip devices surrounding the main sensor have been utilized to study of the evolution of the silicon properties with irradiation. The full-size ATLAS07 sensors have been throughly evaluated within the collaboration [27] with all bulk and surface properties within the technical specifications prior to irradiation.

An extensive program of ATLAS07 miniature sensors irradiations has been undertaken with reactor neutrons from the TRIGA reactor in Ljubljana, Slovenia [28], charged pions from the PiE-1 beamline of the proton accelerator at the Paul Scherrer Institut in Villigen, Switzerland [29] and protons from the Compact Cyclotron at Karlsruhe, Germany [30] and from the the Cyclotron Radio Isotope Centre (CYRIC) at Tohoku University, Japan [31]. The evolution of the sensor properties as a function of particle fluence due to bulk (depletion voltage, leakage current, and collected charge) [32] and surface damage effects (interstrip resistance, interstrip capacitance and punch-through protection voltage) [33, 34] has been measured.

Fig. 3 shows new results after pion irradiations and summary of all charge collection measurements made with ATLAS07 miniature sensors at 900 V as a function of fluence. For devices that were temperature annealed, the collected charge is corrected back to a pre-annealed state using factors derived from [35]. The collected charge for all irradiation sources after the NIEL corrections are consistent within the uncertainties on the fluence and collected charge. The measured values are also consistent with previous measurements of irradiated Micron devices to the same fluences.

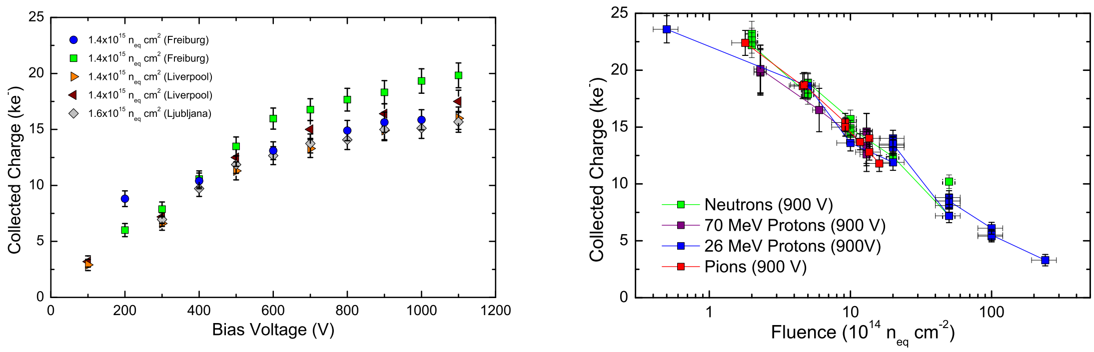
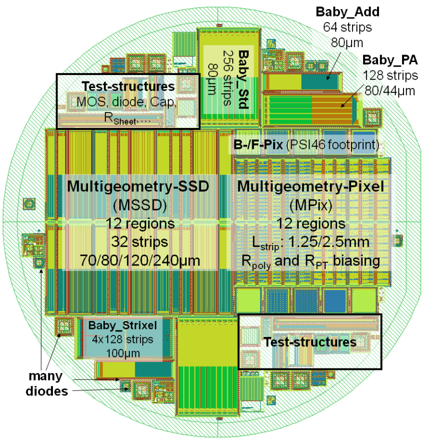


Figure 3: Left: Collected charge of ATLAS07 micro-strip sensors produced by Hamamatsu as a function of bias voltage after 280 MeV pion irradiation and annealing the devices for 80 minutes at 60C°. Right: Summary of collected charge of the ATLAS07 devices as a function of 1 MeV n_{eq} fluences for the different irradiation sources studied at a bias voltage of 900 V. The measurements are performed without temperature annealing or corrected back to an pre-annealing state.

3.3 CMS Upgrade Joint Strip-Pixel Sensors (Hamamatsu)

The CMS collaboration is undertaking an extensive program [36] of sensor studies of devices produced by Hamamatsu. As shown in fig. 4, the 6 inch mask includes diodes, miniature strip and pixel structures with different geometries, and double-metal and Lorentz angle test structure. Float zone, magnetic Czochralski and epitaxially grown bulk materials in both n-in-p and p-in-n geometries will be studied in multiple thicknesses. For the n-in-p devices, the project is also investigating both p-spray and p-stop strip isolation techniques. The devices will be characterized prior to and after mixed particle type irradiations, with both surface and bulk properties evaluated. As the devices will be produced by one vendor and will be tested using an uniform protocol, it is hoped that most systematic uncertainties in the comparison of the different materials and thicknesses will be reduced to a minimum. In total, 158 wafers will be produced at a cost of 200 kCHF with ~ 30 structures per wafer to be evaluated.



bulk-type	thickness (μm)	n-type (p-stop)	p-type (p-spray)	p-type
FZ	320	6	6	6
FZ deep diff.	200	6	6	6
FZ deep diff.	120	6	6	6
MCz	200	6	6	6
Epi	100	2	6	6
Epi	70	4		
Epi	50	6	6	6
FZ deep diff. & double metal	200	6	6	6
FZ	200	6	6	4
FZ on carrier	120	6	6	4

Figure 4: Left: The mask layout of the CMS joint strip-pixel sensor submission with Hamamatsu Photonics, Ltd. Right: Table of number of wafers, substrate bulk type and substrate thicknesses included in the CMS joint strip-pixel sensor production.

3.4 ATLAS Upgrade Strips Sensors (e2v)

In order to qualify another large-volume silicon vendor for the strip region of the HL-LHC upgrade, ATLAS has been producing 300 μm planar n-in-p FZ sensors on 6 inch wafers with e2v Technologies, plc (United Kingdom). The first submission consisted entirely of miniature sensors (1×1 cm^2), which were used to determine the optimal strip isolation and passivation techniques. The preliminary results are encouraging; a set of parameters have been found which yields acceptable performance prior to irradiation with a collected charge after 24 GeV proton irradiation [37] consistent with previous measurements, see fig. 5. Axial-only, full-size (9.75×9.75 cm^2) sensors in the ATLAS short strip geometry are currently under production which will be compatible with both the 128 channel, 0.25 μm CMOS readout ASIC (ABCN25) and the final 256 channel, 130 nm CMOS readout ASIC (ABCN13).

3.5 RD50-CMS-ATLAS Upgrade Pixels Sensors (CiS)

One concern with using n-in-p FZ devices with hybrid-pixels is the large potential difference between the sensor's edges and the readout ASIC, which could cause electrical discharges that damage the pixel package. In order to address this concern, a joint ATLAS-CMS pixel production

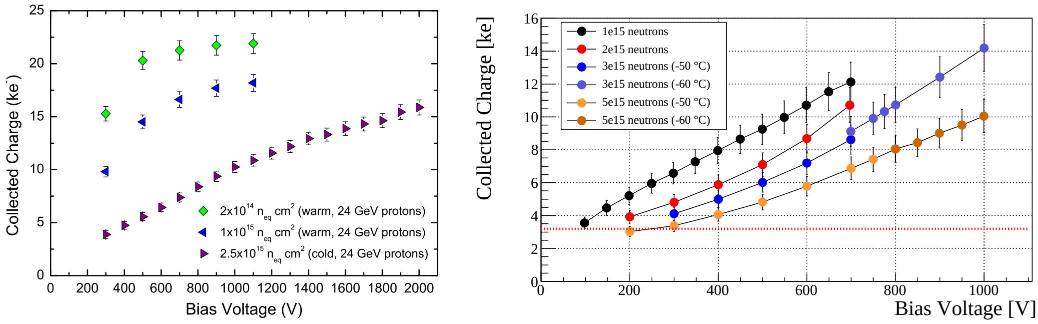


Figure 5: Left: Collected charge as a function of bias voltage for e2v micro-strip devices irradiated with 24 GeV/c protons. Right: Charge collection as a function of bias voltage for 285 μm thick, ATLAS FE-I3 pixel devices produced by CiS [38]. The sensor surface is covered in 3 μm of BCB at IZM Berlin in order to improve the strip edge isolation.

has been undertaken within the RD50 collaboration with CiS Institut für Mikrosensorik and IZM-Berlin [38]. 285 μm thick sensors compatible with the ATLAS FE-I3 and CMS ROC pixel ASICs are produced by CiS, and then the sensor surface is covered with 3 μm of Benzocyclobutene (BCB) by IZM Berlin. The BCB layer increases the isolation between the sensor's edges and the front end ASICs. A number of FE-I3 pixel packages have been bump bonded by IZM-Berlin and then irradiated with reactor neutrons [28]. The BCB post-processing has been successful, with 1000 V bias applied for several hours before and after irradiation with no sign of breakdown. As shown in fig. 5, the collected charge after irradiation using the FE-I3 pixel ASIC is consistent with previous n-in-p FZ micro-strip measurements.

CiS is also producing another pixel sensor wafer for ATLAS. Both 1- and 2-chip devices compatible with the new FE-I4 readout ASIC are included. The FE-I4 is planned to be used in the Insertable B-Layer (IBL) upgrade in 2014 and the outer pixel upgrade in 2021. The sensors will be produced in three thicknesses (150, 200, and 300 μm) without a handle wafer. The devices will be used to study the effects of thickness on collected charge, and on the sensor and bump bonding yields.

3.6 ATLAS Upgrade Pixel Sensors (Micron)

There are a number of difficulties testing irradiated hybrid pixel packages: bump bonding of a small number of prototypes is expensive and it is difficult to disentangle the irradiation effects of the sensor and readout ASIC. In order to answer both of these issues, a pixel sensor wafer has been designed by ATLAS and produced by Micron. The 6 inch wafers contain standard pixel devices which match to ATLAS FE-I3, CMS PSI-46 and Medipix readout ASICs as well as a set of bondable pixels. For the bondable devices, 8 interleaved pixel sets are connected together using a double-metal layer which ends in a wire-bondable pad. These devices can be irradiated separately from any electronics and then wire bonded to LHC-speed, analogue readout ASICs with minimal heating. The first tests [39] of these devices after neutron irradiations were successful with the collected charge consistent with previous measurements of micro-strip devices.

A second set of 6 inch pixel wafers have also been produced by Micron for ATLAS in 140 and 300 μm thicknesses without a handle wafer. This wafer consists of a large number of 1- and

2-FE-I4 compatible sensors. The devices are now at IZM for under-bump metalization and bump bonding to FE-I4s.

3.7 ATLAS Upgrade Thin Strip-Pixel Sensors (MPP-HLL)

Max-Planck-Institut für Physik and MPI Halbleiterlabor have undertaken a joint project (MPP-HLL) to make thin (75 and 150 150 μm) micro-strip and pixel sensors compatible with the ATLAS FE-I3 pixel chip using a handle wafer. The handle wafer can then be selectively etched to act as a thin support frame and to increase stiffness with minimal material. These produced devices had an excellent 99% yield, low bias currents ($\sim$ 10nA/cm^2) and good breakdown behaviour. Three micro-strip devices of each thickness were irradiated with 26 MeV/c protons to fluences up to 1×10^{16} n$_{eq}$ cm^{-2}. As shown in fig. 6, the devices performed extremely well with full charge collection efficiency still possible for the thinner devices for all the fluences studied. [40].

3.8 ATLAS Upgrade Thin Pixel Sensors (Hamamatsu)

Finally, ATLAS is also producing thin n-in-p FZ pixel sensors [41] with Hamamatsu. The 6 inch wafers contain 1- and 4-chip FE-I3 compatible devices and 1- and 2-chip FE-I4 compatible devices. The front of the wafers are patterned on 320 μm thick wafers; after finishing the front, the wafers are thinned to 150 μm and then the backside is completed. As shown in fig. 6, the I-V performance of these devices before irradiation is remarkable with the first signs of breakdown above 900 V. A number of FE-I4 devices are at IZM ready for bump bonding.

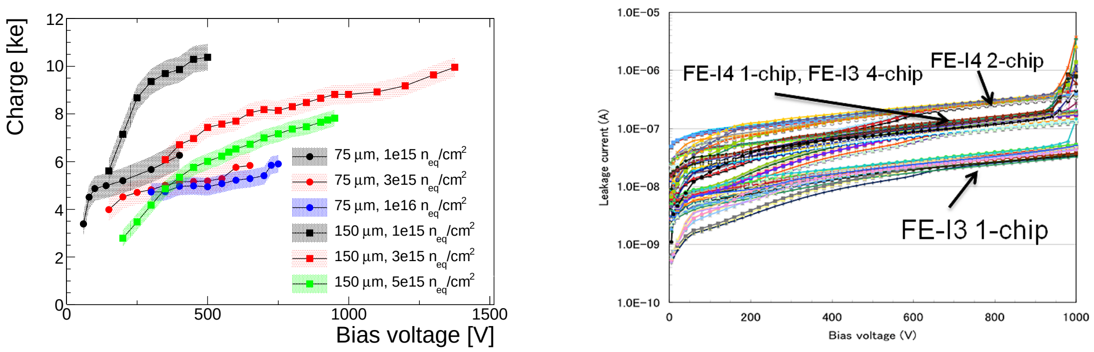


Figure 6: Left: Charge collection of MPP-HLL strip devices as a function of voltage after irradiation with 26 MeV/c protons [40]. Right: Leakage current vs. bias voltage for 140 μm thick pixel devices produced by Hamamatsu. The differences in the leakage current scaled with the areas of the different device types.

4. Research and Development Studies

In addition to wafer productions intended for HL-LHC experimental upgrade prototyping, an active program of device R&D is in progress on two main fronts: edge reduction and charge multiplication enhancement. Tiling of pixel detectors edge-to-edge is attractive in order to reduce material in overlapping devices; tiling puts a premium on reducing the inactive sensor edges as particles crossing these areas would not be detected in that particular layer of the system. Charge multiplication is now understood to be an important element to the radiation tolerance of planar silicon sensors; as such, efforts have begun to try to understand how device geometry influence charge multiplication properties in an attempt to make more radiation tolerant devices.

4.1 Edge Reduction

As part of the production of ATLAS pixel devices with Hamamatsu, special 'slim-edge' diodes were fabricated. These diodes have 3 edges with the standard Hamamatsu diode layout and the last edge being narrowed. As shown in fig. 7, a linear relationship between the total edge width and the square root of the breakdown onset voltage is measured [41]. Because of the square root dependence of the onset voltage, it is believe the onset of breakdown is caused by lateral depletion along the surface of the sensor reaching the device's cut edge. After irradiation, the onset voltage increases. With the results of this study, the minimal edge size needed for a given use-case can be estimated.

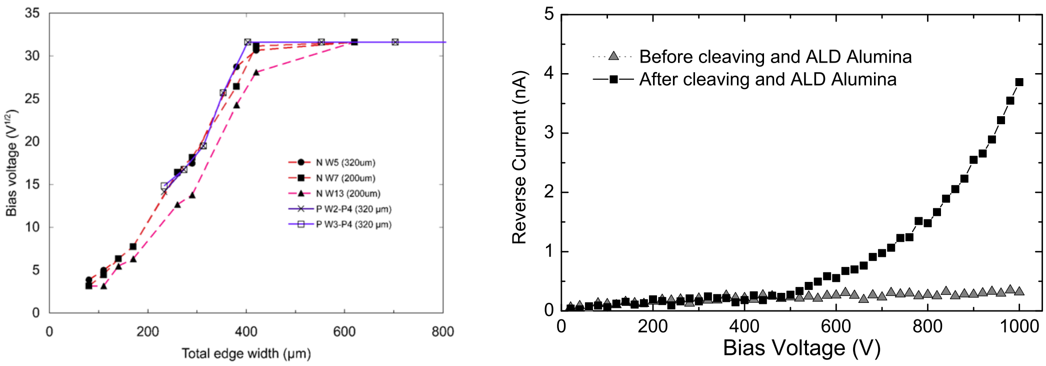


Figure 7: Left: The square root of the bias voltage for the start of breakdown as a function of the total edge width for Hamamatsu test devices. Right: the leakage current as a function of bias voltage for an ATLAS07 diode with cleaved edges 54 μm from the guard ring and ALD alumina edge passivation,

In high-efficiency solar cells, passivation with alumina using an atomic layer deposition (ALD) process provides field-induced isolation of the device edges, due to negative trapped charges in the alumina [42]. The University of California at Santa Cruz has been investigating the use of ALD alumina for the sidewall passivation after laser scribing and cleaving of n-in-p FZ planar sensors to produce slim edges. Results so far have been really promising; a pad diode from the ATLAS07 series has been cleaved 54 μm within the single guard ring and passivated with ALD alumina. After an high-temperature annealing step, the device has low leakage currents up to 1000 V [43], as shown in fig. 7. Based on these results, a new RD50 common project has been funded to extend this study to pixel and strip sensors with both n-type and p-type bulk, including basic measurements of the charge density profile on the edges, of surface recombination and lifetime measurements at the cleaved edges, and of SEM images of the cleaving and ALD alumina.

The final approach for reducing the inactive volume of devices is active edges. After backside implantation, sensors are oxide bonded to a support wafer. The edges of each device is defined by deep reactive-ion etched trenches with p^+ doping. The trenches are then filled with polysilicon. As shown in fig. 8, this process leads to an active edge with the same doping as the backplane. Two sites are pursuing this option. FBK [44] in conjunction with LPNHE is designing FEI3 and FEI4 compatible devices with no or three guard rings. VTT [45] is currently collecting partners for a joint active edge detector project with available thicknesses of 100 and 200 μm.

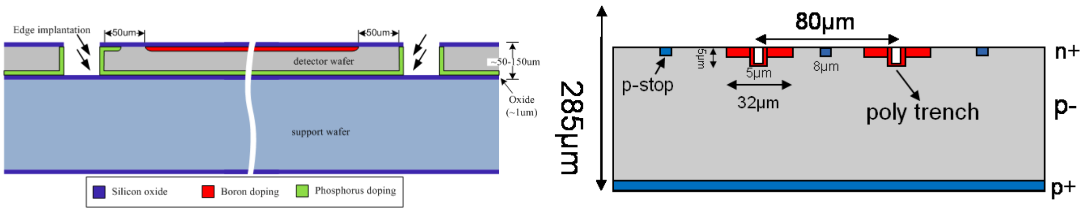


Figure 8: Left: Diagram of the active edge process at VTT. Right: Cross-sectional drawing of trenched detector for multiplication enhancement.

4.2 Charge Multiplication Enhancement

As most of the charge multiplication in planar n-in-p FZ sensors occurs in a narrow region around the segmented n^+ implants, the shape of the implants may be able to be profiled to enhance or reduce this effect. In order to study the effects of implant geometry, the RD50 collaboration is producing 300 μm thick, 6 inch n-in-p FZ wafers with Micron consisting of 60 miniature (1×1 cm^2) strip sensors. The devices have 3 different pitches (40, 80, and 100 μm); each pitch has 3 different implant widths. In addition, all the devices have variants with floating and biased intermediate strips. The wafers have been received and a large program of irradiation and measurement is underway.

Within RD50, a second production exploring enhancement of charge multiplication is underway at IMB-CNM. Two styles of miniature micro-strip devices are understudy. In the first style, a narrow trench is made along the center of the n^+ implant and then filled with polysilicon doped with phosphorus, as shown in fig. 8. This new n^+ implant is expected to modify the electric field, increasing the rate of multiplication after irradiation. Trenches of 5, 10, and 50 μm will be evaluated. In the second style, a p-implant is deeply diffused under the segmented n^+ electrodes. The n/p junction created along the center of the strips by the deeply diffused n^+ implant creates a high field region, which could also enhance charge multiplication effects after irradiation. Simulations of these devices can be found at [46]. A number of these devices have been produced and irradiated. A study of the charge collection performance as a function of irradiation for the two device types is currently underway.

5. Conclusion

Enormous progress has been made evaluating n-in-p FZ technology. It has been shown to be radiation tolerant enough for even the innermost layers of HL-LHC experimental upgrades. Numerous productions of n-in-p FZ strip and pixel silicon devices with 8 different foundries are well underway, with n-in-p FZ technology already chosen as the baseline for the silicon strip regions of the ATLAS HL-LHC upgrades. Vibrant R&D programs are underway to reduce the inactive regions of n-in-p FZ planar devices and to enhance the radiation tolerance through control charge multiplication. These avenues of research should result in the needed devices for the extreme radiation environments of HL-LHC experiments.

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