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Development and Applications of the Timepix3 Readout Chip

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A new pixel readout chip called Timepix3 is being developed that can be used in a wide range of applications varying from X-rays imaging to particle track reconstruction. The Timepix3 will be suitable for readout of both semiconductor detectors and gas-filled detectors.
Depending on the application requirements user can choose one out of three data acquisition modes available in the Timepix3. In the most advanced mode both arrival time information and charge deposit information will be delivered for each hit together with the coordinates of the active pixel. The chosen architecture allows for continuous and trigger-free readout of sparsely distributed data with the rate up to 20Mhits•cm^{-2} •sec^{-1}. For imaging applications and for calibrations the possibility exists of operating in frame-based (non-continuous) data readout mode.
The Timepix3 chip is planned for production in the beginning of 2012.

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1.Introduction

Since the mid 90s readout chips of the Medipix family have been used to build hybrid photon counting pixel detectors for various imaging and medical applications [1]. In these detectors the chips are bump-bonded to the active medium (semiconductor sensor), where direct charge conversion of the X-rays photons takes place delivering high quality images of the object.
The Medipix1 [2] was an evolution of a R&D chip designed for a particle detector. Each pixel had a 15 bit counter which was incremented by signals from photons having an energy larger than 5keV. In order to improve spacial resolution in the detector the pixel size was reduced in Medipix2 [3] down to 55μm. Each pixel had two identical pulse height discriminators. This topology allowed for pulse-height-resolved photon counting used in spectroscopy-aware applications. A highly configurable Medipix3 [4] chip has been designed recently. Its main feature is a new charge summing architecture, which aims to improve the energy resolution in pixelated detectors by mitigating the effect of charge sharing between pixels.
The Timepix1 [5] readout chip is a spin-off of the Medipix2 made on request of the EUDET collaboration. It is meant for the use in Time Projection Chambers and other micro-pattern gas detectors. Each pixel in this chip has a circuit that can operate either in time measurement mode or in charge measurement mode. Readout of one event involving just a few pixels requires the readout of the whole chip. Therefore the Timepix1 can be used only at low event rate and has dead time. Time resolution is constrained to 10ns due to limitations in the distribution of the (100MHz) clock across the pixel matrix. Moreover the accuracy of the time measurement is not optimal due to the time-walk effects in the front-end.
The goal of the Timepix3 project is to develop a general-purpose integrated circuit suitable for readout of both semiconductor detectors and gas-filled detectors. Compared to Timepix1 the circuit will have more functionality, higher time resolution and more advanced architecture for continuous sparse data readout with zero-suppression. It is the Medipix3 collaboration that directs and supports the Timepix3 project.

2. Timepix3: architecture, modes of operation and main specifications

Timepix3 is a 256x256 pixel readout chip structured in 128 double columns. A double column is divided in 64 4x2 pixel groups called super pixels (see Figure 1). Each pixel (55μm by 55μm) is equipped with a fast-response frontend circuit that guarantees high resolution time measurement. The low threshold (500e^-) frontend circuit will be symmetrically sensitive to the input signals of both polarities and will compensate for sensor leakage current. The digital part of the pixel includes a time-over-threshold counter, a coarse-time stamp register and a fine-time counter. A local start-stop ring oscillator per super pixel will generate the fast clock (640MHz) needed for the fine-time stamping.
The on-pixel data will be transferred to the super pixel FIFO and later on to the End-of-Column FIFO via a shared double column bus. A token ring topology is used to arbitrate the bus. After adding the double column ID the data packet is transferred to end-of-the chip logic (Data output block). An 8b10b encoder will be implemented to ensure the reliability of the data transmission off the chip. Data transfer rate is limited

by the bandwidth of the Data output block to 2.56 Gbps. The limitation imposed by the on-chip readout architecture is negligible.

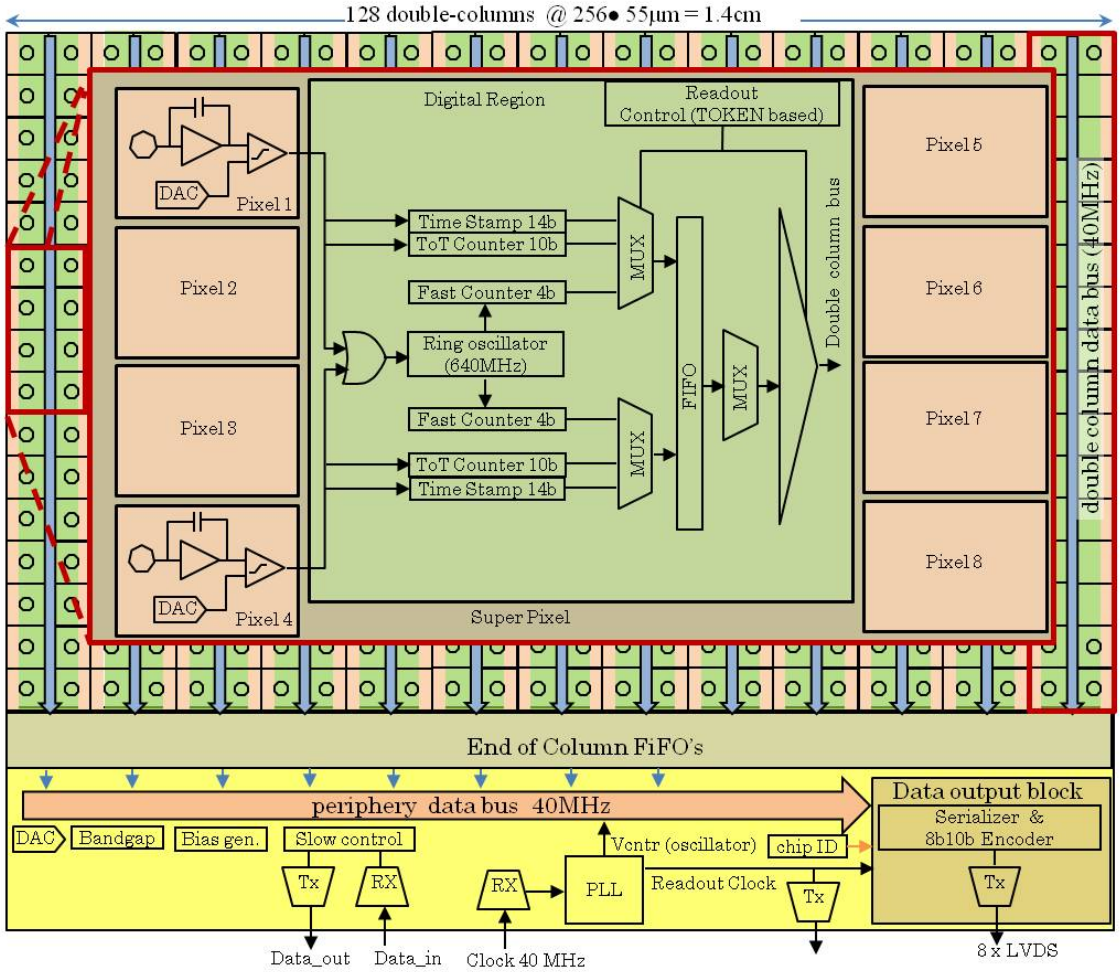

Figure 1. Top level block diagram of Timepix3 chip

2.1 Modes of operation

Timepix3 will have several modes of operation namely ToA&ToT, OnlyToA and EventCount&IntegralToT (see Table 1). In the ToA&ToT (Time-of-Arrival and Time-over-Threshold) data acquisition mode the data packet includes pixel coordinate (16bit), time-over-threshold information (10bit) and time-of-arrival information (4bit fine-time with a resolution of 1.6ns and coarse-time 14bit with a resolution of 25ns). The time-over-threshold information represents the measured deposited charge in the range up to 150ke$^-$. Transportation of the data from the pixel to the super pixel memory lasts 700ns. In addition to the analog frontend recovery time (analog dead time) it will result in significant dead time at the pixel level.

Some applications require a smaller dead time while they do not need the ToT information. For these applications the OnlyToA data acquisition mode is implemented. In this mode the data transportation off the pixel starts right after the discriminator signal goes high. The readout takes only 450ns and occurs during the analog dead time.

In the ToA&ToT and OnlyToA modes hits are transferred immediately to the superpixel FIFO and subsequently sent to the periphery of the chip for further readout. Hence the Timepix3 can sent continuously zero-suppressed information to the data acquisition system.There will be no data loss if the hit rate does not exceed the level of $20 \cdot 10^6$ cm^{-2} sec^{-1}.
The EventCount&IntegralToT mode is meant for photon counting applications. In this mode a shutter signal is used to define the exposure time. When the shutter is open the pixel is counting (10bit) the number of hits. In addition the combined energy deposit of all the hits or integral ToT (14bit@25ns) will be measured. When the shutter closes the counting is stopped, and the readout of the complete matrix started which takes 1.6 ms at most. During the data taking phase (shutter is open) a hit rate of 100 kHz-per-pixel can be handled.

Table 1.
Modes of operation of the Timepix3

	Data acquisition mode		
	ToA & ToT	Only ToA	Event Count & Integral ToT
Data format	Fast Time (640MHz @ 4b) & Slow Time Stamp (40MHz @ 14b) & ToT (40MHz @10b) & Pixel coordinate (16b)	Fast Time (640MHz @ 4b) & Slow Time Stamp (40MHz @ 14b) & Pixel coordinate (16b)	Event Count(10b) & Integral ToT (14b) & Pixel coordinate (16b)
Double hit resolution (per pixel)	ToT + 700ns	> 450ns	-
Readout	continuous sparse data readout with zero-suppression		non-continuous sparse data readout with zero-suppression
	Max counting rate < 1kHz/pixel		Max counting rate < 100kHz/pixel
Full chip readout time	-		1.6msec

The peripheral circuitry is placed at one side of the die. This will allow to minimize detector dead area in a construction when many chips are put together. Also through-silicon via's will be used, they will be implemented next to the die wire bond pads to enable the 3D chip interconnection.

3. High resolution TDC-per-pixel topology

In order to obtain an accuracy of 1.6ns of time measurements each pixel in Timepix3 chip has a high resolution Time-to-Digital Converter (TDC). The TDC topology is based on concept of start-stop ring oscillator [6]. It starts to oscillate at 640MHz frequency every time when a hit signal arrives and is stopped by the rising edge of the 40MHz clock signal. The number of pulses at the output of the oscillator gives the position of the hit signal within one clock period (see Figure 2). One oscillator circuit will be shared between 8 pixels inside a super pixel.

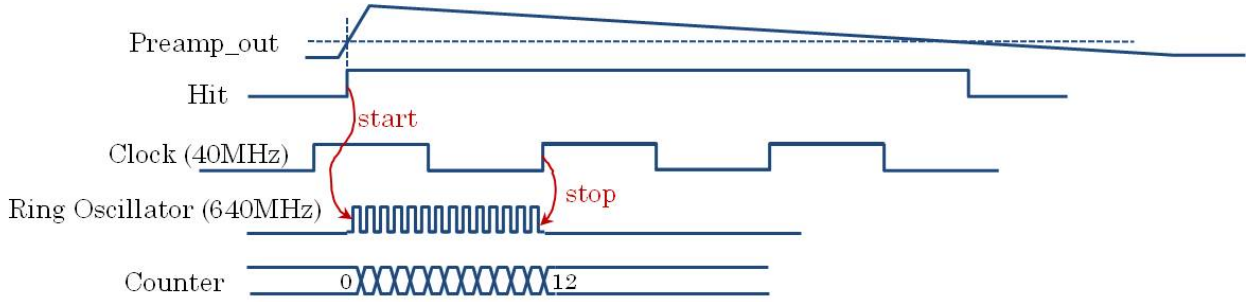

Figure 2. Signals in the TDC based on concept of the start-stop ring oscillator

The oscillator is active only for less than one clock period (25ns) and only when the hit signal occurs. Therefore its switching activity is proportional to the hit rate and is quite low. The oscillator does not consume power when it is not active. Even when operating at the maximum rate ($20 \cdot 10^6$ cm^{-2} sec^{-1}) the power consumption is negligible. Apart from the oscillator the TDC comprises a 4b counter and a block of synchronization logic which take about 10% of the pixel area.

The ring oscillator circuit is a NAND gate with a number of buffered RC delay circuits in the feedback chain (see Figure 3). Voltage-controlled capacitors (varactors) are used to regulate the RC-delay and change the oscillation frequency in the range of 50%. That will be sufficient to obtain the target frequency of 640MHz in every process corner.

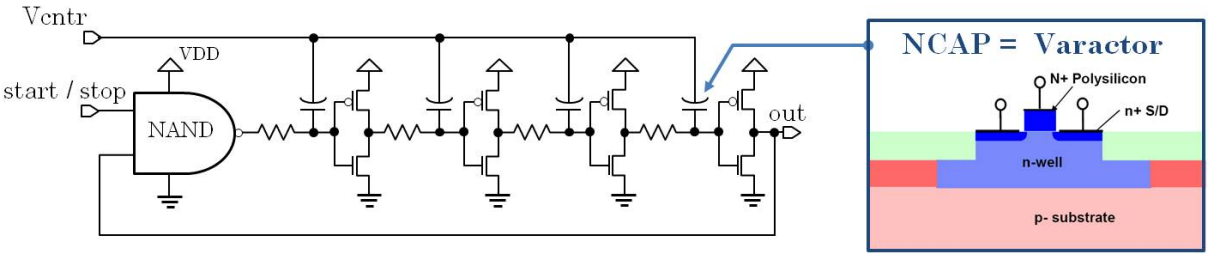

Figure 3. The start-stop ring oscillator implemented in the TDC

The RC-based topology of the ring oscillator is an attractive option for the use in a large-size circuit having significant power supply voltage variation across the die. The varactor bias voltage controls the oscillation frequency and the dependence of the supply voltage is minimal. Because of the good matching properties of the resistors and the capacitors the running frequency does not vary by more than 1% from one oscillator to another.

A PLL circuit with an embedded replica of the ring oscillator will be placed in the periphery of the chip. The PLL will be locked to an external system 40MHz clock. The PLL forces the ring oscillator to run at exactly 640MHz compensating for the fabrication process variation and the temperature drift. The locked-in bias voltage (Vcntr) generated in the PLL will be broadcast across the chip to control local ring oscillators. Those will also run at exactly 640MHz (16 times the system clock of 40MHz) when being switched into the active state. The ring oscillators will not draw current from the bus carrying the control voltage signal. Hence the control voltage will be the same across the whole chip.

4. Frontend circuit

The charge-sensitive preamplifier (see Figure 4) in Timepix3 will be symmetrically sensitive to the input signals of both polarities. The circuit is based on the Krummenacher scheme [7]. It can either sink or source the sensor leakage current making it possible to readout both electron and holes emitting detectors. High gain (50mV/1000e^-) and low noise (σ = 75e^-) ensure efficient hit identification. The circuit has fast peaking time (~10ns) and therefore the time-walk will have a limited impact on the accuracy of the measurement [8]. The preamplifier consumes 3μA from a 1.5V power supply source. A fast response pulse height discriminator will be implemented in order to limit the propagation delay skew and prevent deterioration of the hit arrival time information.

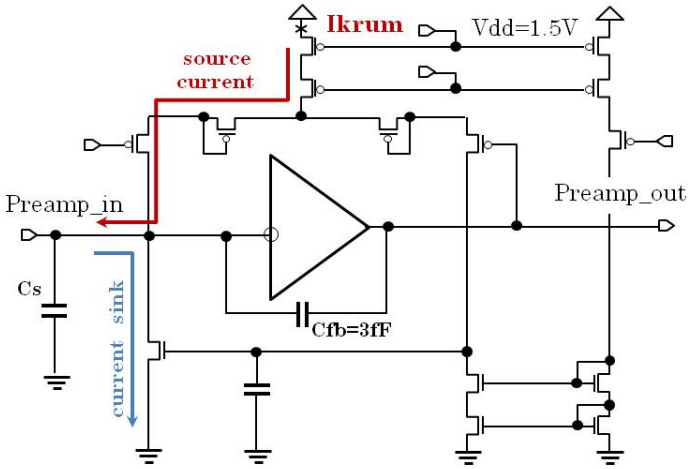

Figure 4. Schematic of the preamplifier circuit

For this reason the value of the propagation delay will be kept close to the TDC bin size (1.6ns). The discriminator will consume only 4 μA of current which is not much for such a high speed circuit. Each pixel will be equipped with a 4-bit DAC needed to compensate the mismatch in the threshold value to the level of 10e^-.

5. Data readout off the Timepix3 chip

8b/10b coding will be implemented for data readout in the Timepix3 chip. This code maps 8-bit symbols to 10-bit symbols to correct disparity between 1s and 0s in a string of bits and provide DC balance on the line. This scheme guarantees continuous switching activity sufficient for stable operation of the clock recovery unit at the receiver side. In this scheme the clock and the data are embedded into one signal and no separate clock line is required. The clock skew variability will be very much under control in the coded signal eliminating the possibility of timing violation and data losses in the readout link. Standards using the 8b/10b encoding also define control characters that can be sent in place of a data symbol for the link synchronization and data alignment.

Although the 8b/10b-coded link is a very attractive feature in the Timepix3 readout, the legacy Medipix readout systems require the traditional or non-coded option as well. Therefore a separate clock output line will be available (see Figure 5).

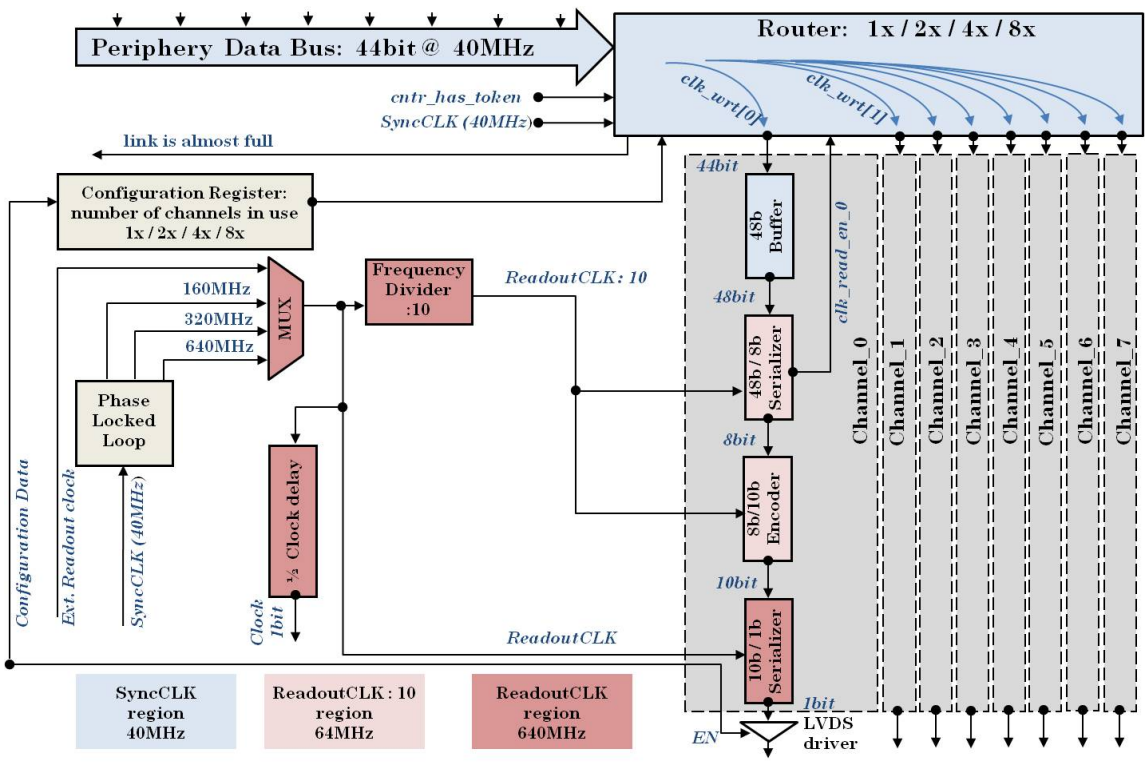

Figure 5. Block diagram of the Output block in the Timepix3

The Output block in the Timepix3 includes a Router that directs a hit data packet to one of readout channels every system clock cycle (40MHz). The Configuration register sets the number of the channels to be used from 1 to 8. A 48-bit data packet will be read out the Buffer in the format of six 8-bit symbols for 8b/10b encoding. The output serializer converts 10-bit symbols into a serial stream to the LVDS driver. The Readout clock signal will be generated either on-chip by the PLL or must be delivered by an external source. The PLL [9] will provide a number of Readout clock frequencies to run the 10b/1b Serializer. If the Readout clock frequency is not high enough to make the Buffer empty before a new write-in cycle occurs, a link_is_almost_full signal will be generated to suspend sending new data to the Output block. Each of the channels will be sending IDLE symbols in absence of hit data.

6.Summary and outlook

The Timepix3 pixel readout chip is being developed in the framework of the Medipix3 collaboration for a wide range of applications. Although the chip will not be tuned for any specific particle physics experiments, it will be used by many R&D groups to explore possibilities and performance of new types of detectors. Among those are the Vertex Locator (VELO) detector for the LHCb upgrade and various micro-pattern avalanche gas detectors. A multi-site design team from CERN, Nikhef and Bonn University is working on getting the Timepix3 chip ready for production in the beginning of 2012.

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