PROCEEDINGS OF SCIENCE

The ATLAS insertable B-Layer (IBL) project

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The ATLAS detector upgrade will undergo different phases towards super-LHC. The first step for the Pixel Detector will consist in the installation of a new pixel layer during the shutdown of the LHC machine in 2013. The new detector, called Insertable B-Layer (IBL), will be inserted between the existing Pixel Detector and a new (smaller radius) beam-pipe, at an average sensor radius of 3.4 cm. The IBL requires the development of several new technologies to cope with the increase of radiation and pixel occupancy at such a reduced radius. Improvements of the tracking physics performance will be achieved by reducing the pixel size and the material budget. An overview of the project is presented in this paper.

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1. Introduction

The Pixel Detector [1] is the innermost detector of the ATLAS [2] tracking system and consists of 3 barrel layers and 6 disk layers, 3 disks in each of the forward and backward directions. It provides at least three high accuracy space-point measurements per track for pseudo-rapidity [1] $|\eta| \leq 2.5$, as needed for track and vertex determination. The innermost pixel layer, so called B-Layer, is located at a radius of 5 cm and plays a crucial role for tracking, vertexing, and *b*-tagging capabilities of ATLAS, especially at high luminosity.

Modules are the basic building blocks of the detector, 1744 in total. Each module consists of a planar n-in-n DOFZ [2] silicon sensor tile, 16.4 mm $\times$ 60.8 mm of sensitive area and 250 μm thickness, and 16 front-end (FE) integrated circuits, each one reading-out 18 $\times$ 160 pixel diodes. On each module, an additional integrated circuit, the Module Control Circuit (MCC), handles data compression and transmission from the front-end chips to the external read-out drivers, and distributes control and clock signals to the front-end chips. The read-out speed is 40 or 80 Mb/link according to the detector position.

The detector has been designed to face a total dose of 50 MRad, a fluence of $1 \times 10^{15} \mathrm{n}_{eq}/\mathrm{cm}^2$ and a peak luminosity of $1 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$. This means that the expected lifetime for the B-Layer, the most exposed to radiation damage, corresponds to an integrated luminosity of about 300 fb^{-1}. Given the present LHC schedule, while the integrated luminosity should reach $\approx$ 340 fb^{-1} at the end of Phase I ($\approx$ 2022), therefore compatible with the detector design, the peak luminosity could reach $2 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$ generating some inefficiency in the B-Layer where the occupancy is higher. The expected inefficiency of the read-out electronics in the B-Layer with respect to the hit occupancy is shown in Figure 1.

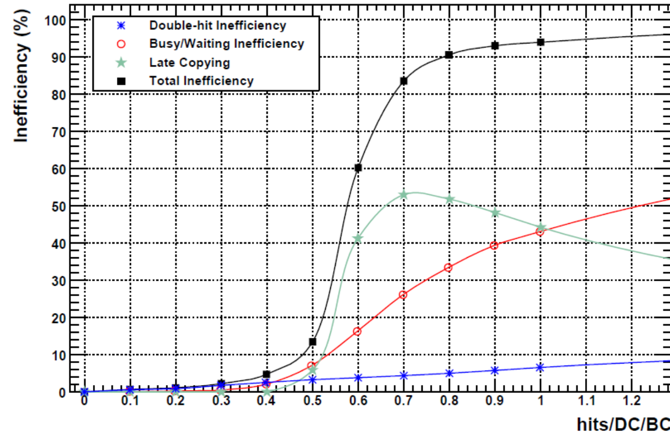

Figure 1: FE inefficiencies as function of the double-column occupancy per bunch crossing. The expected occupancy in the B-layer central module at $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is 0.165 hits/DC/BC. For peak luminosity of $2 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ the inefficiency could reach $\approx$ 3%. Considerable uncertainty, however, should be attached to these values, because of the strong dependence of the simulation upon the time structure of the events.

[1] $\eta = -\ln(\tan(\theta/2))$ where θ is the polar angle from the beam axis.
[2] Diffusion Oxygenated Float-Zone

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In order to mitigate the influence of partial loss of efficiency in the present B-Layer with the increasing luminosity, the 3-layer Pixel Detector will be upgraded to a 4-layer detector through the addition of the "Insertable B-Layer" (IBL) [3] during the LHC shutdown of 2013. The IBL will be built around a new, smaller radius (23.5 mm) beam-pipe and slipped inside the present Pixel Detector, which will be maintained .

The physics impact of the extra layer has been studied in detail by fully integrating the IBL into the ATLAS Inner Detector simulation software. Because of the low mass, the reduced radius and the smaller pixel size, the IBL improves the impact parameter resolution for tracks and thereby the vertexing and b-tagging performance whenever the pile-up increases significantly. As an example, Figure 2 left shows the b-tagging performance as a function of the average number of pile-up interactions for a standard b-tagging algorithm, comparing the results with and without IBL as well as for different track selections. The light jet rejection[3] at 60% b-tagging efficiency with IBL and $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ pile-up is better than the performance of the current detector with no pile-up. Also the impact of the IBL in case of failure scenarios has been studied using dedicated simulation samples. The case of dead detector modules (3.1% of the modules in the B-Layer are not operational at the moment) and the inefficiencies of the present electronics at high luminosity have been assessed. Figure 2 right shows the b-tagging performance as a function of the average number of pile-up interactions in case of 10% of B-Layer hits randomly lost: the reconstruction with IBL not only recovers from the simulated failures, but exceeds the performance of the current detector without such failures.

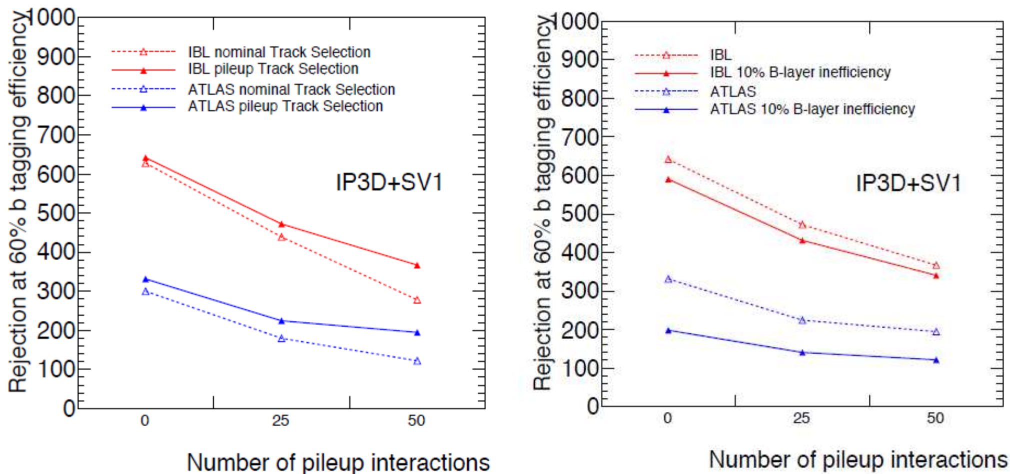

Figure 2: Light jet rejection in $t\bar{t}$ events for 60% b-tagging efficiency as a function of the average number of pile-up interactions: on the left figure results are compared with and without IBL and different track selection; on the right plot the same comparison in case of a failure scenario in which 10% of the B-Layer hits are randomly lost. At $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ the average number of pile-up collisions is ≈ 50. For these studies the default ATLAS impact parameter based b-tagging algorithm (IP3D) and secondary vertex based algorithm (SV1) are used.

[3]The jet rejection is defined as the inverse of the mis-tagging rate which is the fraction of non b-jets erroneously tagged as b-jets [4].

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2. Requirements and Layout

The IBL sensors and front-end electronics will be located at an average radius of $\approx$ 34 mm from the beam axis. Such a small radius implies severe requirements for the IBL. For an integrated luminosity up to $\approx$ 550 fb^{-1}, including safety factors, the IBL needs to withstand 250 Mrad of ionizing dose and $5 \times 10^{15} \mathrm{n}_{eq}/\mathrm{cm}^2$ of non-ionizing dose, that corresponds to a factor 5 larger radiation hardness with respect to the current Pixel Detector requirement. To allow performance gains, the IBL developments are aimed at reducing the radiation length of all inactive parts: most notably with thinning of the electronics, light flex circuits and the use of light-weight materials in support and cooling parts. While the radiation length of a present pixel layer is approximately 2.7%, the IBL project aims for a total of 1.5% radiation length.

The IBL will consist of 14 pixel staves surrounding the beam-pipe. Each carbon-fibre stave carries and provides cooling to 32 FE-I4 read-out chips [5], which are bump-bonded to silicon sensors. The IBL collaboration currently considers two type of sensors: planar n-in-n sensors, similar to the present Pixel Detector [1], and 3D silicon sensors [6]. In case of planar sensors, one sensor tile carries two FE-I4 chips, in case of 3D sensors, one sensor carries one FE-I4 chip. The staves are inclined by 14° with respect to the radial direction in order to achieve overlap of active area between staves and to compensate for (a) the Lorentz angle of drifting charges in the 2 T magnetic field in case of planar sensors or (b) the effect of partial column inefficiency with perpendicular tracks in case of 3D sensors. There is no shingling of sensors along z due to the lack of radial space. Modules are glued on the stave with a physical gap of 200 μm for planar two-chips modules and 100 μm in case of single-chip 3D modules. The 643 mm long active area of a stave corresponds to a pseudo-rapidity coverage of $|\eta| < 3$. From the end of stave, services for power, read-out and cooling connect each half-stave to the end of the Pixel Detector, and from there to the power supply, control and read-out units in the counting rooms of ATLAS. Figure 3 shows a

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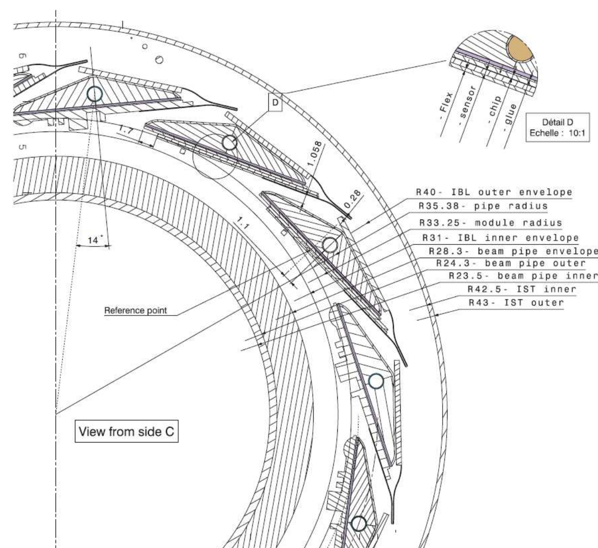

Figure 3: Section view of the IBL, the new beam-pipe and the IBL support tube (IST). Radii of envelopes are given in mm.

cross-sectional view of the IBL detector, the new beam-pipe and the IBL Support Tube (IST). The staves are mounted around the beam-pipe with the modules facing the pipe. The function of the staves is to support the detector modules around the beam-pipe, provide cooling to them and carry the multi-layer flexible circuit in Al/Cu which electrically supplies and reads out the FE-chip. The staves are cooled by an evaporative CO2 cooling system [7], that has been chosen to allow lower sensor temperature and usage of a small diameter, 1.5 mm, cooling Ti pipe inside the stave, which minimizes the material.

3. Modules

In order to improve the tracking performance of ATLAS, the IBL assembled modules need to fulfill tight requirements, namely: hit efficiency $> 97\%$ at the end of the detector lifetime, minimal inactive edge (typically 200 μm), low operational threshold (about 1500 e^-), bias voltage ≤ 1000 V and power dissipation below 200 mW/cm^2 for a sensor temperature of -15 °C.

3.1 Electronics

In the IBL the read-out electronics has to cope with a larger fluence and peak luminosity, higher hit rate and occupancy, therefore a new generation of read-out chip, FE-I4, has been developed starting from the current Pixel Detector electronics design. To solve the inefficiencies expected in the FE-I3 at high luminosity, a new architecture has been deployed. A 2×2 pixel region in a double column share a common digital processing stage, which includes hit buffering, trigger logic and data encoding. The local hit buffering resolves the data transfer limitation of the previous design, where any hit was transferred to the end of column for buffering, being inefficient as less than 1% of the hits are effectively triggered. The FE-I4 chip is manufactured in the IBM 130 nm CMOS process and has a large active area (16.8×20 mm^2) to reduce the dead regions. Pixels are organized in an array of 80×336 cell, each pixel size is reduced to 50×250 μm^2. The main differences between the two chip generations are summarized in Table 1.

Table 1: Main parameters of FE-I3 and FE-I4.

	FE-I3	FE-I4
Pixel size (μm^2)	50×400	50×250
Pixel array	18×160	80×336
Chip size (mm^2)	7.6×10.8	20.2×19.0
Active Fraction (%)	74	89
Analog current (μA/pixel)	26	10
Digital current (μA/pixel)	17	10
Analog voltage (V)	1.6	1.4
Digital voltage (V)	2.0	1.2
Data out transmission (Mb/s)	40	160

The first full chip version (FE-I4A) has been submitted in 2010 and has been extensively tested without and with sensors as well as in irradiations and test beams. Yield on wafer is pretty high (70%) for such a large chip. The preliminary noise measurement has shown a typical r.m.s.

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noise of 80 e^- without sensor, 130 e^- to 140 e^- with un-irradiated sensors and 150 e^- to 160 e^- with sensors irradiated up to $5 \times 10^{15} n_{eq}/cm^2$, pending further gain calibration, which is currently ongoing. In testbeams and laboratory tests the FE-I4 could routinely be operated with thresholds of 1600 e^- with both sensor types, which is significantly lower than the previous FE-I3 chip working point.

3.2 Sensors

The sensors currently supported for the IBL are planar n-in-n pixel sensors and 3D silicon pixel sensors. The 3D sensors will be arranged on the edges of the staves, to exploit their better charge collection at large $|\eta|$, covering 25% of the total sensitive area.

The planar n-in-n sensor design is largely based on the design of n-in-n sensors used in the ATLAS Pixel Detector. The sensors are manufactured by CiS[4] and they are 200 μm thick. The design has been adapted to the IBL needs by reducing the pixel size from $50 \times 400\ \mu m^2$ to $50 \times 250\ \mu m^2$ and by optimizing the edge region, in order to maximize the possible operation voltage and minimize the inactive edge. The so-called "slim-edge" design, shown in Figure 4a), uses guard rings on the bias side of the sensor to manage the potential drop between bias contact and physical sensor edge. To maximize the active area, the edge pixels on the electrode side of the sensor are 500 μm long and overlap the guard ring area. Within this overlap the detector operates underdepleted, however still sufficient charge is collected so that hits are registered and the area can be considered active, see Figure 5. Testbeam results indicate an inactive edge of 200-250 μm with this layout.

In the 3D sensor design the measuring and biasing electrodes are edged through the p+ silicon bulk by Deep Reactive Ion Edging (DRIE), as shown in Figure 4b)-c). The sensor is depleted between n+ pixel electrodes and p+ biasing electrodes. This biasing scheme makes the sensor depletion independent of the sensor thickness. It allows for high field strength and good charge collection after irradiation at moderate bias voltages. For the IBL a design with two n+ electrodes per pixel, surrounded by six p+ biasing electrodes, has been chosen to optimize the maximum collected charge and minimum electronics noise due to detector capacitance [8]. The sensors are 230 μm thick and are manufactured in double-sided processes by CNM[5] and FBK[6]. The sensors manufactured by the two firms share the same top metal layout for identical bump-bonding connection to the electronics. Both 3D designs by CNM and FBK feature the edge pixel of standard 250 μm length and an inactive edge of 200 μm width. However the production processes, the design of the edge region, the electrodes properties, the isolation techniques are different between the two manufactures.

The sensor designs for planar and 3D detector have been extensively prototyped and tested with ATLAS Pixel FE chips. Initial pre-production runs with FE-I4 chips have shown a good sensor yield of approximately 90% for planar sensors and 60% for 3D sensors. The difference in yield is due to the more complex manufacturing steps in 3D detectors. Table 2 summarizes the main sensor characteristics.

[4]CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Erfurt, Germany, http://www.cismst.org/

[5]Centro Nacional de Microelectronica, Barcelona, Spain http://www.cnm.es/

[6]Fondazione Bruno Kessler, Trento, Italy, http://www.fbk.eu/

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Table 2: Main parameters of the 3D and planar Si sensors.

	3D	Planar
Active size (mm^2)	16.8×20.0	16.8×40.9
Physical size (mm^2)	18.8×20.5	18.54×41.3
Thickness (μm)	230	200
Typical depletion voltage (V)	≤15	≤35
Typical initial operation voltage (V)	25	60
Operation voltage at end of lifetime (V)	180	1000

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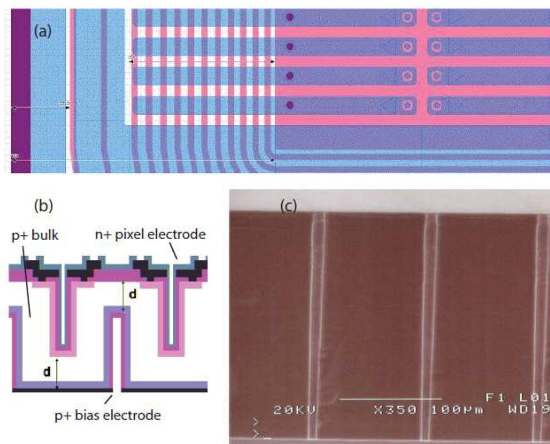

Figure 4: (a) Edge pixel and guard ring layout of the IBL planar n-in-n silicon sensor design. (b) Schematic view of the 3D silicon pixel sensor (c) Micrograph of the deep reactive ion edged (DRIE) columns in a 3D sensor manufactured by FBK.

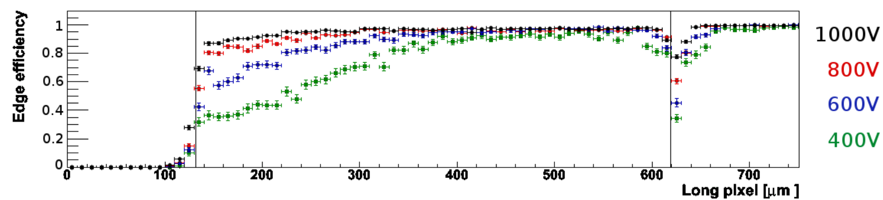

Figure 5: Efficiency for the edge 500μm long pixels for a planar sensor irradiated with neutrons at $3.7 \times 10^{15} n_{eq}/cm^2$ and different values of the sensor bias, measured at the SPS June 2011 testbeam. The edges of the pixel cell are highlighted by the two vertical lines. The efficiency is rather high in the full region if the applied voltage is high enough.

3.3 Hybridization and connection to the external services

More than 80 FE-I4-sensor devices have been assembled by IZM[7] using SnAg solder bump-bonding to obtain IBL prototype modules for tests of electronics and sensors performance. Due to the large chip size, a significant bow of the chip during the reflow of solder bumps is expected. If the out of plane bow exceeds 20 μm, some pixels can be expected to be disconnected, mainly on the edges. To avoid this edge disconnection either a thick chip (450 μm) or a handling wafer on top of a thin chip is needed. While in the prototyping phase thick electronics has been used, to reduce extra material in the detector a handling wafer process has been devised: the chip is thinned to a thickness between 100 and 150 μm and a glass handling wafer is bonded to the thinned chip wafer using a photo-sensitive adhesive. After the flip-chip and reflow process the glass is removed by means of laser exposure of the adhesive. The first single and two-chips thin IBL modules have been successfully assembled using this process.

Most of the prototype FE-I4 sensor assemblies, usually single-chip assemblies mounted on test boards, have been characterized in laboratories, in testbeams, before and after irradiations. Preliminary analysis of the testbeam data confirm a tracking efficiency of $> 99\%$ on un-irradiated planar and 3D IBL prototype modules. Analysis of data taken on irradiated modules is currently in progress.

Procedures to build, handle and load IBL thin modules are currently being finalized: a flex circuit with passive components will be glued on the back of the sensor and, once the module will be qualified and glued on the mechanical support, it will be used to establish the connection via wire-bondings to the multi-layer flex, laying on the stave backside, see the sketch shown in Fig. 6.

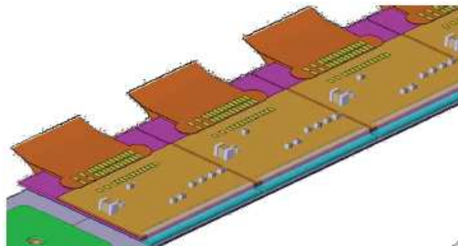

Figure 6: Three-dimensional view of IBL modules on stave, close to the support edge.

4. Conclusions

ATLAS currently develops and constructs a new Pixel Detector layer for the first upgrade of its tracking system: the ATLAS Insertable B-Layer Pixel Detector (IBL). The new layer will be inserted between the innermost layer of the current Pixel Detector and a new beam pipe, with reduced radius. A new generation of pixel FE-chip, allowing for low inefficiencies at high trigger rates, has been developed and tested. A mixed scenario of planar and 3D silicon pixel sensors has been approved, with the 3D sensors at large $|\eta|$ to exploit the better charge collection at large incident angles. The overall support and cooling system has been prototyped, based on staves

[7] Fraunhofer IZM, Berlin, Germany, http://www.izm.fraunhofer.de/

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cooled with an evaporative CO2 system. Production of sensors, read-out electronics, modules and staves has started. The installation is expected to be completed during the LHC shutdown of 2013.

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