

## RADIATION-HARD ASICS FOR OPTICAL DATA TRANSMISSION

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We have designed two ASICs for possible applications in the optical links of a new layer of the ATLAS pixel detector. This new layer is to be installed inside the existing pixel detector for the initial phase of the LHC luminosity upgrade. The ASICs include a high-speed driver for a VCSEL and a receiver/decoder to extract the data and clock from the signal received by a PIN diode. Both ASICs contain 4 channels for operation with a VCSEL or PIN array. The ASICs were designed using a 130 nm CMOS process to enhance the radiation-hardness. We have characterized the fabricated ASICs and the performance of the ASICs is satisfactory. The receiver/decoder properly decodes the bi-phase marked input stream at low PIN currents and the driver can operate a VCSEL up to  $\sim 5$  Gb/s. The added functionalities are also successful, including redundancy to bypass a broken VCSEL or PIN channel, individual control of the VCSEL currents, and a power-on reset circuit to set all VCSEL currents to a nominal value. The ASICs were irradiated to a dose of 46 Mrad with 24 GeV/c protons. The observed modest degradation is acceptable and the single event upset rate is negligible. Experience gained from these prototype ASICs has been incorporated into a new 12-channel version of the chips which will be discussed briefly.

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## 1. Introduction

The Large Hadron Collider (LHC) at CERN (Geneva) is currently the highest energy and luminosity collider in the world. However, planning has already been initiated to increase the design luminosity by a factor of five to  $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ . The ATLAS experiment at the LHC plans to add a new pixel layer to the current pixel detector during the 2013 shutdown. As a result, the optical data transmission will require an upgrade to handle the higher data transmission speed. The upgrade for the optical links will be based on VCSEL and PIN arrays operating at 850 nm as in the current system. In preparation for the upgrade, two new ASICs, a four-channel array driver and a four-channel array receiver, have been designed using a 130 nm CMOS process for this new generation of optical links.

The ASICs have been designed using a 130 nm CMOS process. This is a modern version of the ASICs [1] designed using the 0.25  $\mu\text{m}$  CMOS process which in itself is an updated version of the ASICs [2] designed using 0.8  $\mu\text{m}$  transistors. The driver couples to a VCSEL array with one channel designated as a spare. Similarly, the receiver / decoder couples to a PIN array with one channel designated as a spare. With the inclusion of a remote control interface, this arrangement allows redundancy in both directions by enabling a signal to be re-routed from a bad VCSEL or PIN channel. The submitted chip contains four VCSEL drivers (VDC), four PIN diode receivers/decoders (Digital Opto-Receiver Integrated Circuit or DORIC), and the associated circuitry to control the re-routing of the signals to the designated spare channels. All circuitry within the test chip was designed following test results and guidelines from CERN on radiation tolerant design in the 130 nm process used [3]. We have characterized the fabricated ASICs and then irradiated the ASICs to a dose of 46 Mrad using 24 GeV/c protons. The results will be presented below. Experience gained from these prototype ASICs has been incorporated into new 12-channel versions of the chips which will be discussed briefly.

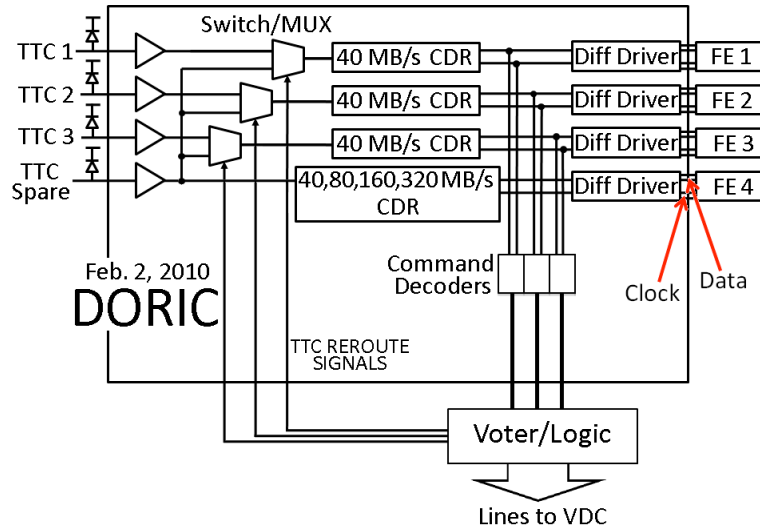
## 2. DORIC

Each of the DORIC channels contains a PIN diode receiver/pre-amplifier, a bi-phase marked (BPM) clock and data recovery circuit, and has low voltage differential signal (LVDS) outputs for both the clock and data. All four DORICs are designed to operate with a 1.5 V power supply and a 40 Mb/s BPM input stream. One of the DORICs includes circuitry to extend its operational speed to 80, 160, or 320 Mb/s. Two-channel multiplexers have been inserted in the post amplification paths of the non-spare DORIC channels. With these multiplexers, the signal from the spare amplifier channel may be routed to the channel of choice. A block diagram of the DORIC section of the chip is shown in Figure 1.

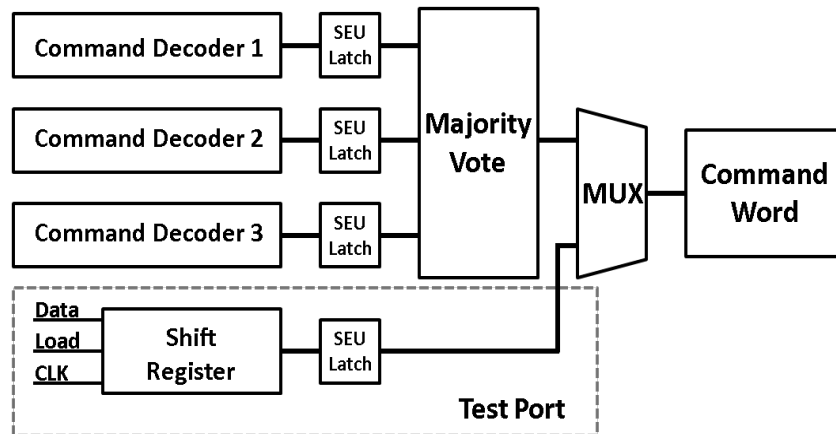
In order to allow remote control over channel steering and other functionality within the chip, a command decoder has been included in three of the DORICs. The command decoder was designed for the front-end (FE) chips of the new pixel layer. Because the chips will be resided in a high radiation environment, special care was taken to improve the single event upset (SEU) tolerance of the command decoder. The command word for configuring the chip is formed by a majority vote of the three command decoders. To further improve our chip's

tolerance to SEUs, all latches in our design are based on a dual interlocked storage cell (DICE) latch designed for use in the configuration memory of the FE chips of the pixel detector.

To simplify some of the testing and to allow verification of the command decoder's operation, we have included a serially interfaced test port to the command word. Figure 2 shows a block diagram of the interface.



**Figure 1:** DORIC block diagram. In the final design, there will be one less output than input, i.e. if one of the PIN diode malfunctions, the optical signal will be transmitted via the spare PIN to the original FE channel.



**Figure 2:** There are two interfaces for loading the 16-bit word needed for the ASIC operation: the command decoder interface on the top or the test port on the bottom.

The current consumption at 1.5 V for the single speed channels is 40 mA per channel. For the multi-speed channel, the power consumption increases to 60 mA due to the circuitry required to handle multiple speed operation. All four DORIC channels can properly decode data at 40 Mb/s with no bit errors for low input PIN currents,  $\sim 20 \mu\text{A}$  for the three single-speed channels and  $\sim 40 \mu\text{A}$  for the multi-speed channel. For the multi-speed channel, the threshold is higher at higher speed, from  $\sim 60 \mu\text{A}$  at 80 Mb/s to  $\sim 100 \mu\text{A}$  at 320 Mb/s. The clock jitter (peak-

to-peak) at 40 Mb/s is  $\sim 1.4$  ns for both single-speed and multi-speed channels. For the multi-speed channel, the jitter is smaller at higher operating speed, as little as  $\sim 100$  ps at 320 Mb/s. It should be noted that the multi-speed channel requires external bias tuning for proper operation at 160 and 320 Mb/s due to the limited dynamic range of the clock duty cycle control circuitry. The steering circuit functions properly, i.e. signal received at the spare DORIC channel can be rerouted through the other DORIC channels. However, this can only be excised via the test port because the scan chain enable of the command decoder was left floating due to a miscommunication with the designer of the command decoder.

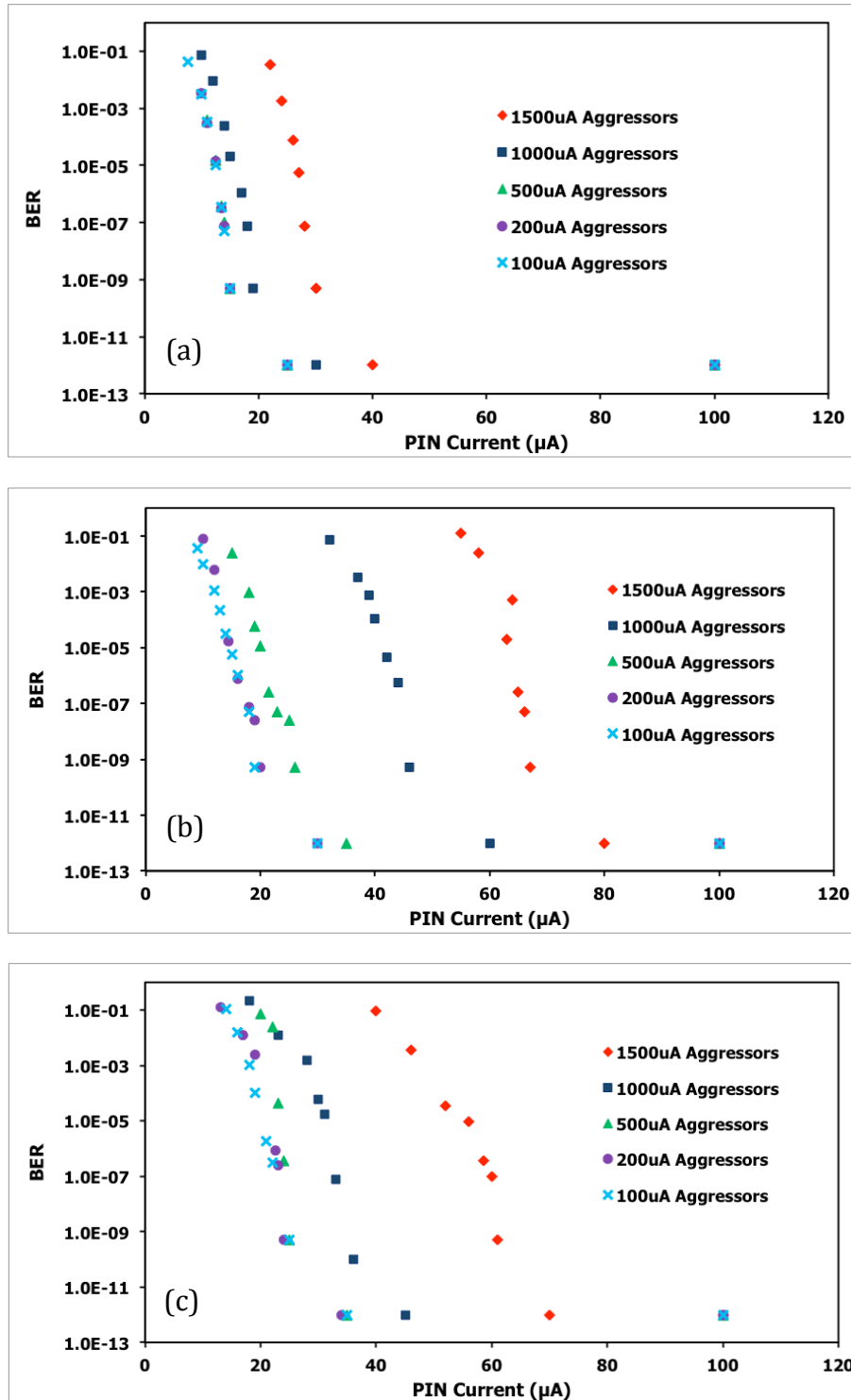
Due to the nature of the optical packaging and the proximity of the channels within the DORIC, we have studied the effects of crosstalk on the bit error rates (BER) of each channel. Because present upgrade scenarios require 40 Mb/s data links to the detector, we have focused our study at this rate. In all cases, we illuminated the aggressor PIN channels with identical input amplitudes running with  $2^{23}$  pseudo-random data. As expected, there is a measurable BER penalty with the other channels operating with large levels of incident light, above  $\sim 500$   $\mu\text{A}$ . In the worst case, with 1,500  $\mu\text{A}$  currents in the aggressor channels, corresponding to 2.5 mW of incident light, the BER threshold curve is shifted up by 35  $\mu\text{A}$  for the multi-speed channel and 15  $\mu\text{A}$  for the single speed channels. A comparison of the BER vs. the input PIN current is shown in Figure 3 for the multi-speed channel, channel 1, and steered channel 1. It is evident that the BER penalty increases significantly as the aggressor channel currents increase. It is interesting to note that the impact of the aggressor channels is more visible in the case when a channel is steered. In the worst case, steering channel 1 across channel 2 and 3 to reach the spare channel, the channel is impacted significantly with 1,000  $\mu\text{A}$  incident on the aggressor channels.

### 3. VDC

The four VDC channels are designed to operate at speeds up to 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a driver stage for converting the received LVDS signal into a current sufficient to drive a VCSEL. Two of the four VDC channels provide the capability to add a pre-emphasis current to the VCSEL modulation current. The duration of the pre-emphasis current pulse and its amplitude are adjustable via wire-bond pads. One of the VDC channels is designated as the spare channel and contains a 16:1 multiplexer. The multiplexer allows routing of the received LVDS signal from any of the other three channels to the spare channel output. A block diagram of the VDC portion of the test chip is shown in Figure 4.

The 8-bit DAC and LVDS receiver are designed to operate with a 1.5 V supply and the driver stage is designed to operate with a 2.5 V power supply. A higher supply voltage is required by the output stage to allow enough headroom to drive VCSELs which normally have threshold voltages of  $\sim 2$  V. The VCSEL driver is designed using enclosed transistors in the thick oxide technology to enhance the radiation hardness. The output driver is capable of delivering up to 12 mA modulation current and up to 4 mA bias current if driving a VCSEL with a 2 V threshold voltage. With the driver operating at 160 Mb/s (the speed required for the new pixel layer) and all channels active with each VCSEL set to 10 mA peak current, the

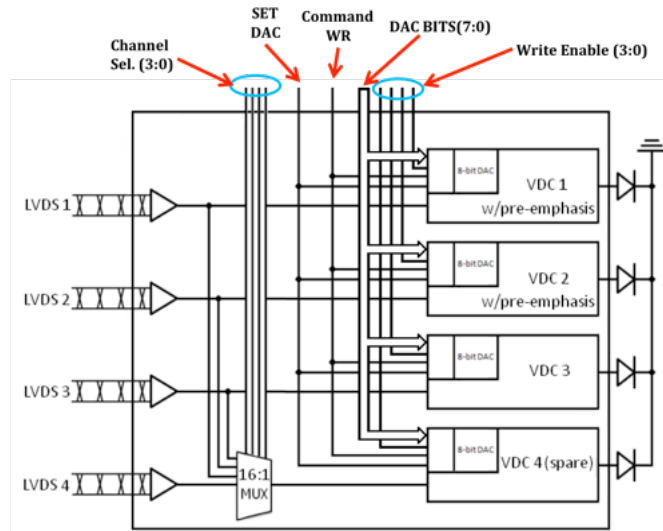
current consumption on the 1.5 V supply is ~5 mA and the consumption on the 2.5 V line is ~90 mA.



**Figure 3:** BER vs. incident PIN current for (a) channel 1, (b) steered channel 1, (c) the multi-speed channel. All other channels are active with the PIN currents as indicated.

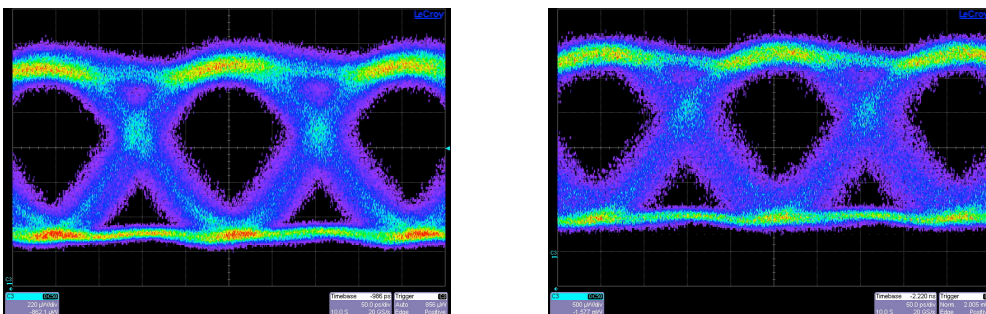
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The 8-bit DAC is used to set the VCSEL modulation current. The setting of each DAC is accomplished by sending appropriate commands to the command decoders in the DORIC. To enable operation in case of a failure in the communication link to the command decoder, we have included a power-on reset circuit that will set the VCSEL modulation current to 10 mA upon power up. Furthermore, we have included a test mode that allows bypassing of the DAC to directly set the modulation current via a wire bond pad. This functionality will not be implemented in the final design.



**Figure 4:** VDC block diagram. In the final design, there will be one less input than output, i.e. if one of the VCSELs malfunctions, the LVDS signal will be transmitted via the spare VDC/VCSEL.

In the prototype VDC, the power-on reset circuit functions properly, supplying a VCSEL modulation current of  $\sim 10$  mA upon power up. We can steer the signal received via the test port to the spare VDC/VCSEL. In addition, we can set the DAC to control individual VCSEL currents. All four channels run error free at 5 Gb/s with bit error rate of  $< 5 \times 10^{-13}$ , including the spare channel with the signal routed from the other LVDS inputs. Figure 5 shows the eye diagrams of the optical signal in one channel and the signal routed from a spare channel. It is evident that the eye is “open” but more improvement is desirable for better operating margin.



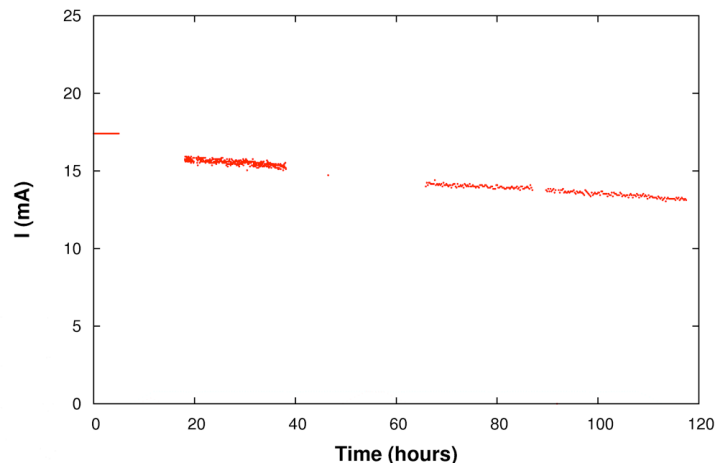
**Figure 5:** Eye diagram of the optical signal in a VDC channel (left) and the signal routed via a spare channel (right). The signal is measured with a 4.5 GHz optical probe.

#### 4. Radiation hardness

Two chips were packaged for irradiation with 24 GeV/c protons at CERN in August 2010 to evaluate the radiation hardness of the devices. Each chip contained 4 channels of drivers and receivers. The total dose received was  $1.7 \times 10^{15}$  protons/cm<sup>2</sup> (46 Mrad). All testing were electrical to avoid complications from degradation of optical components. The remote location required the use of long cables which limited the testing to low speed. We observed little degradation of devices.

In the 2008 irradiation with the previous version of the VDC, we observed significant decrease in the current consumption and the output drive current. The degradation was due to the fact that the current mirror in the driver circuit used thick oxide technology with a mix of PMOS and NMOS transistors in order to produce sufficient voltage to drive a VCSEL. Consequently the circuit was sensitive to the different threshold shifts of the NMOS and PMOS after irradiation, which is larger in the NMOS than in the PMOS. We used PMOS transistors only in the present design and the decrease in the drive current is now quite modest (Figure 6).

There are a total of 126 SEU hardened latches per 4-channel chip which could be upset by traversing particles. During irradiation we monitored both the amplitude of the VDC drive currents and the signal re-routing functions for possible SEU. We observed 13 occurrences of an error in these functionalities during 71 hours of irradiation in one chip and a similar SEU rate in the other. This corresponds to a SEU cross section of  $\sim 1 \times 10^{-16}$  cm<sup>2</sup>. The particle flux is  $\sim 3 \times 10^9$  cm<sup>-2</sup>/year at the opto-link location. This implies a SEU rate of  $\sim 3 \times 10^{-7}$ /year/link. Obviously this is quite acceptable.



**Figure 6:** Current in the 25  $\Omega$  resistor driven by a VDC as a function of time during the irradiation. The dose at the end of the irradiation is  $1.7 \times 10^{15}$  protons/cm<sup>2</sup>.

#### 5. New 12-Channel DORIC and VDC

We have designed an improved version of the chips based the experience gained from the 4-channel DORIC and VDC. Each new chip containing 12 channels with the outer two channels reserved as spare as shown in Figures 7 and 8.

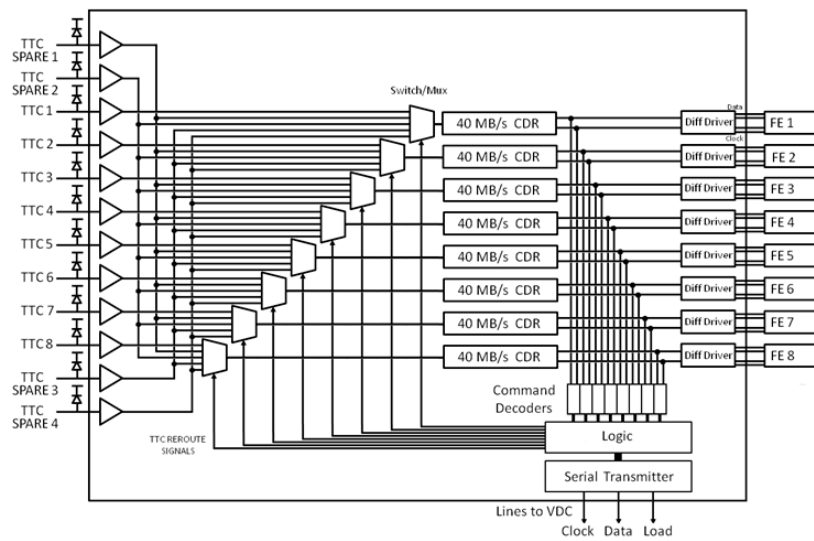


Figure 7: A 12-channel version of the DORIC.

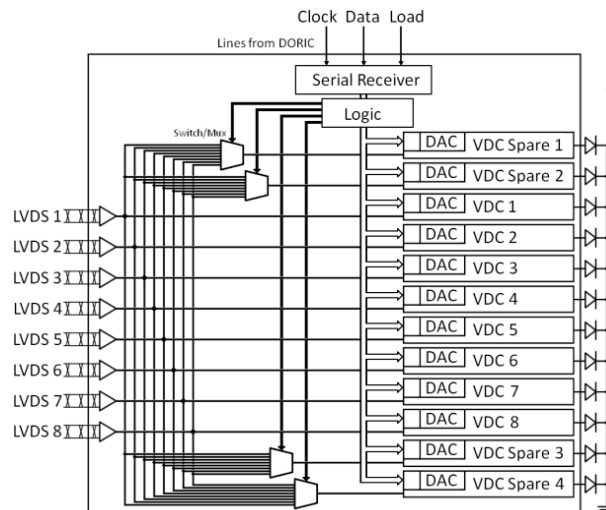


Figure 8: A 12-channel version of the VDC.

As mentioned previously, the DORIC chip, and the DAC and LVDS receivers within the VDC chip are designed to operate with a 1.5 V supply while the VCSEL driver stage within the VDC is designed to operate with a 2.5 V power supply. In the upgrade scenarios currently being proposed, only one service line is available to deliver DC power to the opto-board. In response to this we developed a PMOS LDO to generate 1.5 V from the 2.5 V rail. The LDO is adjustable via an external resistor network and is capable of delivering 1000 mA at 1.5 V. The LDO is contained within the DORIC. Both the DORIC and VDC have been submitted for fabrication in May and we expect the delivery of the chips in the summer.

## 6. Summary

We have successfully fabricated 4-channel driver and receiver ASIC arrays in the 130 nm CMOS process for use in the optical link upgrade. The receiver properly decodes the bi-phase



marked input stream with low PIN current and the driver can operate a VCSEL up to  $\sim 5$  Gb/s. The added functionalities are also successful, including redundancy to bypass a broken VCSEL or PIN channel, individual control of VCSEL current, and power-on reset circuit to set all VCSEL currents to a nominal value. The ASICs were irradiated to a dose of 46 Mrad with 24 GeV/c protons. The observed modest degradation is acceptable and the SEU rate is negligible. We have submitted a 12-channel version incorporating the lesson learned from this submission.

### Acknowledgments

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- [3] F. Faccio, personal communication, 2007.