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Development of Readout System for Double-sided Silicon Strip Modules

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The inner tracker of the ATLAS detector will be replaced at the future upgrade to keep the performance at high luminosity operation. We have developed the super-module integration concept based on double-sided silicon strip modules. A super-module consists of twelve double-sided modules, each of these having 80 readout ASICs. Each chip has 128 readout channels, thus a total of 122880 channels per super-module. Since the number of readout strips becomes very large to keep the hit occupancy at an acceptable level, the data readout is one of the key issues. We have developed a readout system based on the Soi Evaluation BoArd with Sitcp (SEABAS). The SEABAS processes the data from the super-modules by means of an FPGA (User-FPGA) and transfers data to a computer via Ether-net with SiTCP protocol, a technology to realize direct access and transfer the data in the memory of the User-FPGA from the PC by utilizing TCP/IP and UDP communication with a dedicated FPGA. We developed the firmware and the software for the SEABAS, together with the readout hardware chain, and established basic functionality for reading out the super-module.

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1. Introduction

The ATLAS experiment at the Large Hadron Collider (LHC) at CERN will be upgraded after 2022 for high luminosity operation at LHC. The target of integrated luminosity is 3000 fb^{-1} with a peak instantaneous luminosity of 5×10^{34} $cm^{-2}s^{-1}$. During the upgrade, all the inner tracker, currently consisting of the Pixel detector, Semi-Conductor Tracker (SCT), and Transition Radiation Tracker (TRT) will be replaced. The TRT will be replaced by a new SCT or by a tracker made with some other new technologies. For the upgrade of the SCT, we have developed new double-sided silicon strip modules based on the super-module concept.

In the super-module concept, twelve double-sided silicon strip modules are mounted in a local support structure as shown in Fig. 1. One module is composed of two n-in-p silicon strip sensors glued to a central Thermo-Pyrolitical-Graphite (TPG) baseboard [1, 2]. The sensor has 1280 strips and the pitch is 74.5 μm. The strip length is 2.4 cm, which is one fifth of the length of the current ATLAS SCT (12.4 cm). Four hybrids, two per module side, are bridged on top of the facings through a carbon-carbon sheet underneath the flex circuit so that the hybrids remain electrically and thermally decoupled from the silicon sensors. The new SCT will be constructed with about 500 super-modules.

In the prototype modules for the future tracker, each hybrid has 20 Atlas Binary Chip Next (ABCN) front-end chips [3]. The current version of the ABCN chip is produced by IBM with 0.25 μm technology. The chip handles the readout of 128 strips with a binary architecture and it is conceptually very similar to the ABCD3TA chips used in the current ATLAS SCT [4]. In the analog part, there are a pre-amplifier, shaper and differential discriminator for each readout channel. The binary data at the discriminator output is latched at every clock cycle to the input register and then buffered in a 256-cell (6.4 μs) pipeline. Upon the reception of a L1 trigger, the data corresponding to three consecutive bunch-crossings is output serially. The data output rate is 40 or 80 MHz, selectable from outside by sending the corresponding command signals to the chips.

Before sending the data to the DAQ system, data from two links of 10 ABCN chips is multiplexed by a Buffer Control Chip (BCC). The BCCs are produced with 0.25 μm Taiwan Semiconductor Manufacturing Company (TSMC) process [5] by The MOSIS Service [6]. Since the data from the ABCN chips comes at 40 or 80 MHz, the data is multiplexed and output at 80 MHz or 160 MHz. In our current design, two BCCs are mounted on one BCC board, which also allows to

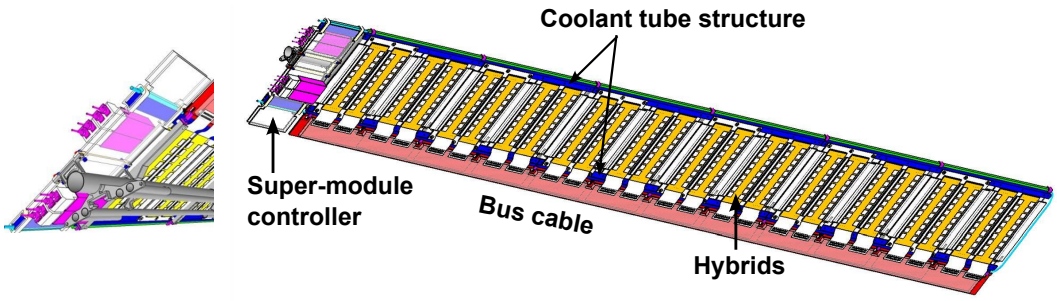

Figure 1: Schematic image of the super-module.

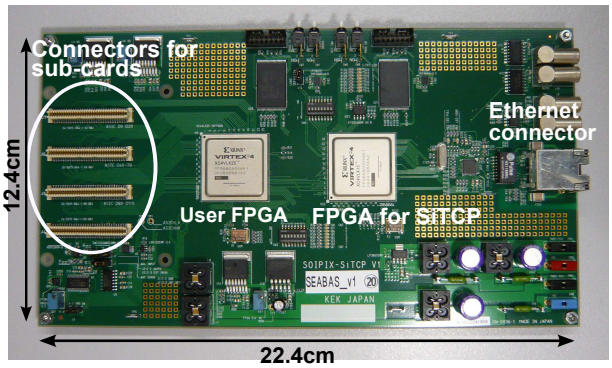

Figure 2: SEABAS.

distribute the power for two hybrids.

We have developed the first reduced scale super-module prototype with eight (instead of twelve) double-sided silicon strip modules. There are 81920 readout strips with 640 ABCN chips and 16 BCC boards. In the super-module, the number of the readout strips becomes very large to keep the hit occupancy at an acceptable level. For that reason, data readout is one of the key issues. We especially need to transfer data to a PC with high transfer rate (above 100 Mbps), however, special technical knowledge is usually necessary to use devices for high speed data transfer like Ether-net communication. Based on a Soi Evaluation BoArd with Sitcp (SEABAS) [7], we have designed a DAQ system that allows to handle such devices without special skills.

2. Soi Evaluation BoArd with Sitcp (SEABAS)

The SEABAS has been developed as a DAQ board for a general purpose tests of chips (Fig. 2). Its size is 12.4 cm $\times$ 22.4 cm. The SEABAS has 4 connectors to attach user-designed sub-cards to interface devices with specific readout chip. 65 MHz 12 bit Analog-to-Digital Converter (ADC), a four channel 12 bit Digital-to-Analog Converter (DAC), and NIM I/O ports are also prepared for easy tests of the chips while they are not used in our application. The SEABAS has two FPGAs for User-FPGA and SiTCP [8]. Data from the chips is processed with a User-FPGA and transferred to a computer via Ether-net with SiTCP protocol.

SiTCP is a technology to realize direct access and transfer of the data in the memory of User-FPGA from the PC by utilizing TCP/IP and UDP communication with a dedicated FPGA. The data transfer speed of TCP/IP communication is 100 Mbps (1 Gbps for the latest version of the SEABAS). UDP communication is used for slow control due to its slow operation clock of 500 kHz. In SiTCP, First-In First-Out (FIFO) memory devices are prepared to store the data from the User-FPGA and PC for TCP/IP communication. In order to use TCP/IP, users only have to send/read data to/from the FIFOs in SiTCP. UDP communication is realized by using registers associated with their addresses. SiTCP adopts the minimum protocol set required by a PC for communication by using standard OS socket functions without special tuning. These specifications of SiTCP allow users to focus on only the development of firmware in the User-FPGA without taking care of technical issues of communication with the PC.

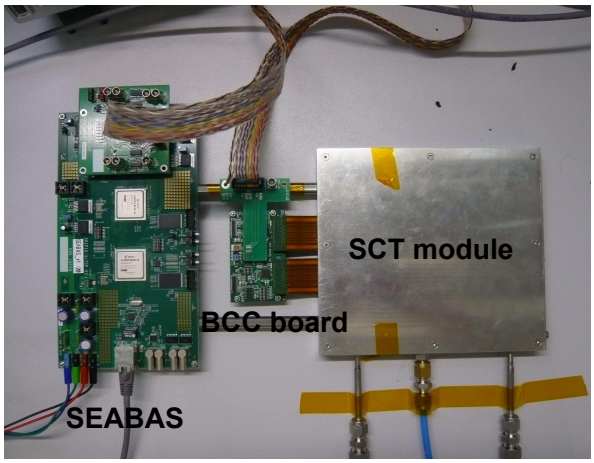

Figure 3: SEABAS DAQ system for a single double-sided silicon strip module.

3. SEABAS DAQ system

We have developed DAQ system for the super-module prototype by using a SEABAS. As the first step, the system for a single double-sided silicon strip module was developed as shown in Fig. 3. Two hybrids of the module top-side are connected to a BCC board, which is linked with a sub-board on the SEABAS. In this system, we have 5120 readout strips corresponding to 40 ABCN chips.

To operate the DAQ, we have developed the firmware implemented in the User-FPGA on the SEABAS and the software used to operate the DAQ system with the PC. Both the firmware and software are designed to be available for the super-module prototype without major modification. The firmware has two parts. One is a circuit block to send signals necessary to configure and operate the ABCN chips, where the bit patterns are defined in the software. TCP/IP is used to send the bit patterns for the configuration and operation of the ABCN chips. On the other hand, configuration of the BCCs and SEABAS functionality is done by using UDP.

The other part in the firmware is the block to read data from the ABCN chips and store it into FIFOs, where 32 FIFOs are prepared in the firmware to read 32 hybrids in the prototype. Once the specific header part of output data from the ABCN chips is detected, the readout block starts to store the data into the FIFOs and stops when it finds the trailer part of the data. After the whole block of data is stored into the FIFOs, it is sent to PC with TCP/IP.

Both the data reception and data decoding are done simultaneously in the software, and the hit information is extracted and stored event by event into a ROOT data-file [9]. The data analysis is done off-line within the ROOT framework.

Since the control bit-patterns and the decoding routines are implemented in the software, the DAQ system is available for operation and data readout of any front-end chips only with minor modification of the firmware.

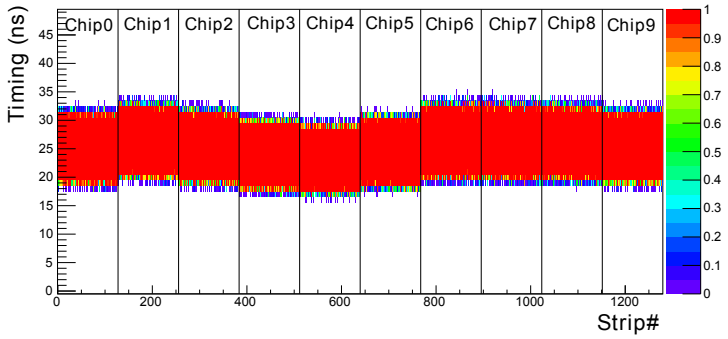

Figure 4: Occupancy plot of strip v.s. timing to select three bits in 256 bits of the binary pipe line for 10 ABCN chips, where timing in the vertical axis shows time before reception of level-1 triggers. In the plot, the timing of 0 corresponds to 2.8 μs before reception of level-1 triggers. The color axis shows the hit efficiency when 100 calibration pulses are injected.

4. Performance test

The performance of the single double-sided silicon strips module was evaluated by using SEABAS DAQ system. For this test, we applied 250 V to the double-sided silicon strip sensors. The data output rate from the ABCN chips was set to 40 MHz, therefore, the multiplexed data from the BCCs is 80 MHz. It was confirmed that the results are compatible with the readout rate of 80 MHz for the ABCN chips, i.e., 160 MHz readout rate of multiplexed data from the BCCs. All the measurements were done by using calibration pulses generated with the ABCN built-in internal calibration circuitry.

At first, we tried to adjust the timing to select which timing part of hit information in the binary pipeline is output. In the ABCN chips, hit information is stored in the binary pipeline whose total length is 256 bits, corresponding to 6.7 μs latency time. After obtaining a level-1 trigger, only three bits in 256 bits of the pipe line are output as the hit information. For that reason, it is necessary to adjust the timing to select the three bits in the pipe line. Figure 4 shows the hit occupancy plot for 10 ABCN chips, where timing in the vertical axis shows the time before reception of level-1 triggers. In the figure, the timing of 0 corresponds to 2.8 μs before reception of level-1 triggers. The calibration pulses were input about 3 μs before the level-1 triggers in this measurement and the hit occupancy became 1 at that timing. The occupancy plots were made as a function of the timing for each chip, then, the rising edge (t_{up}) and falling edge (t_{fall}) were determined to have 50% hit efficiency where 6400 (128 strips $\times$ 100 pulses $\times$ 0.5) hits are observed for 100 calibration pulses without dead strips. Finally, the timing were set to $t_{\mathrm{up}} + (t_{\mathrm{fall}} - t_{\mathrm{up}})/4$.

We evaluated the gain of each readout channel in the ABCN chips by measuring the output voltage for input charge of 0.52, 1.00 and 1.52 fC. The threshold scan was performed for the three input charges. Fitting the threshold curves with the error functions, the output voltage was determined as the threshold voltage to have 50% hit efficiency. Then, the gain was extracted by fitting plots of input charge v.s. output voltage with linear functions. We obtained the average gain of about 110 mV/fC.

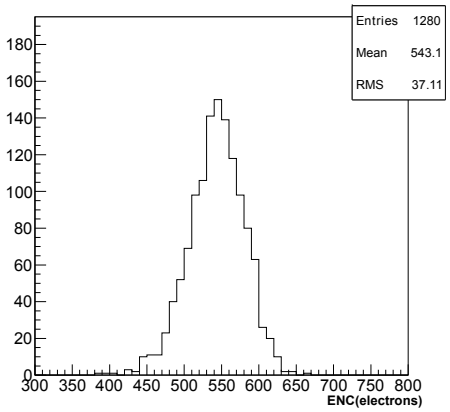

Figure 5: Histogram of the noise values for 10 ABCN chips.

The equivalent noise charge (ENC) was evaluated at the input charge of 1 fC. The threshold curves for each readout channel were fitted with error-functions. The ENC was evaluated from the standard deviation in the error-function, dividing it by the gain obtained in the previous measurement. The average ENC was around 550 electrons as shown in Fig. 5, while that of the ABCN chip only is 375 electrons.

These measurement results are reasonable, comparing to the reference values. For that reason, we conclude that SEABAS DAQ system works properly for readout of the single module.

5. Super-module prototype

We have developed the super-module prototype as shown in Fig. 6, where four double-sided silicon strip modules are already mounted [10]. Eight modules will be finally installed with 640 ABCN chips and 16 BCC boards. The digital voltage for the ABCN chips is provided by prototype SM01C DC-DC converters [11]. Three different service buses have been produced and are used in the prototype. The data-bus is used to derive the common LVDS signals to control both the ABCN chips and BCCs, and to receive each multiplexed data stream coming from up to 16 BCCs. A high-voltage bus supplies bias voltage to each sensor individually and low-voltage bus is used for powering the DC-DC converters. The high and low voltage is operated with NI-LabVIEW based controller. Two sets of the three different service buses are used for top and bottom side in the prototype. The Super Module Board (SMB) is used as an interface board between the data-bus and DAQ system. Two ADCs [12] are also mounted on SMB to monitor temperature of each hybrid. The temperature information is provided as 12 bit values, converting voltage from thermistors (SEMITEC 103KT1608-1P [13]) attached on each hybrid. SEABAS DAQ system will be used for the performance check of the prototype.

6. Summary and Conclusions

We have developed super-module concept for the inner tracker upgrade of the ATLAS detector,

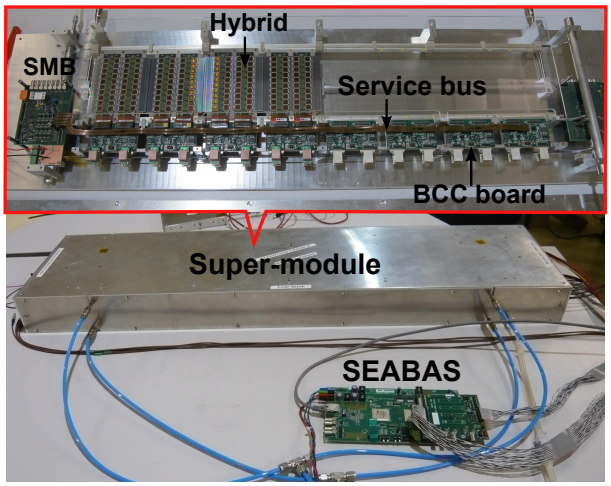

Figure 6: Super-module prototype. In the picture, four double-sided silicon strip modules are already mounted.

based on double-sided silicon strip modules. In this concept, one super-module has 122880 readout strips. Since the number of the readout strips becomes very large to keep the hit occupancy at an acceptable level the data readout is one of the key issues.

We have developed a readout system based on the SEABAS. The SEABAS processes the data from the super-modules with User-FPGA and transfers data to a computer via Ether-net with SiTCP protocol. SiTCP is a technology to realize direct access and transfer of the data in the memory of User-FPGA from the PC by utilizing TCP/IP and UDP communication with a dedicated FPGA. We developed firmware and software for the SEABAS, together with readout hardware chain. For the readout test with the single module, SEABAS DAQ system gave excellent results.

We have developed the super-module prototype with eight double-sided silicon strip modules and 81920 readout strips. The DAQ system has to read data from 32 hybrids (32 BCCs). SEABAS DAQ system is ready to read data from the prototype and will be used for the performance check.

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