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Status of ASIC readout for the prototype Si-W electromagnetic calorimeter

Elmaddin Guliyev

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Abstract

High channel density and space restrictions required that the front end electronics integrated into the active elements of calorimeter. For that purpose novel readout chain base on Application-Specific Integrated Circuit (ASIC) designed for the Electromagnetic Calorimeter for the future International Linear Calorimeter experiment. In this paper, the performance study of ASIC with injected charge is presented.

1 Introduction

Particle Flow Algorithm (PFA) required the achieved jet energy resolution. After the decay of short lived particles, about 60% of the jet energy is carried by charged particles (hadrons), 30% by photons and remain 10% by neutral hadrons [1]. PFA technique is going to measure the hadrons momentum by tracking detectors, photon energy in Electromagnetic Calorimeter (ECAL) and neutral hadrons are obtained from the Hadron Calorimeter (HCAL) [2]. Therefore the performance of the calorimeter is directly proportional the ability of particle flow technique. Using the PandoraPFA particle flow reconstruction algorithm it has been shown that the jet energy resolution about on 3% can be achieved for jet energies in the range 100 - 1000 GeV. From the detailed study of simulations ECAL transverse segmentation 5x5 mm^2 with approximately 30 longitudinal samplings are optimized. The requirements of good segmentation in transverse and longitudinal direction brings to utilize the ECAL with tungsten absorber and silicon pad sensors (Si-W ECAL) [3]. The silicon pad sensor signals are processed by Application-Specific Integrated Circuits (ASICs).

2 ASIC readout for electromagnetic calorimeter

High channel number and density and space limitation required that the front-end electronics should be integrated into the active elements of the ECAL. The detector signals are processed close to silicon pad sensors by ASICs, which handle 64 individual channels. In addition, the ASIC could be fulfill the requirements according to physics program. The requirements are described as follows:

* large dynamic range;

on behalf of the CALICE Collaboration

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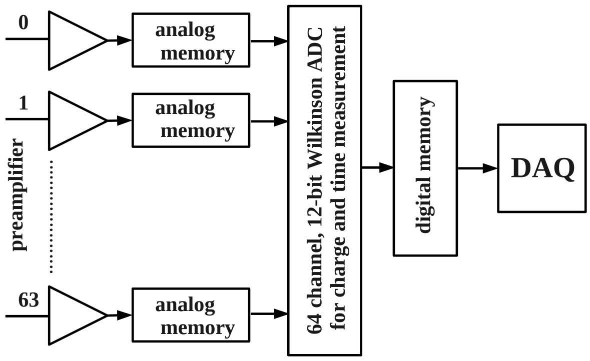

Figure 1: Global overview of designed SKIROC chip

* low noise;
* low power consumption;
* large number readout channels;
* small size;

The designed ASIC for read-out of Si-W calorimeter called SKIROC - Silicon Kalorimeter ReadOut Chip. The input charge from 0.5 MIP up to 2000 MIP (MIP-Minimal Ionizing Particles). The chip has been fabricated using a AMS 0.35 μm SiGe technology [4]. Each channel is made of a variable-gain low-noise charge sensitive preamplifier adjusted by dual gain shaper - one with gain 1 and the other with a gain 10. The measured charge stored 15 switch capacity array (SCA) and can be digitized by 12-bit Wilkinson ADC.The schematic overview of the ASIC chip is presented in Figure 1.The digitized data will stored to 4 kB RAM [5].

3 Si-W ECAL prototype tests

To test the performance of the front-end electronics base on SKIROC chip, a series of measurements within the Si-W ECAL protoype was performed. The test setup consisted of a single slab of very-front end electronic card (FEV8), four SKIROC chip, silicon pad sensor (5x5 mm^2), detector interface (DIF). In addition, the setup has adjusted link data agregator (LDA) and clock card creator (CCC). The block diagram of experimental setup presented in Figure 2.

The silicon pad sensors glued bottom side of FEV8 and four SKIROC chip top side. For the debug of chip status the converter board placed between FEV8 and DIF. From the figure one can see the test input of external signal via lemo connector is also adjusted on the converter board. The DIF itself connected

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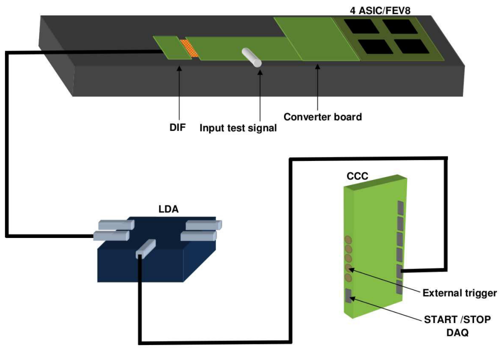

Figure 2: Block-diagram of experimental setup for performance measurements.

to link data aggregator (LDA) via using high definition multimedia interface (HDMI) cable. LDA will help to accumulate the data from several DIFs (in our case one DIF connected). In addition, the LDA will share the programming functionality in many other ASICs. For the acquisition of collected data the LDA output coupled directly to data creator card (CCC).

3.1 Study with injected charge

The performance of preamplifier and digitization of SKIROC chip is investigated injecting a charge from the pulse generator. The injected charge has a rectangular shape with 1μs length and 50 Hz rate. Injected charge pre-amplified and shaped inside the chip. To save the amplitude of this signal track and hold switch is going to do it. Figure 3 describe the analog output of pre-amplified and shpaed signal, input signal and hold position where the falling edge holds the amplitude. While performing of a scan of hold position for fixed level of injected signal one can reconstruct the shape of signal output of analog memory of SKIROC chip.

When the position of hold signal is adjusted to baseline level of the pre-amplified and shaped signal, the data acquisition started to digitize the noise level. From that point we can study the noise level of preamplifier/shaper. The noise level for all four chip is measured around 5-7 ADC Count. There is one issue is also, minimization of cross-talk between the channels. The noise correlation between the channels is shown in Figure 4. The correllation factor between the neighboring channels is less than 20

After the performing the study of noise level, test for linearity between injected charge and digitized value is performed. The gain set to 3.2 pF for feedback capacitance for shaper. The position of falling edge of hold signal optimized 220 ns. From the Figure 5 we can see linear behaviour for between digitized and injected charge values.

After the performing of digitazition, the gain of shaper started to study. As mentioned the gain of preamplifier/shaper is determined from the feedback capacitance. For that performing study the trigger threshold and hold position fixed (the both parameters same as previous tests) and gain varied. From the

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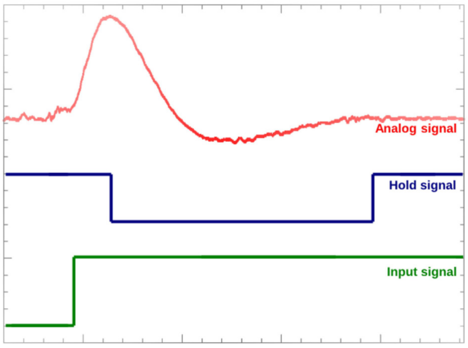

Figure 3: The output signal from the analog memory of SKIROC (red), hold signal (blue) and injected impuls (green).

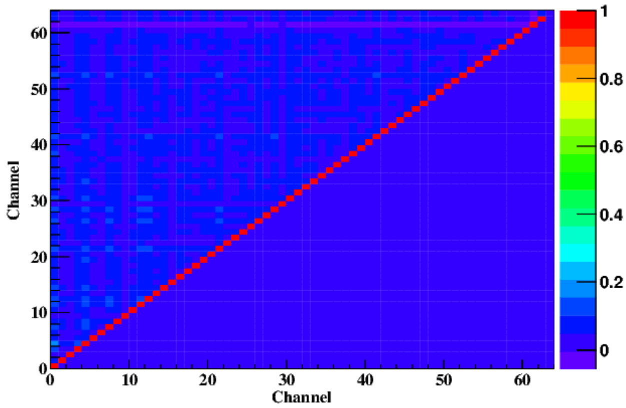

Figure 4: Correlation between neighboring channels.

Figure 6 we can see the output signal level from the chip is linear for different gain value.

4 Conclusion

The feasibility of the ASIC readout has been demonstrated using a Si-W ECAL protoype. Using the rectangular pulse generator the prototype ASIC-SKIROC chip tested. The performed test to show that we can use the Si-W ECAL protoype with ASIC readout in test beam.

References

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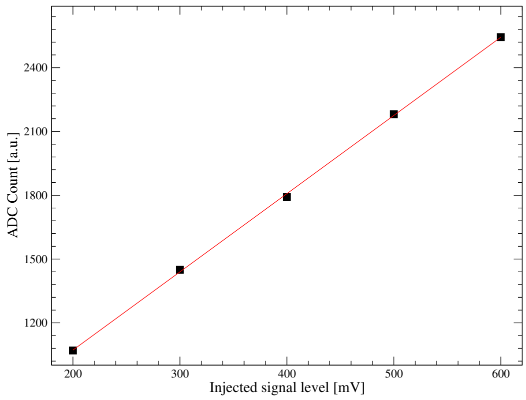

Figure 5: The digitized signal from the SKIROC output for different injected charge values.

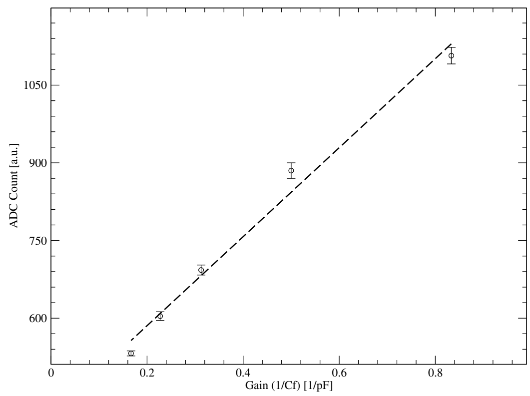

Figure 6: Digitized signal for different gain.

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