

## Electronics and data acquisition systems for the RPC based INO ICAL detector

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The India-based Neutrino Observatory (INO) [1] collaboration is planning to set up a magnetised Iron-CALorimeter (ICAL) detector to study atmospheric neutrino oscillations with precise measurements of oscillations parameters. ICAL detector will use 50kton iron as target mass and about 28,800 single gap Resistive Plate Chambers (RPCs) of  $2\text{m} \times 2\text{m}$  in area and operated in the avalanche mode as its active detector elements. About 3.6 million electronic channels need to be instrumented. ICAL's Data Acquisition (DAQ) system records - on receiving a physics trigger signal, pattern of RPC pickup strips hit by the charged particles which are produced in the neutrino interactions as well as their precise time of crossing the active detector elements. Besides, the DAQ system also performs a number of slow control and monitoring functions in the background. The proposed scheme and status of development of electronics and DAQ systems for the ICAL detector are presented.

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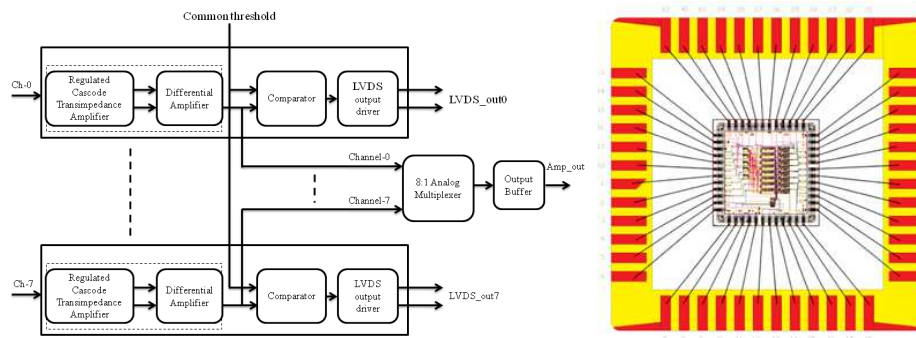
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## 1. Overview

An ICAL RPC with a pickup strip pitch of 30mm, will have 128 analog signals to be readout and processed - 64 positive and negative polarity signals from each plane. Architecture of the ICAL's electronics and DAQ systems is based on designating the RPC as the minimum standalone unit. Front-end electronics, signal digitisation, data acquisition as well as data transfer functions - are all implemented on the RPC unit itself. While the front-end electronics is mounted on two orthogonal edges, common processing electronics - called RPC-DAQ module, is located at one corner of the RPC unit. Digitised data is transmitted to back-end through a network interface built on the RPC-DAQ module.

## 2. Front-end electronics

ICAL front-end electronics comprises of a preamplifier followed by a leading-edge discriminator stage. This is implemented by an indigenously developed 8-channel ASIC, which is shown in Figure 1. Each of the channels comprises of regulated cascode trans-impedance amplifier, differential amplifier, common threshold comparator and LVDS output driver. Amplifier's output of a selected channel is also available across a  $50\ \Omega$  output buffer through a builtin analog multiplexer.



**Figure 1:** Block diagram of the front-end ASIC chip (left) which is fabricated in a CLCC48 package with a chip area of  $13\text{mm}^2$  (right).

Some of the important features of the front-end ASIC are shown in the Table 1.

## 3. RPC-DAQ module

The RPC-DAQ module which is located on the RPC unit, handles all the signal processing, data acquisition and data transmission functions of an entire RPC unit. It is designed to acquire the following information using the incoming RPC strip signals:

- Event data on each trigger received asynchronously from the trigger system: (a). Strip hit data as a 128-bit pattern (1-bit per strip), (b). Relative time of strip hits with respect to the global trigger signal, (c). Time over threshold information, obtained from the timing data of both the edges of strip hit pulses and (d). RPC strip's pulse profile.

|                        |                                |
|------------------------|--------------------------------|
| Process                | AMSc35b4c3 (0.35 $\mu$ m CMOS) |
| Input dynamic range    | 18fC - 13.6pC                  |
| Input impedance        | 45 $\Omega$ @350MHz            |
| Amplifier gain         | 8 $\mu$ V/ $\mu$ A             |
| 3-dB Bandwidth         | 274MHz                         |
| Rise time              | 1.2 ns                         |
| Comparator sensitivity | 2mV                            |
| LVDS drive             | 4mA                            |
| Power per channel      | 20mW (approx)                  |

**Table 1:** Important features of the front-end ASIC

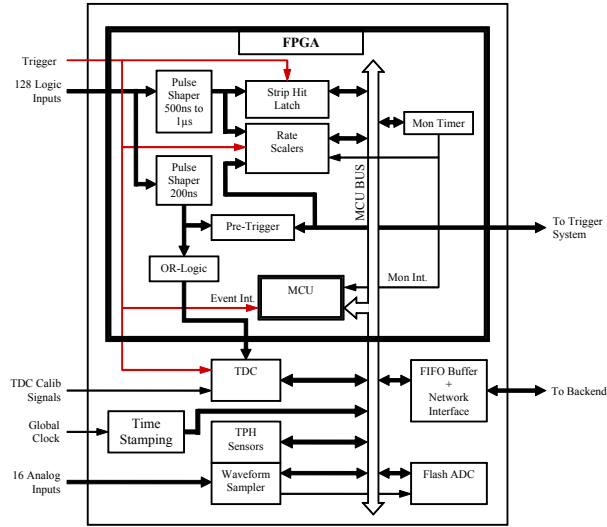
- Monitor data collected over programmable periodicity: (a). Background rates of the individual RPC strips. Groups of strips are multiplexed and their rates counted sequentially in order to minimise the number of counters needed, (b). Ambient parameters such as temperature, barometric pressure and relative humidity and (c). RPC bias voltage and current.

Main functional components of the RPC-DAQ module (Figure 2) are enumerated below:

1. Pulse shapers: One per readout channel for strip hit latch and another for generating pre-trigger logic.
2. 128-bit strip hit latch
3. 16 rate scalers, one per each block of 8 RPC strip signals.
4. Pre-trigger logic to generate trigger primitives from an RPC unit.
5. Micro Controller Unit (MCU) for overall control, data acquisition and communication with back-end
6. Data network interface.
7. 16-channel Time-to-Digital Converter (TDC).
8. 16-channel waveform sampler.
9. Ambient parameter monitor (TPH).

First six components listed above will be implemented inside an FPGA. Since deployment of an FPGA is inevitable, considering the flexibility it offers, it is decided to implement as many components as possible inside the FPGA. This will result in reduced board space and eliminates the inter-component connections, besides reducing the power consumption of the module.

The RPC-DAQ module receives the following inputs or signals: (a). Unshaped discriminated RPC signals from 128 strips in LVDS form, (b). 16 analog RPC signals, each signal is a summed or



**Figure 2:** Functional block diagram of the RPC-DAQ module

multiplexed output of 8 amplified RPC strip signals, (c). Global trigger signal from an autonomous ICAL trigger system, (d). Global clock for synchronising the time stamping on each RPC-DAQ module, (e). TDC calibration signals from the back-end and (f). TCPIP connection to back-end for command and data transfer.

### 3.1 Timing device

The passage of a charged particle through an RPC produces a signal, whose timing with reference to a global trigger provides information about the directionality (upward or downward) of the tracked particle. In order to record the timing of the RPC signal, a TDC with least count of about 200ps is necessary. Other requirements of the ICAL timing device are summarised in the Table 2.

|                           |   |
|---------------------------|---|
| Number of channels        | 8 or 16                                       |
| Least count               | 200ps   |
| Dynamic range             | 2 $\mu$ s (essential), 32 $\mu$ s (desirable) |
| Number of bits            | 14 (essential), 18 (desirable)                |
| Type                      | Common stop                                   |
| Hits                      | Single hit (essential), multi hit (desirable) |
| Double hit resolution     | 5-10ns  |
| Readout buffer size       | 128 words (maximum)                           |
| Signal and control inputs | LVDS and LVTTTL respectively                  |
| DNL/INL                   | 100ps (typical)                               |

**Table 2:** Requirements of the ICAL timing device

A number of FPGA-based and ASIC timing chips [2], which are capable of meeting these requirements, are already available. While efforts are underway within the collaboration to design

our own device, we plan to use one of the available chips for the ICAL prototype detector.

### 3.2 Pulse shape monitoring

A provision is being made to digitise a group of multiplexed or summed RPC strip pulse profiles using a waveform sampler. This data is useful for systematic study and monitoring of RPC pulse profiles. It may also be used to correct offline, for the time-walk in the timing data. It may be noted that time-walk is an unavoidable feature of the leading-edge discriminators, like the one used in ICAL. If the analog signals from 8 strips are multiplexed, then it is possible to record the waveform sampler data during the monitoring cycle. If on the other hand the analog signals from 8 strips are summed, then it is possible to sample the signals during the event recording cycle. DRS4 [3] chip is currently being evaluated for its possible deployment for this purpose.

### 3.3 Network interface

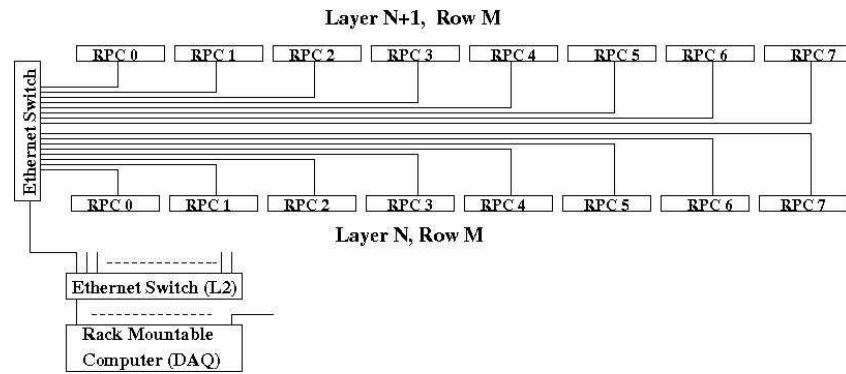
Assuming that waveform sampler is configured to acquire data in the event recording cycle, the event data record size is about 256kbits. Therefore, for an event trigger rate of 1Hz, 256kbits of data needs to be handled every 10 secs. During this time the background monitor cycle, operating over 10 secs cycle time will accumulate about 1kbits of data. Both these data need to be transmitted to the backend using an appropriate data interface built onboard RPC-DAQ module. Implementing a network interface requires the following components (layers): (a). The protocols, viz., TCP (Transport Control Protocol), IP (Internet Protocol), ARP (Address Resolution Protocol), UDP (User Datagram Protocol), (b). Media Access Control (MAC), (c). Media Independent Interface (MII), (d). The physical layer (PHY), the actual medium and (e). A user application that runs on top of these protocols which carries out the data transfer.

Two approaches are currently being considered for implementing a TCP/IP based network interface for the RPC-DAQ module. In the first approach, MAC and MII can be implemented in an FPGA, while an additional ASIC is required to implement the physical layer. As for the TCP/IP protocols, these are not available as synthesizable IP cores for FPGA, and therefore have to be implemented in the software running under an operating system. Running a TCP/IP stack in the software is an extremely CPU cycle consuming task. Also since an operating system needs to be installed, it further increases the resource requirement and the system complexity. In the second approach, a hardware TCP/IP single chip (W5300 from Wiznet [4]) solution is used. This chip incorporates full hardware logic of the TCP, IP, UDP protocols as well as 10/100 Ethernet MAC and PHY layers. This approach frees the micro controller unit from the network interface functions.

## 4. Network configuration

As discussed in the previous section, since network interface incorporates an embedded CPU, TCP/IP stack and Ethernet interface, the RPC will become a network device. The entire ICAL detector will thus become a large Ethernet LAN, suitably segmented, with RPCs as LAN hosts together with the DAQ computers (Figure 3).

On receiving the master trigger, the onboard CPU of every RPC acquires, processes and stores the data in its onboard memory. A bank of networked RPCs will be assigned as clients of a DAQ computer that acts as a server. This scheme exploits the fact that the estimated data rates of ICAL



**Figure 3:** Schematic diagram of the proposed ICAL network configuration

will be significantly smaller than the bandwidth provided by gigabit Ethernet components. We see that for our purpose UDP based communication holds advantage over TCP.

The advantages of this networked RPC scheme over the VME scheme are many. The entire DAQ hardware will be much more compact and elegant. We are immune to worries about VME falling out of favor of manufacturers in future. Apart from the embedded CPUs on RPCs, the DAQ will entirely comprise of Ethernet switches and computers, all of which keep getting cheaper and better with time. In the VME scheme, communication between RPCs and backend VME is a major area of design and development. This is circumvented in the network scheme because of the numerous options of standard network protocols and high level computer language support readily available in public domain. Besides, this network scheme also offers an elegant way for monitoring of RPC health and slow control of onboard parameters. The onboard CPU can be assigned the background task of monitoring its own signals and periodically sending the results to servers. Standard protocols like SNMP can be used by servers for slow control of parameters on RPC.

## 5. Summary

Pilot production of the front-end ASIC chips were tested with the RPC detector. Based on these performance studies, first revision of the chip is already taken up. Most of the functional blocks inside the FPGA were implemented using Cyclone II family FPGA from Altera. NIOS II soft processor from Altera is also integrated in the the FPGA. W5300 from WIZnet is also successfully interfaced to the NIOS II processor and configured. Work is progress for establishing data communication using TCP/IP between the processor and a host.

## References

- [1] INO Collaboration, <http://www.ino.tifr.res.in/ino/OpenReports/InterimReport.pdf>
- [2] M. Mota and J. Christiansen, IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1360-1366, 1999; Y. Arai, et al., IEEE Trans. Nucl. Sc., vol. 49, no. 3, pp. 1164-1169, 2002
- [3] <http://drs.web.psi.ch/>
- [4] <http://mct.de/download/wiznet/w5300.pdf>