

A sampling ADC as a universal tool for data processing and trigger application

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For the particle identification via energy loss measurement and algorithm tests for the PANDA Straw Tube Tracker (STT), a new dedicated FPGA firmware for the 16 channel 240 MHz sampling ADC has been developed. New FPGA firmware can simultaneously deliver charge, amplitude and time informations which are extracted from the detector signals. It also provide the possibilities to record raw signal information in an intelligent oscilloscope mode. The sampling ADC with the new FPGA firmware has scaler capabilities and can be used for self triggering and as a coincidence unit.

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1. Introduction

The developments presented in this article were driven by the investigation of the particle identification via energy loss measurement (dE/dx) with the straw tube tracker for the PANDA experiment [1], [2]. In the PANDA experiment at the HESR antiproton storage ring (HESR) of the Facility for Antiproton and Ion Research (FAIR) in Darmstadt (Germany), the central Straw Tube Tracker (STT) which consists of more than 4600 straw chambers will provide information about traversing particles trajectories, momenta and energy loss.

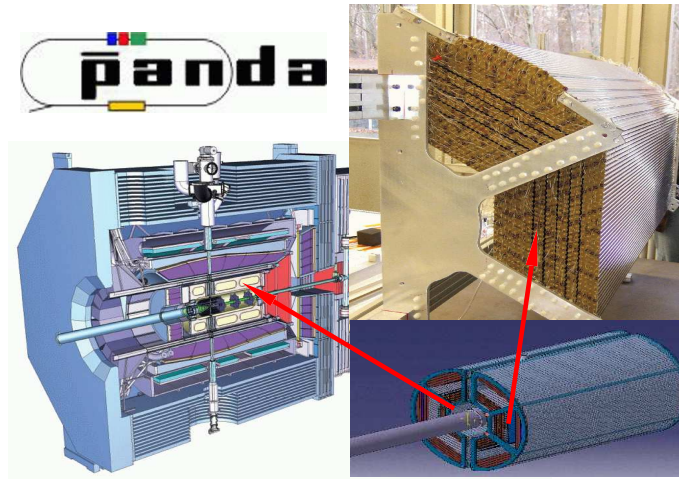


Figure 1: Left: The Straw Tube Tracker as central tracking detector of the PANDA experiment. Top right: Two assembled sectors of the STT. Bottom right: Illustration of the STT comprising six sectors.

The sampling ADC gave us the possibility to develop various analysis techniques by processing the collected raw signals (off-line mode) and to test them with much higher statistics using implemented FPGA algorithms (on-line mode) with the same device and without changing experimental setup.

The experimental setup consists of 120 straw tubes of 150 cm length divided in four layers of sixteen straw each. For the data readout up to eight 240 MHz 16 channel sampling ADCs were used together with several F1 chip based 64 channel TDCs [3], [4].

The measurement of charge, time and signal amplitude, the oscilloscope mode, as well as the trigger and counting capabilities of the sampling ADC will be described in this article.

2. The sampling ADC

The 240 MHz 12 bit sampling ADC (Fig.2) is divided into four input sections, each controlled by an input FPGA (XC3S1500). The input sections are connected to the main control FPGA (XC3S400). Each input section has four channels. For the signal digitization the LTC2242 ADC chip is used. The possible signal range is $\pm 0.4V$. The ADC data are collected continuously in a ca. $12\mu s$ long ring buffer. The size of the analysis window is ca. $6\mu s$ and allows to collect data up to ca. $6\mu s$ before the trigger. The position with respect to the trigger and the length of analysis windows can be set independently for each input section. The sampling ADC has two additional

inputs, an analog signal input for the common test signal and a digital trigger input which can be used for triggering of the module or as 2 ns resolution TDC. For module controlling and data transfer the Low-Voltage Differential Signaling (LVDS) bus is used. For module supply and hosting dedicated crates with LVDS backplane are used. One crate can host up to 15 modules. It is possible to mix sampling ADC with 64 channel TDC based on GPX or F1 chips. The 160 MHz and 80 MHz versions of the sampling ADC [6] are used as QDC at the WASA at COSY experiment [7].

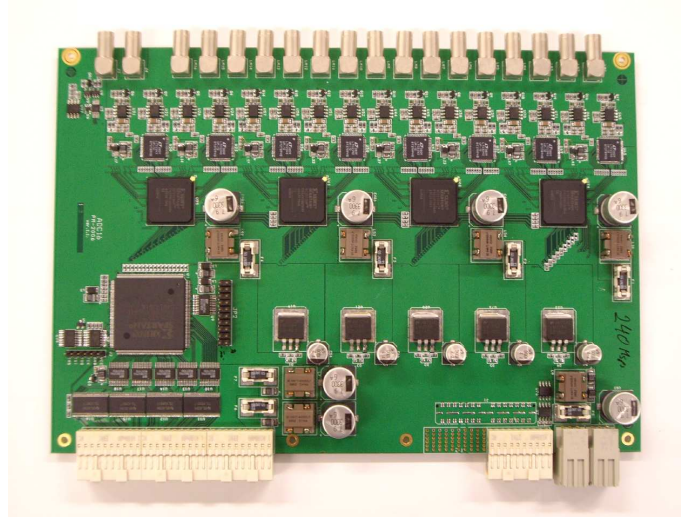


Figure 2: The 240 MHz sampling ADC. The 16 signal inputs, test pulse input and trigger input are on the top and LVDS bus connectors on the bottom are visible.

3. Charge measurements

In this section the "direct" energy loss measurements methods which are implemented on the FPGA are described.

Different methods exist to measure the deposited energy. Examples of direct measurements are collecting the signal charge on capacitors or integrating the signal shape over a certain time. Indirect measurements are for example the Time over Threshold (ToT) method [8] or cluster counting [9]. For direct charge (energy) measurements based on signal integration, the stability of the base line is crucial. Therefore the baseline value is continuously updated by the input FPGA.

3.1 Fixed gate QDC

The signal integration inside fixed gate is a standard method used in QDCs. The principle is presented in Fig. 3. The length and position of integration gate are defined with respect to the trigger and the signal is integrated within that gate. This method is simple to implement but the results strongly depend on the selected position and length of the integration gate.

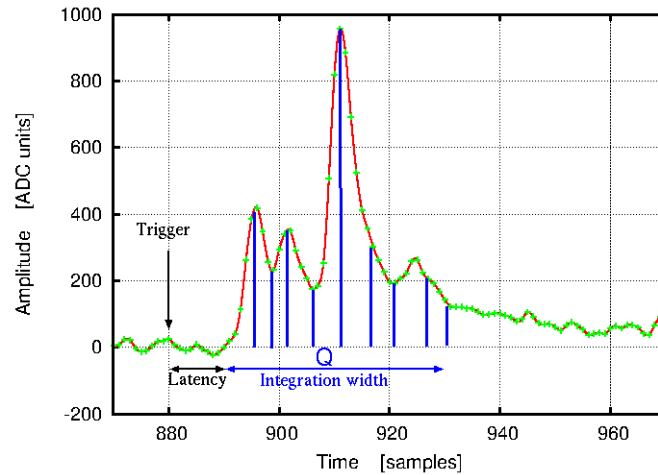


Figure 3: Fixed gate integration principle.

This method does not work well when the start position relative to the trigger and the signal length vary and in the case of pile-ups.

3.2 Pulse search QDC

To reduce the influence of the varying start position and length of the signal, the so called pulse search method was implemented using the complete signal shape information. In this method, the start position and the length of the search window with respect to the trigger are defined and the algorithm implemented in the FPGA search for all pulses within this window. The integration of each pulse starts at the detected pulse begin and stops after the selected integration length. If the algorithm detects the begin of a new pulse before the end of the set integration length, the running integration ends and a new integral starts. The information from all these integrals (Q1 to Q4 in Fig. 4) are available in the output data together with a pile-up indication.

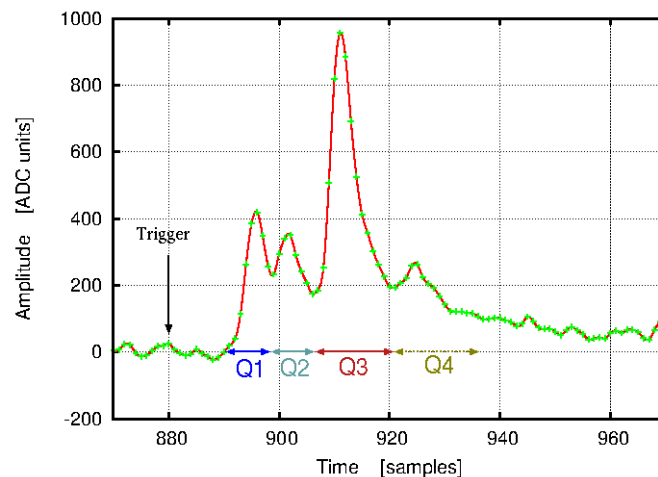


Figure 4: Pulse search mode of the sampling ADC. The begin of the integration is independent of the trigger time.

4. Time and amplitude information

The algorithms implemented in the input FPGAs provide time information from different kinds of discriminators and information about position and shape of the found pulses. The pile-up detection is also implemented.

4.1 Time information — discriminators

The first implemented discriminator algorithm uses the level crossing method (LC) (green arrows in Fig. 5). The time when the pulse crosses a selected level is determined. The times of both the rising and the falling part of the pulse are available. In addition, a pulse width criterion is implemented which allows to exclude pulses which are too narrow. Using the level crossing times, one can obtain ToT information for each pulse.

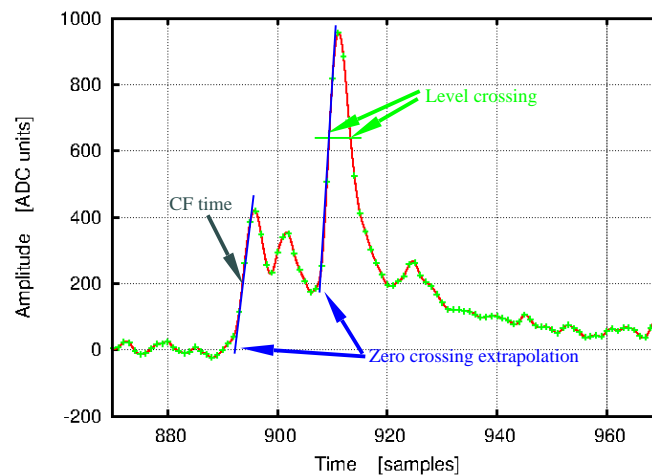


Figure 5: Different time extraction methods.

The second discriminator technique implemented in the FPGA is the zero crossing discriminator (ZC) (blue arrows in Fig. 5). In this case a linear extrapolation is made to find the time of the "zero" crossing of the signal. The (LC) and (ZC) discriminators exhibit time walk with changing signal amplitudes. One well known method to overcome this is the use of a constant fraction discriminator (CFD) which is the third available discriminator type. The implementation of the CFD is fully digital. The pulse search algorithm determines the pulse maximum and then the crossing point of the rising part of the pulse with the line representing the selected fraction of the pulse maximum is determined. The fraction can be set in 1/16 steps of the amplitude height. The (CFD) time is determined only for the first pulse in a "cluster", (ZC) and (LC) are also available for pile-up pulses and are additionally marked. Additional time information can be obtained from the pulse shape information as described in next subsection.

4.2 Pulse information

The amplitude and the time information of the pulse minimum and maximum are provided for each pulse which is found by the pulse search algorithm (blue and gray arrow on Fig. 6). The

time of signal maximum has a large time walk but in case of signal pile-ups these can be used as additional information to improve timing and energy determination.

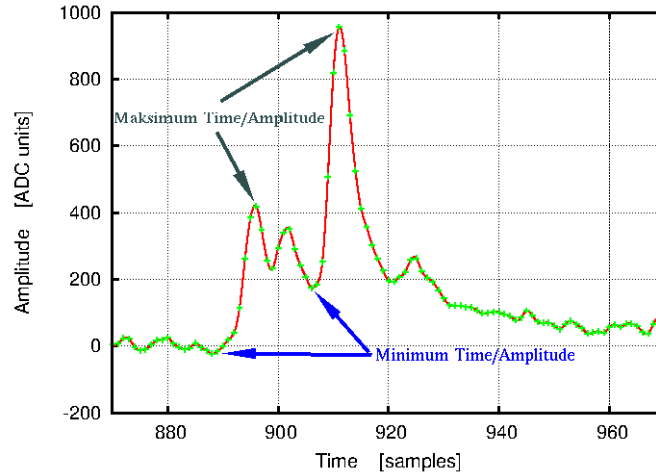


Figure 6: Different pulse information provided by the FPGA algorithms.

5. Oscilloscope mode

Different options for raw signal recording are implemented in the FPGA firmware. A "raw" mode which changes the sampling ADC module to a simple 16 channel oscilloscope and an "intelligent" mode with advanced signal selection mechanisms.

5.1 Raw mode

In the raw oscilloscope mode all signal points inside a defined window are available in output data (Fig. 7). The maximal length of such window can be up to ca. $6\mu s$ and the window can start up to ca. $6\mu s$ before the trigger.

For testing and controlling of the extraction algorithms, the so called "raw cycle" mode is implemented – the raw signals (if pulses were detected) are available every "n" events in the output data.

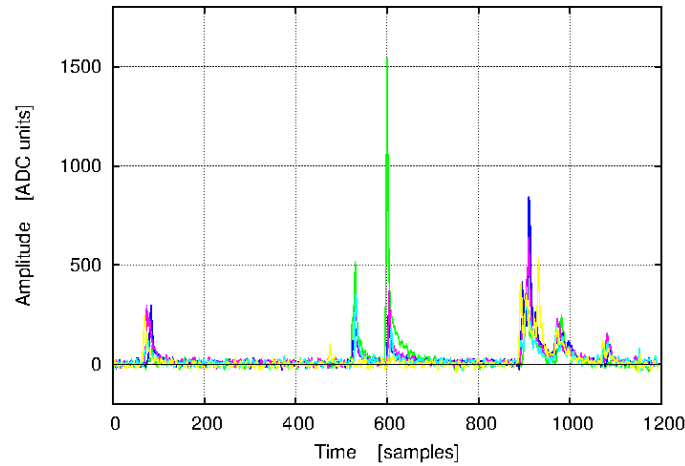


Figure 7: Example of raw data collected with the sampling ADC.

5.2 Intelligent mode

The intelligent oscilloscope mode was developed to effectively collect raw signals for off-line analysis. In this mode the raw signals are collected only if selected criteria are fulfilled. The implemented criteria are: charge obtained by fixed gate QDC (Q2 on Fig. 8), signal level crossing with minimum width criterion (Level on Fig. 8) and pulse charge found in search window (Q1 on Fig. 8). These three criteria can be combined. This approach significantly reduces amount of the output data.

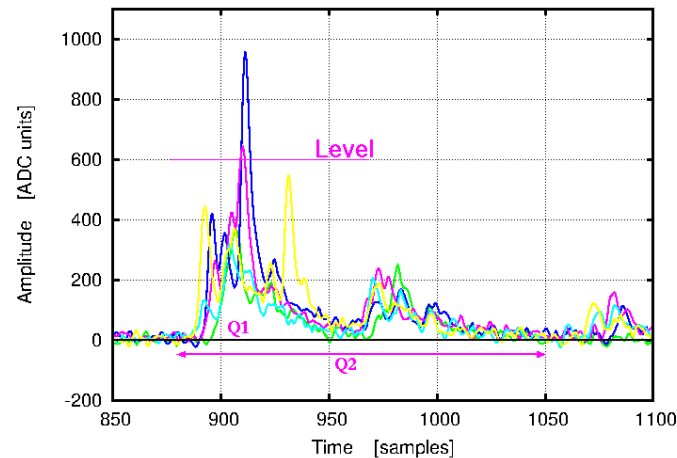


Figure 8: Selection criteria implemented in intelligent oscilloscope mode.

6. Trigger decisions and counting

In the modules FPGAs a complex trigger logic and counters were implemented. For logic part (coincidence and counters) second, independent of the (LC) discriminator, level with minimum width criterion is used. The output of the coincidence logic can be used for "self" triggering of the

full system. The coincidence output is also available on the internal connector and can be used for e.g. external oscilloscope triggering. The discrimination level, signal output width and length can be set individually for each input channel.

6.1 Coincidence and trigger capabilities

The scheme of the lookup table based coincidence logic is presented in Fig. 9. For each input section (A to D) one 16 bit lookup table is defined which allows all possible logic functions in each section. The outputs of each input section (L1 to L4) are then combined in a control FPGA using another 16 bit lookup table. The main logic output can be used as an external coincidence output or for triggering applications.

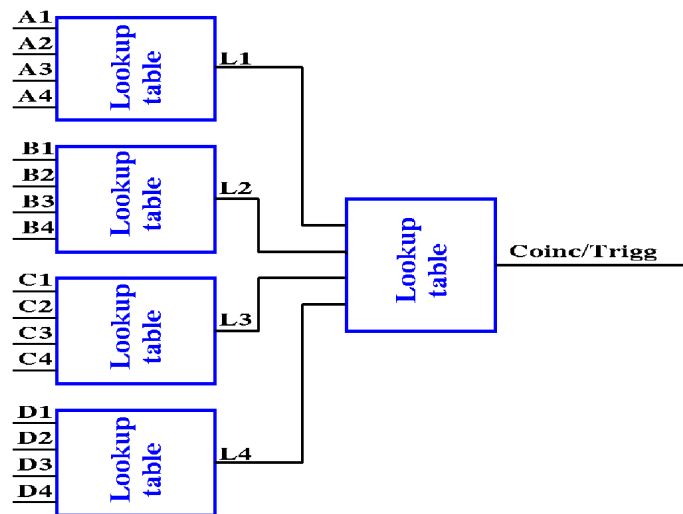


Figure 9: Scheme of the lookup table based coincidence logic.

6.2 Counter

The counters are implemented as 120 MHz free running 32 bit counters. Two modes of operation are foreseen. The first mode is synchronous with the main trigger and appends the counter value to the event output data every "n" events. The second mode is an asynchronous mode for on-line analysis in which the counters can be readout independent from the main trigger and can be used for e.g. on-line display. Synchronous and asynchronous mode can be run in parallel.

7. Summary and outlook

The use of a fast 240 MHz 12 bit sampling ADCs for data collection and pre-analysis allowed us to efficiently develop methods which can be used for particle identification by means of energy loss measurements with the PANDA STT [10]. The different possibilities implemented in the firmware of the sampling ADC helped us to test and optimize data analysis techniques and detector setups. The sampling ADC has many different functions (TDC, ADC, QDC, counter, logic and trigger unit) implemented in a single unit and therefore it is a very useful data acquisition tool for detector tests and the development of algorithms for data analysis based on real detector signals.

A huge advantage of such a broad functionality is that the need of signal splitting between the detector and the data acquisition hardware is strongly reduced. ADC, QDC, TDC and counter are working on the same signal input. In the near future, functions which take the "cluster" structure of the straw tube signals into account will be available; better selection of informations included in the output data and a new baseline algorithm will be implemented. Modification for using sampling ADC with the phoswich like detectors are investigated.

Acknowledgments

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References

- [1] W. Erni et al., Physics Performances Report for PANDA (2009), arXiv:0903.3905v
- [2] M. Kotulla et al., Technical Progress Report for PANDA—Strong Interaction Studies with Antiprotons (2005)
- [3] P. Kulesa, *PoS* , BORMIO2011:010,2011.
- [4] K. Pysz, *PoS* , PoS BORMIO2011:011,2011.
- [5] P. Wintz, *AIP Conference Proceedings*, Volume 698, (2004) 789
- [6] H. Kleines et al. *IEEE Trans.Nucl.Sci.*53 (2006) 893
- [7] K. Fransson, *Int.J.Mod.Phys .A*225(2007) 570
- [8] P. Gagnon, ATL-INDET-2004-008
- [9] G. Cataldi et al., *NIM A*386 (1997) 458
- [10] Technical Design Report for the PANDA Straw Tube Tracker