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Scribing-Cleaving-Passivation for High Energy Physics Silicon Sensors

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Future High Energy Physics (HEP) experiments will include silicon sensors because of their superior resolution, tracking, and vertexing performance. Silicon sensors normally have an inactive region along the perimeter of the sensor. This inactive area on the perimeter contains the guard rings that protect the active area from electrical currents and damage caused in the manufacturing of the device. These inactive areas can significantly degrade the performance of the closely arranged sensors for HEP instrumentation and need to be minimized. In this paper, we describe a scribe, cleave, and passivate (SCP) technique for the fabrication of slim edges. We present results for n- and p-type sensors with different sidewall passivations. The leakage current depends strongly on the type of sidewall passivation for p- and n-type silicon. Furthermore, the amount of sidewall damage does change the leakage current. We tested different scribing techniques. Some scribe damage can be removed by an additional silicon etch step after cleaving. We also applied the technique to large area n-type single-sided strip detectors and are working towards a fully automated process.

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PoS(Vertex 2012)020

1. Introduction

Silicon particle detectors provide significantly improved performance capabilities over other sensor technologies and consequently are of great interest for High Energy Physics (HEP), medical, space and homeland security applications. Due to the penetrating nature of these rays/particles and the small size of a single sensor element, large arrays of silicon detectors must be tiled and stacked to provide the needed sensitivity and spatial coverage. The typical silicon detector requires relatively large dead areas on the perimeter called guard rings which protect the active area from electrical currents and damage caused by traditional dicing methods. These dead areas can significantly degrade the performance of the arrayed system and need to be minimized. We are working on minimizing these dead areas with a new procedure for dicing the sensors and passivating the sensor's sidewall, called a slim edge process. Rather than the conventional cutting with a diamond blade, a process for scribing and cleaving was developed that generates a silicon wall with a very low defect density. A sidewall passivation technique using atomic layer deposition (ALD) with a fixed interface charge replaces the need for guard rings. The fixed interface charge leads to a controlled voltage drop along the edge of the sensor, the same way a guard ring structure provides a controlled voltage drop.

For the IBL (Insertable B-Layer) of the ATLAS experiment, the inactive area should not exceed 225 μm at the sensor edge [1]. Future HEP experiments will most likely require even smaller inactive areas. The IBL specification can be met by implementing an "active edge", as already proposed by Parker [2, 3]. An active edge is an implanted junction at the sensor's sidewall. The edge is made by a DRIE (deep reactive ion etch) process. The fabrication of an active edge has one main drawback: It requires a support wafer during DRIE etching and ion implantation (making it incompatible with a double-sided process). The handle wafer can not easily be removed. The fabrication process of an active edge is expensive and difficult to apply for mass production. We developed a processing method for "slim edges". This process sequence does not require an implantation step and can easily be applied to various silicon sensors.

1.1 Scribing and Cleaving

We are working on slim edges for finished sensors (dies or wafers) with front and back side metallization. One essential step is to replace regular blade dicing. (Dicing is sometime also called die singulation). Traditional blade dicing uses diamond covered blades. This technique is well-established and has been used for decades. Blade cutting leads to micro-cracks and chipping at the die edge, leaving a $\sim 100\mu$m wide damaged region. As the semiconductor industry moves to thinned dies, the problems with chipping become more problematic. Furthermore, semiconductor devices using modern low-K dielectrics can not be diced by blade cutting. Alternative dicing techniques with reduced edge damage for die singulation include: (1) dicing before grinding, (2) laser dicing, (3) plasma dicing, and (4) mechanical scribing and cleaving.

Dicing before ginding (DBG) reverses the usual process of fully dicing the wafer after grinding. In DBG, first the wafer is half-cut with a special dicing saw. Then, die singulation occurs when the wafer is thinned below the level of this cut. This technique is not applicable for semiconductor sensor production because front and back side processing is needed; DBG allows only regular front side processing.

PoS(Vertex 2012)020

In recent years, several **laser-dicing** technologies have been developed, each having specific characteristics for a separation process. The main dicing technologies that have become most common in the semiconductor industry are ablation laser dicing and sub-surface dicing. ("Stealth dicing" from Hamamatsu Photonics K.K. (HPK) is a sub-surface process.) In ablation laser dicing, the wafer material is removed by irradiation of laser pulses which locally generate a combination of melt and vapor. The vapor pressure drives the molten material out of the wafer generating an opening also referred to as kerf. This technology is predominantly used for dicing through the whole wafer substrate thickness, even backside metallization. Depending on the application (wafer material, thickness, throughput, and die size), the laser type is chosen. Main laser process parameters that determine the interaction of laser light with the wafer material are wavelength, pulse duration and power. The size of the Heat Affected Zone (HAZ), the thickness and appearance of the resolidified molten material (recast) and the resolidified particles forming debris all depend on these parameters. This paper presents results for laser-scribing and full laser-cutting for HEP sensors. Scribing is a partial cut, and laser- cutting is a full through-cut. Scribing requires a cleaving step (see details below) to fully singulate the dies. This is true for all scribing methods, not only laser-scribing.

Plasma dicing is a plasma based etch step, similar to DRIE etching. Overstolz et al. used a deep reactive ion etching (DRIE) to release MEMS devices from on SOI (silicon-on-oxide) wafer [4]. The DRIE etch stopped at the buried oxide interface. A HF (hydrofluoric acid) vapor etch releases devices from the SOI carrier by underetching the buried oxide. Panasonic Corp. developed a full dry etch system, Plasma Dicer PSX800, that etches silicon with an ICP (induction coupled plasma) [5]. The wafer is cut/etched with a SF_6/O_2 gas mixture. This gas mixture allows for an anisotropic through-etch etc. We used plasma-etching to etch a shallow scribe line. Plasma dicing, as used in the semiconductor industry, is a full through-cut.

Mechanical scribing and cleaving has proven to be very efficient for volume III-V-compound semiconductor laser manufacturing [6, 7]. GaAs or InP optoelectronic devices are routinely scribed and cleaved. The classical example is the fabrication of laser diodes; a mirror-like sidewall is traditionally formed by cleaving the semiconductor wafer. The cleaved surface has very low damage and is nearly atomically flat, making it ideal for laser applications. III-Vs are brittle and tend to cleave easily following the $\{111\}$ crystal planes. Furthermore, the wurtzite crystal structure helps during cleaving, generating an anisotropy for different planes. For GaAs lasers and LEDs based on sapphire, yields up to 90-98 % have been reported. Fully automated systems exist and are made by different vendors, e.g. Dynatex and Loomis Inc. We used such system for scribing and cleaving silicon HEP sensors.

Silicon is more difficult to cleave than a III-V semiconductor, because cracks in silicon can propagate along the $\{110\}$ and $\{111\}$ crystal planes. We used scribe-and-cleave for silicon sensors. The cleaved surface can be mirror-like and have virtually no defects, just like the III-V compound semiconductors. We used three scribing techniques: laser-, plasma-, and diamond-scribing. During diamond scribing, a scribe force is applied to the wafer by the diamond-tipped scribe tool and generates a ductile groove and micro-cracks inside the silicon substrate.

PoS(Vertex 2012)020

2. Results and Discussion

The fabricated sensors were first evaluated based on their leakage currents. We measured the leakage currents of the different sensors using a probe station at room temperature. The IV curves were collected by using a Keithley 237 high voltage source measurement unit. We also collected charge collection data for these sensors; these measurements are presented in different publications [8, 9]. A short summary is given below, section 2.5. Furthermore, we are currently evaluating, how irradiation will affect the sidewall passivations and resulting leakage currents, see section 2.6.

2.1 Micro-Fabrication

We processed different n- and p-type diodes and n-type single sided strip detectors (SSSD). The n-type diodes (area of 0.5 cm x 0.5 cm) and SSSDs were part of the GLAST sensor production [10] (Gamma-ray Large Area Space Telescope, now called the Fermi Gamma-ray Space Telescope). The leakage current from the n-type diodes and GLAST baby strip detectors has been extensive documented by the GLAST collaboration. The average leakage current was < 0.75 nA. We also used p-type pad diodes that were manufactured in the context of the ATLAS07 strip sensor development for the ATLAS upgrade [11].

The general process squence was, see Fig. (1) for a schematic: **1.Scribing**. Either top or bottom surface of the sensor needs to be scribed along the lattice orientation. The purpose of the scribe mark is to seed the location of the cleaving plane. The mechanical stress during the cleaving step concentrates at the scribe mark. These technqiues are analogous to the dicing techniques mentioned above. The following technologies have been prototyped and shown to work: a.Diamond scribing, b.Laser-based scribing, c. Etching a trench on the surface with XeF_2, d.Etching a trench on the surface with DRIE. **2.Cleaving**. Mechanical stress is induced on the wafer to separate the die. The stress can take the form of wafer bending or pulling. We have worked with the following technologies: a.Manual cleaving with tweezers, b.Cleaving by industrial machines, for example ones made by Loomis Industries and Dynatex International. These machines frequently possess both the diamond scribing and cleaving functionalities. **3.Sidewall damage removal**. This is an optional step that was found to improve the performance when there is a time lapse between cleaving and passivation, see details below. **4.Passivation.** This is the final step of the processing. The type of sidewall passivation depends on the substrate doping, see [12] for details. As a result, the optimal sidewall passivation leads to a controlled potential drop along the edge due to a fixed interface charge. We found that the use of ALD (atomic layer deposition) alumina layers with a negative interface charge works best for p-type sensors. A PECVD (plasma enhanced chemical vapor deposition) amorphous hydrogenated silicon nitride (H-SiN_X) shows the lowest leakage currents for n-type sensors. A PECVD deposited H-SiN_X layer has a fixed positive interface charge. Similar passivations for p- and n-type silicon are used for solar cells to increase carrier lifetime and solar cell effectiveness [13, 14].

Besides the fixed interface charge, a low trap density is needed. An interface high trap density would lead to a high leakage current. The traps are localized right at the silicon dielectric interface. Hydrogen is often used to passivate traps. Interestingly, the alumina ALD reaction produces hydrogen as a by-product. This hydrogen most likely contributes to the interface properties by passivating defects. Also during H-SiN_X PECVD deposition hydrogen is produced. Since PECVD

PoS(Vertex 2012)020

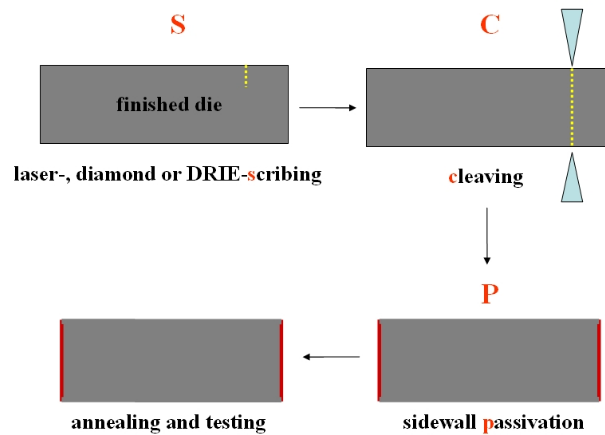

Figure 1: Schematic of the SCP (scribing-cleaving-passivation) process.

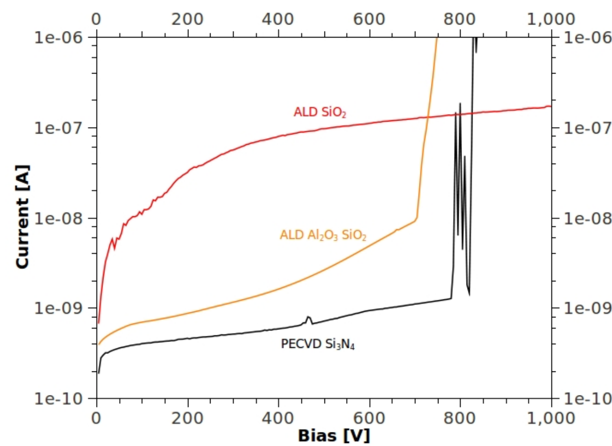

Figure 2: IV curves for different n-type diodes for different types of sidewall passivations.

is not a very conformal deposition method, it's not ideal for covering sidewalls. ALD, on the other hand, is extremely conformal. Hence, we also developed an ALD passivation with a positive interface charge for n-type sensors. A combination of SiO_2 and Al_2O_3 shows low leakage currents. The silicon interfaces with the SiO_2, providing the positive interface charge. The subsequent Al_2O_3 generates the needed hydrogen for the trap passivation.

2.2 N-Type Si

As mentioned above, PECVD deposited H-SiN_X layers can be used for n-type sensors. A disadvantage of PECVD is that the deposition is not very conformal. When PECVD is used, the plasma directs the ion deposition. Since we need to deposit onto the sidewall passivation, PECVD is not a good choice. ALD, on the other hand, is very conformal and ideal for covering sidewalls. Dingemans et al. showed that ALD deposited SiO_2/Al_2O_3 nanostacks have excellent passivation properties for n-type Si [15]. Fig. (2) shows the IV curves for different types of sidewall passivations in our tests. The SiO_2/Al_2O_3 nanostack (2 nm SiO_2 and 50 nm Al_2O_3) shows low leakage currents.

PoS(Vertex 2012)020

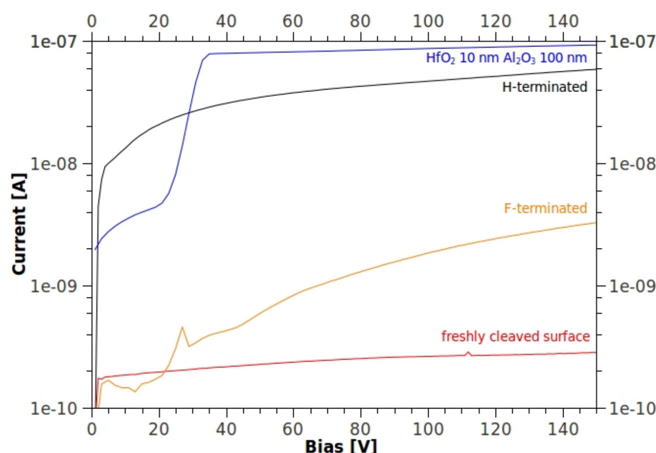

Figure 3: IV curves for different p-type diodes for different types of sidewall passivations.

2.3 P-Type Si

As mentioned above, p-type Si requires a sidewall passivation with a fixed negative interface charge. Aluminum oxide (Al_2O_3) layers, prepared by atomic layer deposition (ALD), have a negative interface charge and provide excellent surface passivation properties on crystalline Si surfaces. ALD-deposited Al_2O_3 is currently the only known dieletric with a fixed negative interface charge. Fixed charge densities, Q_f, up to 10^{13} cm^{-2} are commonly reported. For Al_2O_3 thin films, Q_f is located close to the interface with Si. However, the mechanism that defines Q_f is currently not known [15]. Since ALD is a layer-by-layer deposition technique, Q_f depends strongly on the first few deposition cycles. These inital ALD reactions are a function of the silicon surface termination. Fig. (3) shows IV curves for p-type diodes with different surface termination prior to thermal alumina ALD. A freshly cleaved silicon surface shows the lowest leakage current (only seconds after cleaving in air, the diode was placed into ALD deposition chamber).

A hydrogen H-terminated silicon surface shows a rather high leakage current. Several groups found a thin (1-2 nm) SiO_X layer at the interface of ALD-deposited alumina [15, 16]. This interfacial SiO_X also forms on H-terminated silicon (e.g. after HF, hydrofluoric acid, treatment) [16]. Since silicon oxidizes when exposed to air, HF is commonly used to remove the so-called native oxide. Since a native oxide has a positive interface and a high trap density, an oxide etch is required prior to alumina deposition. We are currently working on ALD deposition conditions that can circumvent the problem with the H-termination and interface oxide formation.

Fig. (4) shows the IV curves for a p-type diodes before and after the SCP process. The leakage current did not change up to 200 V altough the distance to the active area was $< 2\mu$m. The sidewall passivation was alumina and the ALD deposition was done on a freshly cleaved sidewall.

2.3.1 Sidewall Damage Removal

As mentioned above, all scribing methods introduce some silicon damage (much less than blade dicing though). During diamond scribing a scribe force is applied to the wafer by the diamond-tipped scribe tool and generates a ductile groove and micro-cracks inside the silicon substrate. Etch-scribing is done by etching a shallow trench into the silicon. This step can be performed

PoS(Vertex 2012)020

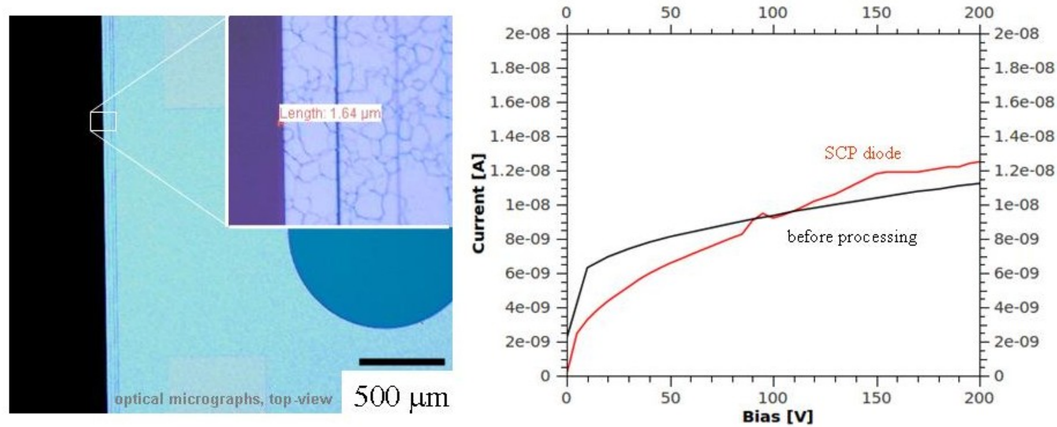

Figure 4: P-type SCP diode with a cut less than 2 μm from active area (optical micrographs). The IV shows an unchanged IV curve up to 200 V.

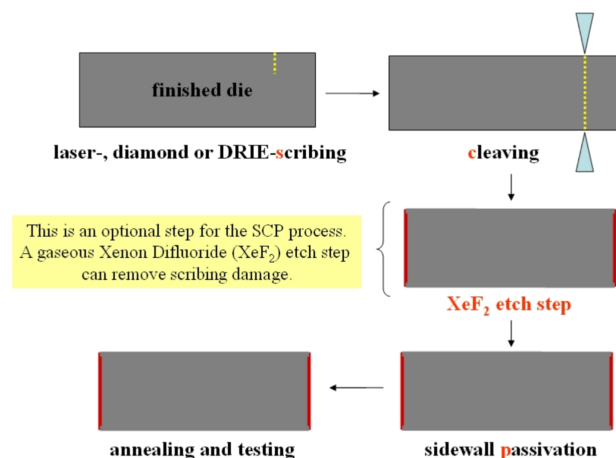

Figure 5: Schematic of SCP process with an optional XeF_2 sidewall etch step.

by a gaseous or reactive ion etch step. The sidewall damage from etch-scribing is rather low, but the step introduces sidewall roughness. During laser dicing, the wafer material is removed by irradiation of laser pulses which locally generate a combination of melt and vapor. Laser-scribing leave a Heat Affected Zone (HAZ). The HAZ consists of resolidified molten material (recast), debris, and micro-cracks.

We found that a gaseous etch step after cleaving can remove some scribe damage. The modified SCP process is shown in Fig.(5). We use a XeF_2 (xenon difluoride) etch with an etch depth of roughly 7 μm to remove the damaged silicon (1 T XeF_2, 30 T N_2, 10 pulses, 30 sec pulse). Since XeF_2 is very selective to silicon, no photo-resist mask is needed.

There is a semiconductor industry equivalent for the sidewall etching step; it's called Die Strength Enhancement (DSE). The finished die needs to withstand mechanical stress during further packaging, e.g. 3-D stacking. Cracks at the die sidewall can lower the die strength and increase the risk of breakage. Die strength enhancement is done with different sidewall treatments including plasma and gaseous silicon etch techniques. Boyle et al. used XeF_2 etching for DSE [17].

PoS(Vertex 2012)020

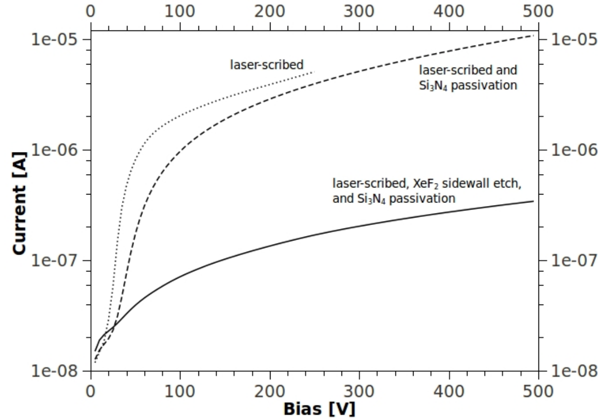

Figure 6: IV curves for different laser-scribed GLAST sensors. The addiational XeF_2 etch significantly reduces the leakage current.

2.4 Large Area Sensors

For large area sensors, we introduce a small etched grove parallel to the strips. To demonstrate the technique, we used GLAST "baby" detector, 1.7 cm x 3.5 cm, 128 strips. The baby sensors have the all features of the full-size detectors.

As mentioned above, dry etching techniques (or plasma dicing) have been used for releasing sensitive MEMS devices and singulating dies. We, on the other hand, only scribe the silicon and do not fully release the devices by dry etching. We used two different methods to etch the silicon: XeF_2 and DRIE-etching (i) We used XeF_2 for etching a scribe line parallel to the silicon strips. XeF_2 etching is very selective and does not introduce any silicon damage. It is well suited for processing silicon sensors with existing metalization and surface passivations. (ii) We also used DRIE etching. Since the plasma contains F and O ions, the silicon and the surface passivation layers must be protected with a photoresist during DRIE. A simple lithography step was used to defined the scribe location. The typical etched scribelines were 5 μm deep and 10 μm wide.

Fig. (7) shows a cross-section SEM micrograph and IV curve of a cleaved sensor with a DRIE-etched scribeline. The silicon sidewall underneath the shallow etched groove shows no visible damage. Furthermore, we used an additional XeF_2 sidewall etch after cleaving to remove any scribe damage. We used a Xetch-3 from Xactic, Inc (20 etch pulses, one pulse at 1 mTorr XeF_2 and 30 mTorr nitrogen for 30 seconds). The IV curve shows low leakage currents up to 1,000 V. The passivation was a SiO_2/Al_2O_3 nanostack, as described in section 2.2.

2.5 Charge Collection Measurements

We performed charge collections measurements for n- and p-type sensors. R. Mori et al. [8] looked into the pulse height distribution of the signals from a beta source with the ALiBaVa system [18]. The sensors were n-type test devices from GLAST/Fermi production [10]. The distance between the bias ring and the edge was 195 μm on these 400 μm thick sensors. The signal distribution on the first and last strips showed a low-amplitude tail due to charge sharing with the bias ring. However, the distributions were quite similar for the strip near the slim edge and the strip near regular (wide) edge. No charge deficiency was found, within 5 percent of the total amplitude.

PoS(Vertex 2012)020

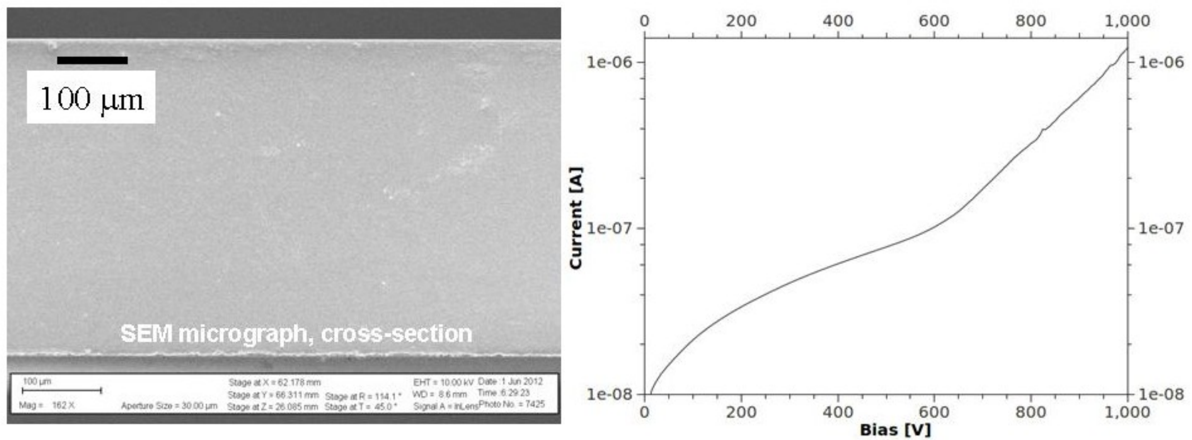

Figure 7: SEM micrograph (cross-section) and IV curve from a GLAST "baby" after SCP.

In another study using a p-type sensor [9], a micro-focused X-ray beam was used to vary the charge injection position on a strip p-type sensor produced by CIS for ATLAS PPS studies [19]. The distance between the bias ring and the edge was 140 μm and the sensor thickness 300 μm. The signals were also read out by the ALiBaVa system. The edge strip did not a show charge deficit compared to its neighbors. The method features an exquisite spatial sensitivity and further studies are planned.

2.6 Irradiation Studies

In our initial attempt to study the radiation hardness of SCP method we have irradiated 12 samples at 4 fluences with 800 MeV/c protons in Los Alamos. The results at higher fluences, 6.8x10^{14} and 5.6x10^{15} p/cm^2, were encouraging. All of these samples showed an increase in the breakdown voltage. However, two lower fluences in the 10^{13}-10^{14} p/cm^2 range shows some samples with improved breakdown, and some with deterioration. Post-mortem examination revealed that the sidewall coating could be damaged by strong mechanical contact, which is one possible reason for the deterioration. To clarify the performance, we have irradiated both n- and p- type diodes at CERN SPS. We will study them as soon as we get them back after cool-down period.

3. Conclusions

This paper decribes the SCP (scribing-cleaving-passivation) technique for slim edge silicon sensors. The technique presented works on full wafers or on a finished die scale. Using this technique, we made slim-edge p-and n-type diodes with extremely low leakage currents (comparable to an active edge). This is important in cases when the amount of passive material at the perimeter of the sensor needs to be minimized. Furthermore, by etching a groove with XeF_2, we successfully transferred the SCP technique to SSSDs. (Cleaving is still done manually but we are working on a full and scalable automated process.) We processed single side strip sensors on n-type Si. A SSSD (1.7 cm x 3.5 cm sensor with 128 strips) with a SCP slim edge at 50 μm showed low level leakage current and > 1,000 V breakdown voltage.

PoS(Vertex 2012)020

References

[1] M. Kocian, et al., *ATLAS Pixel, phase 0 (IDL)*, this proceedings, 2012.

[2] C. Da Via, et al., *3D active edge silicon sensors with different electrode configurations: Radiation hardness and noise performance*, Nucl. Instrum. Methods A, vol. 604, p. 505, 2009.

[3] S. I. Parker et al., *A proposed new architecture for solid-state radiation detectors*, Nucl. Instrum. Methods A, vol. 395, p. 328, 1997.

[4] T. Overstolz, P. A. Clerc, W. Noell, M. Zickar, N. F. de Rooij, *A clean wafer-scale chip-release process without dicing based on vapor phase etching*, IEEE MEMS (2004) 717-720.

[5] K. Arita, *Panasonic's plasma dicing technology*, Suss Report, 4 (2010) 4-7.

[6] K. Wasmer, et al., *Dicing of gallium arsenide high performance laser diodes for industrial applications: Part I. Scratching operation*, J. Mat. Process. Tech, vol. 198, p. 114, 2008.

[7] K. Wasmer, et al., *Dicing of gallium arsenide high performance laser diodes for industrial applications: Part II. Cleavage operation*, J. Mat. Process. Tech, vol. 198, p. 105, 2008.

[8] R. Mori, et.al., *Charge collection measurements on slim-edge microstrip detectors*, J. of Instrumentation 7 (2012) P05002.

[9] R. Bates et al., to be submitted.

[10] T. Ohsugi, H. F.-W. Sadrozinski, et al, *Design and Properties of the GLAST Flight Silicon Micro-Strip Sensors*, Nuc. Instr. Meth. A. 541 (2005), 29.

[11] Y. Unno, For the joint collaboration of the RD collaboration in Japan, *Development of radiation-tolerant silicon microstrip sensor for the ATLAS inner tracker at the SLHC*, Nuc. Instr. Meth. A 623 (2010) 165-167.

[12] M. Christophersen, et al., *Alumina and Silicon Oxide/Nitride Sidewall Passivation for P- and N-Type Sensors*, Nuc. Instr. Meth. A. (2012) in press

[13] B. Hoex, J. Schmidt, R. Bock, P. P. Altermatt, M. C. M van de Sanden, W. M. M. Kessels, *Silicon surface passivation by atomic layer deposited* Al_2O_3, Appl. Phys. Lett. 91 (2007) 112107-112110.

[14] M. Lipinski, P. Panek, S. Kluska, M. Sokolowski, H. Czternastek, *Optimization of SiNx:H layer for multicrystalline silicon solar cells*, Opto-Electr. Rev. 12 (2004) 41-44.

[15] G. Dingemans, et al., *Controlling the fixed charge and passivation properties of Si(100)/*Al_2O_3 *interfaces using ultrathin* SiO_2 *interlayers synthesized by atomic layer deposition*, J. Appl. Phys. 110 (2011) 093715

[16] G. Dingemans, et al., *Status and prospects of* Al_2O_3*-based surface passivations schemes for silicon solar cells*, J. Vac. Sci. Techn. 30(4) (2012) 040802 1-27.

[17] A. Boyle, D. Gillen, K. Dunne, E. F. Gomez, R. Toftness, *Increasing Die Strength by Etching during or after Dicing*, European Patent EP 1 825 507 B1 (2011).

[18] R. Marco-Hernandez and ALIBAVA Collaboration, *A portable readout system for microstrip silicon sensors (ALIBAVA)*, IEEE Transactions on Nuclear Science, VOL. 56, NO. 3, (2009).

[19] M. Beimforde, for the Planar Pixel Sensor Collaboration, *The ATLAS Planar Pixel Sensor RD project*, Nuc. Instr. Meth. A. 636 S8 (2011).

PoS(Vertex 2012)020