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Strip Technology and HVMAPS

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High-voltage particle detectors in commercial CMOS technologies, or HVMAPS, are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution. Thanks to its high radiation tolerance, the HV detectors are seen at CERN as a promising alternative to the standard detector options. In order to test the concept, within ATLAS upgrade R&D, we are currently exploring two detector concepts, the bumpless hybrid pixel detector and the pixelated strip detector, both based on the HV detectors. This paper describes the pixelated strip detector.

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1. HVMAPS - Introduction

The use of segmented radiation sensors in standard CMOS technologies has gained in popularity over the last decade. In commercial applications, CMOS sensors have mostly replaced the previously dominant technology - the CCDs.

The principle of the CMOS pixel-sensors is that the signal charge is attracted to a positively biased n-type doped region (n-well), it is converted to voltage and amplified within the pixel itself. Since the first signal processing steps are performed in the pixels, these sensors are also referred to as the active pixel sensors - APS.

The APS in their original form do not have a full sensitivity across the entire pixel surface, they do not have a 100% fill-factor. The signal charge, generated underneath the pixel electronics, gets attracted by the transistor structures. Such charge losses are not critical when visible light is detected, however they should be avoided in the high-energy physics applications.

In order to solve the problem of the non-ideal fill factor, in recent years, many groups have been working on the development of the Monolithic Active Pixel Sensors (MAPS). This approach relies on the signal generation in the $\sim 15\,\mu$m-thin epitaxially-grown layer underneath the pixels (epi-layer). The pixel electronic is based on n-channel MOS (NMOS) transistors that are placed above the sensitive area, as shown in Fig. 1.

Since the epitaxial layer is lower doped than the p-wells housing the NMOS transistors and the p-type wafer-substrate, it acts as a potential well for the signal-electrons. The only structure with a lower potential for electrons than the epi-layer is the collecting electrode (n-well) itself. Since the epitaxial layer is mostly field-free, the charge collection occurs by diffusion. The existence of the potential barriers significantly reduces the charge losses. In this way it is possible to make compact and cheap detectors with excellent spatial resolution and a perfect fill factor. Unfortunately, MAPS sensors have a few limitations. Not every semiconductor technology has the necessary properties, the charge collection by diffusion is relatively slow and is strongly affected by the radiation damage so that the radiation tolerance is relatively poor.

We have proposed a slightly different way to implement a CMOS pixel sensor. Our structure can be derived from a standard APS by four improvements:

1. **CMOS pixel electronics**, Fig. 2 A: We are using both p- and n-channel transistors inside the pixels. This allows us to implement more advanced pixel electronics than in the case of the standard MAPS - particularly to implement a high-gain charge sensitive amplifier (CSA). Note, that the use of a PMOS (biased in a standard way) in an APS or MAPS pixel would lead to a signal loss. A PMOS transistor is embedded in an n-well that is biased by connecting it to the most positive voltage in the circuit. Such an n-well would compete with the small collecting electrode, and "steal" a part of the signal charge from it.
2. **Two-fold use of the n-well**, Fig. 2 B: In order to avoid charge losses in our structure, we bias the PMOS n-well using a high resistance. The n-well is then used in two ways: 1) as the PMOS substrate and 2) as the collecting electrode. No additional n-well electrode for charge collection is needed. In this way we do not have competitive wells and no charge collection losses happen. The signal amplification occurs in the following way: the electrons collected by the n-well cause a small voltage drop in it. The n-well is coupled to the input of the pixel amplifier. The amplifier amplifies the signal and restores the original n-well

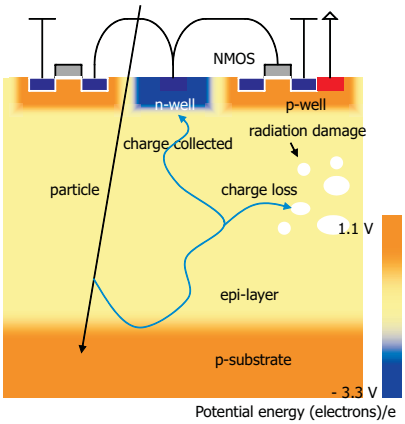

Figure 1: MAPS - cross-section.

voltage. The use of the CMOS electronics allows us to implement an efficient, high-gain, charge sensitive amplifier. A CSA has the property that its amplification does not depend on the detector capacitance. In this way, we can compensate for a higher capacitance of the collection electrode than in the case of MAPS.

3. **Deep n-well**, Fig. 2 C: We use the option offered by the most CMOS technologies, particularly by the high-voltage CMOS processes, to surround the entire pixel electronics by a deep n-well. In this way we can isolate the NMOS transistor-bulk - the shallow p-well - from the chip substrate.
4. **High n-well reverse bias**, Fig. 2 D: The p-type substrate can be biased with a high negative voltage, down to typically $-100\,\mathrm{V}$. In this way a depleted region of typically $10\,\mu$m-$15\,\mu$m can be induced underneath the n-well. The depleted layer thickness depends on the resistivity of the wafer substrate, in the technology we used it is about $20\,\Omega$cm. The substrate is uniform, *i.e.* without an epi-layer. The primary signal is therefore similar as in the case of MAPS, however the charge separation and the charge collection occur by drift in a high-field region; they are fast and nearly lossless. This can improve the radiation tolerance.

We are referring to our detectors as the high-voltage CMOS detectors, smart diode arrays or simply as the HVMAPS.

We are developing the HVMAPS sensors since 2006. Within first proof-of-principle project phase, we have demonstrated a good detector performances and a radiation tolerance up to $10^{15}\,\mathrm{n_{eq}/cm^2}$ and 50 Mrad. The results have been published in [1-6]. The HVMAPS technology is also the main option for the tracking detector of the proposed Mu3e experiment [7, 8]. Thanks to its high radiation tolerance, the HV detectors are seen also at CERN as a promising alternative to the standard detector options. In order to test the concept, within ATLAS upgrade R&D, we are currently exploring two detector concepts, the bumpless hybrid pixel detector described in [6] and the active pixelated strip detector. In this paper, we will describe the second structure.

2. Strip Technology and HVMAPS

Our idea is to design a detector demonstrator that replaces a standard diode-based strip sensor

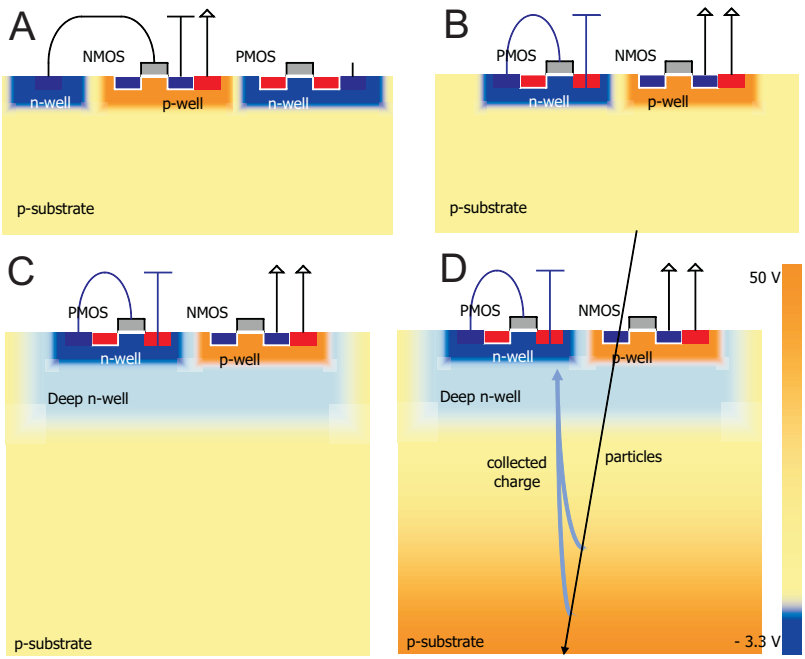

Figure 2: From an APS to the high-voltage CMOS pixel.

with an active HVMAPS. The clear advantage is the use of a commercial CMOS process which would allow a cheaper production of a large area-sensor. The typical price of an 8-inch wafer is 1500 EUR. The use of active circuits on the sensor would also open new possibilities, like generating the additional spatial information, or configurable grouping of strip channels.

The present LHC strip detectors consist of the large-area strip sensors that are connected by wire bonds to the multi-channel ASICs. For simplicity we consider the particular case of the short strips proposed for ATLAS upgrades, where the strip dimensions are $80\,\mu$m $\times$ 2.5 cm and each strip is connected to one channel of an ABCN chip.

The baseline demonstrator concept is a one-to-one replacement of the strip sensor by a large-area CMOS sensor, with no change to the ABCN chip or the rest of the system. A large area CMOS sensor can be produced by stitching several 2 cm $\times$ 2 cm wafer reticles.

The sensor basic unit would be an $80\,\mu$m $\times$ $100\,\mu$m pixel. Each pixel would contain a simple low-power ($< 5\,\mu$W) CMOS amplifier and a comparator. This would lead to a total 10 cm $\times$ 10 cm sensor power of the order of several watts (about 1.25 mW per $80\,\mu$m x 2.5 cm strip-channel).

When a pixel is hit by a particle, its electronics generate a digital pulse with a predefined amplitude and duration. The outputs of all pixels in one column (equivalent to one former strip) would be summed (logically "OR"-ed) and transmitted to the dedicated input of the readout ABCN ASIC. This is shown in Fig. 3.

The summing of the pixel output signals can be done for instance capacitively, which means the voltage pixel output signals are coupled to a summing line using small ($\sim$ 1 fF) in-pixel capacitors. Capacitive coupling is illustrated in Fig. 4. Such capacitive signals can be easily detected by presently used readout ASICs, since their input amplifiers are charge sensitive. Different implementations are also possible, like connecting/disconnecting of current sources to the summing

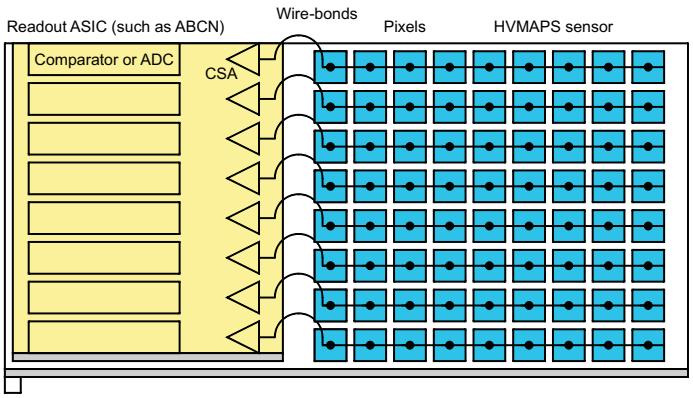

Figure 3: HVMAPS detector connected to strip-readout ASIC.

line.

The above simple description is the baseline demonstrator concept. As mentioned before many variants are possible due to the fact that we are reducing information in going from pixels to strip-like. The variants fall in 3 classes:

1. **Output pulse modulation:** This can be used to encode additional information in the pulse amplitude and/or duration. For example if one would use an analog readout ASIC instead of a binary one, one could adjust the pulse height as a function of z coordinate, as shown in Fig. 4. One could similarly adjust the pulse width as function of detected charge. Generating a signal of slightly different amplitude can be easily done by continuously increasing the size of the coupling capacitors from pixel to pixel, or by increasing the output voltage amplitude. In this way, we obtain a detector with 2D spatial resolution that can be readout by the ASICs designed for a detector with 1D segmentation. This would obviously reduce the number of readout channels compared to present stereo strip systems, and could provide high precision for the z coordinate. We call the detector "Pixelated Strip Detector" (PSD).
2. **Pixel ganging pattern:** Above we presented the case of ganging pixels in simple strips. However, any arbitrary pattern is equally possible. In particular, one can configure a CMOS sensor as an axial or stereo strip sensor by just the choice of ganging, and one can even have, both, axial and stereo ganging on the same sensor, with the possibility to dynamically select axial, stereo, or both at the same time in the case of having enough output bond pads. This can clearly also reduce material while keeping the same channel count. The stereo angle is not constrained by rotation angles of physical objects in this case, and could be anything up to even 90 degrees.
3. **Added processing:** While the baseline demonstrator is a simple one-to-one replacement of the strip sensor, it would clearly be possible to move some functionality from the readout ASIC into the CMOS sensor, or add new functionality in the CMOS senor that present systems lack. For example real time track trigger systems could benefit from such added functionality.

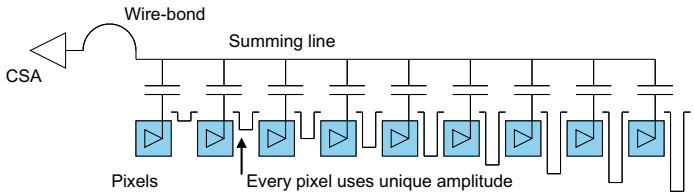

Figure 4: Pixel signals are summed and transmitted to readout ASIC.

3. Prototype Chip

In order to test the concept we have designed a test detector in a 180 nm high-voltage CMOS process. This detector has a pixel pitch of $33\,\mu\text{m} \times 125\,\mu\text{m}$ that is mostly determined by the requirements of the project where we readout the pixels capacitively using the FE-I4 pixel-readout ASIC. More details about this application and the ASIC itself can be found in [6].

To demonstrate the strip-readout, the pixels can be grouped into the arrays (columns) that contain 3 times 24 pixels. These arrays are readout through two summing networks that can be connected to two channels of the strip-readout ASIC. There are 20 such arrays on the test chip. The array structure and the ganging pattern are illustrated in Fig. 5. The summing of the pixel signals is performed by connecting of the pixel-output current sources to the summing networks A and B. We refrain of connecting of the neighbor pixels to the same network, otherwise the duplicated signal amplitudes will be measured in the case of charge sharing. The current-mode signals are converted to voltage and capacitively transmitted to the strip-readout ASIC using resistances R and capacitances C. To provide the information about the z hit-position the current sources are biased by a z-dependent bias voltage. The pixels receiving a higher bias generate an output current of a higher amplitude. The z-dependent bias is generated by a current flow through the resistor arrays (bias line resistors). To be able to distinguish the pixel signals coming from three pixel sub-arrays, three separated resistor arrays are used for biasing.

Fig. 6 shows the photograph of the test detector.

4. Experimental Results

Fig. 7 shows the output signals measured at the summing network when the pixel array is irradiated with ^{55}Fe source. The iron-source has been used for calibration purpose since it generates the charge signals of similar amplitudes as the minimum ionizing particles. The signals have been measured externally using an oscilloscope; no strip-readout chip has been used. The left graph shows several signals in the case when no z-dependent bias has been used. The different particles hitting different pixels generate signals of nearly equal amplitudes. This is as expected since the output pulse amplitude is determined by the strength of the current source in the pixels. Since all current sources are biased equally, they generate nearly equal signals. The slight amplitude variation can be explained by the current source mismatch and the noise. On the other hand, the pulse width corresponds to the time over threshold and is proportional to the charge measured by the CSA. The large variation of the pulse width can be explained by the charge sharing and by the threshold mismatch. The right graph shows the output signals when the z-dependent bias is used. The signal amplitudes are z-coordinate dependent and they fluctuate from hit to hit.

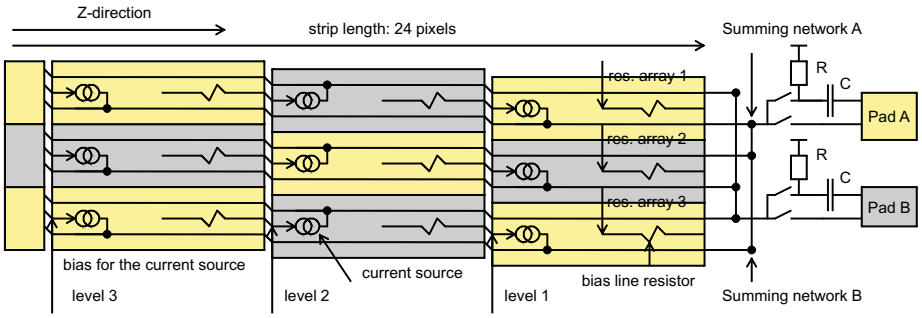

Figure 5: The structure of a pixel array implemented on the test detector.

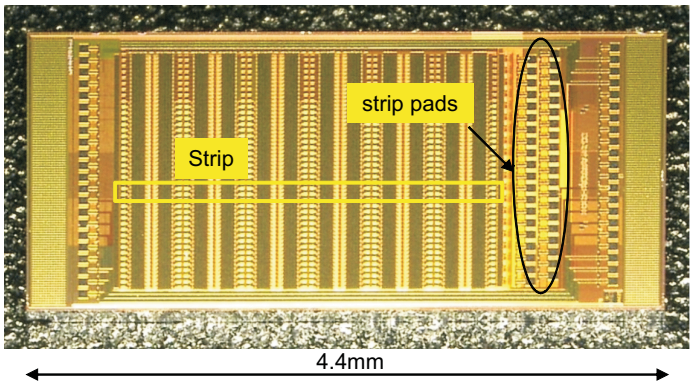

Figure 6: Photograph of the text-detector.

Fig. 8 shows the measured output signal amplitude as the function of the pixel-position. A test injection circuit has been used to emulate the signal charge. Again, the signals have been measured externally using an oscilloscope, no strip-readout chip has been used. We can see that the pixel amplitude depends on the z-coordinate. A rather large noise of the output signal is most probably caused by the fact that the output amplitudes are measured externally. The pixel output currents are driving the large output pad and the oscilloscope probe capacitances leading to a reduced signal to noise ratio. We are expecting to improve the results with our next test system based on a strip-readout chip.

The voltage amplitudes were in the range from 50 mV to 70 mV. These signals will be transmitted through 100 fF capacitors to the strip-readout chip leading to charge signals in the range 5 to 7 fC or 30 to 42 ke. Such a signals can be easily detected for instance by ABCN chip. The first measurements with a strip-readout chip will be performed soon.

5. Conclusions

High-voltage particle detectors in commercial CMOS technologies are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution. In order to test the concept, within ATLAS upgrade R&D, we are exploring the possibility to replace the standard strip sensor with an active HVMAPS. A strip of such a sensor is implemented as a pixel array, where the digital pixel outputs are summed and readout by a strip-readout ASIC.

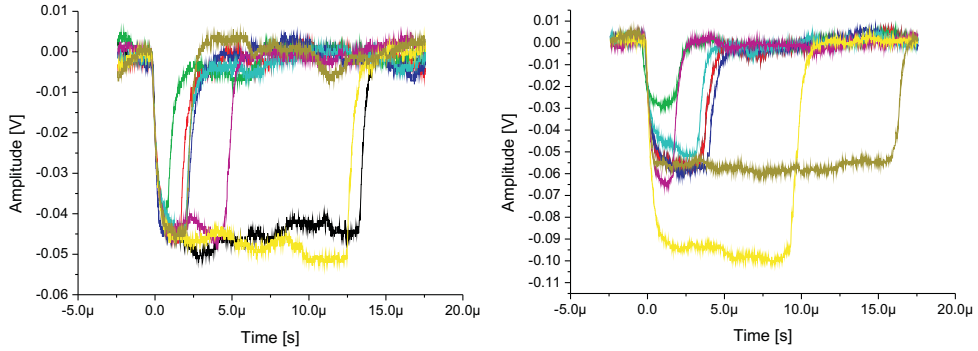

Figure 7: ^{55}Fe source measurements, the output signals have been measured with an oscilloscope. Left: no z-dependent bias is used. Right: z-dependent bias is used.

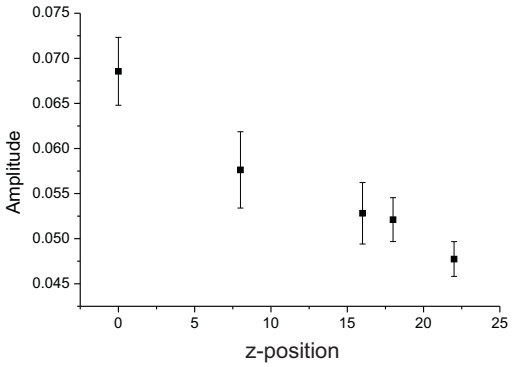

Figure 8: Measured output signal amplitude as the function of pixel-position.

Substituting of strips with the arrays of active pixels opens many new possibilities like generating the additional spatial information, or configurable grouping of strip channels. In the case of the pixelated strip detector, the pixel pulse height is a function of the z coordinate. This allows a 2D spatial resolution using one-dimensional strip-readout electronics. In contrast to double sided strip detectors, a pixelated strip detector would also work in the case of a relatively high occupancy: For instance, a double sided strip detector generates ghost hits in the case when two particles hit the sensor segment defined by the lengths of the overlapping strips. A pixelated strip senor generates a corrupted pixel position only when two particles hit the same strip, which occurs less frequently. Moreover, more advanced summing networks are possible that can cope with multiple hits per column. As an illustration, a simulation shows that a pixelated strip sensor based on $100\,\mu\text{m} \times 100\,\mu\text{m}$ pixels grouped into $100\,\mu\text{m} \times 1.28\,\text{cm}$ strips could work with more than 99% efficiency in the case of particle flux of less than 8 particles/cm^2/25 ns if the summing network can handle two simultaneous hits.

We have designed a test detector in a 180 nm high-voltage CMOS process. The first measurement results are presented. The detector behaves in the stand alone tests as expected and the first

measurements with a strip-readout ACIS will be performed soon.

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