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3D Interconnection with TSV

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3D interconnection with TSVs (through silicon via) allows the construction of quasi-monolithic multi-tier ASICs, a technology which offers many advantages. In addition to increasing the available area the main advantage is in shortening the length of metal connections within the circuitry reducing delays and decreasing power dissipation. For industry 3D interconnection is a possibility to continue Moore's law, or even improve on it ('more than Moore') beyond scaling. Though many of these arguments are not really relevant for HEP ASICs or sensors 3D technology still offers some important benefits like the possibility of monolithic devices in heterogeneous technologies or backside connectivity for more efficient I/O (4-side buttable chips). R&D has started, notable the Fermilab's 3DIC activity, projects converting the ATLAS FEI3 frontend into a 3D device and the WP3 work package of the EU funded AIDA project. Examples of these projects will be discussed.

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1. Introduction

The basic idea of 3D integration is to stack layers of thinned ASIC chips on top of each other and connect them by vias through the silicon bulk. This has obvious advantages:

- The area available for circuitry increases (doubles, triples,.. depending on the number of layers). This allows larger density without using smaller feature size.
- Different layers can be made in different technologies each optimized for its respective purpose. Layers can be designed e.g. as processors, memories, sensors or I/O.
- The circuit layout can be made more compact, reducing the length of metal interconnections between gates. This has important consequences for speed and power consumption.
- I/O connections can be routed through vias to the backside of the chip where they may be easier accessed.

The idea is actually quite old. E.g. Shockley patented holes through silicon wafers in 1962 [1] and Feynman proposed multi-layer computer chips in a lecture in 1985 [2].

3D interconnection is based on two technological ingredients:

- Vias need to be etched through the silicon bulk, insulated and filled with a conductor (copper, tungsten or polysilicon). In order to reach high densities and not to reduce the area for circuitry the vias need to be very small (view microns). DRIE (Deep Reactive Ion Etching) etching can reach aspect ratios of 10:1 which implies that chips need to be thinned to less than 50 μm to achieve vias of 5 μm diameter.
- High performance 3D chips need thousands of vias between the layers. Such high density vias need to be complemented by a high density interconnection technology. Industry standard for bump bonding has a pitch of about 200 μm, and even advanced processes hardly go below 50μm pitch. This is certainly not adequate. Microball bonding, SLID or direct copper-copper bonding need to be used to achieve the high density needed.

The via processing has to be integrated into the ASIC production chain. Depending on the order the vias are processed two different methods can be distinguished:

- Via first: The vias are etched before the processing of the CMOS circuitry (implants, dielectrica and metal layers). Hence the vias can be covered by the circuitry and do not require much extra area. Furthermore the via processing can use high temperature allowing for example filling with polysilicon. Compared to other materials polysilicon vias do not introduce stress due to thermal expansion mismatch. Via first processing has to be integrated in the CMOS process, which limits possible vendors and technologies. Sometimes vias are introduced later in the processing chain but still before the metal layers. This variant is called 'via middle'. It has essentially the same advantages and drawbacks as the via first approach.

- Via last: The vias are processed after the completion of the CMOS circuitry (including metal). This postprocessing can in principle be done with wafers of any CMOS process and fab by a third party. However, in order to protect the metal layers no high temperature processes are allowed, excluding polysilicon filling. The CMOS design has to be prepared for the via processing, e.g. space without active circuits or passive filling layers must be reserved. A requirement which is sometimes in conflict with design optimization done by the CMOS fab.

While via first offers highest via density and best use of the chip area, the via last process has more flexibility: different technologies from different suppliers can in principle be integrated to a monolithic device even if the suppliers do not offer TSVs in their process.

2. Motivation in Industry

The main driver for industry is the continuation of Moore's law. To date this has been achieved by scaling, that is using smaller and smaller feature size. There are increasing doubts whether this trend can continue. The problem may not be the technology limits to get small transistors but more the widths and thickness of the metal lines. Narrower, thinner lines increase power consumption and limit speed. Hence it can be expected that 3D technology will at some point outperform conventional chips with smaller features size. Apparently this is not yet the case and high performance 3D chips exist only as demonstrators and niche applications but not as large volume products.

Still, there are some application where 3D is ready to enter the mass market. One is stacking of memory chips. Such stacks are already in use (you may find them in your smartphone) but the stacks are staggered and the bus connection is made by stitched wire bonds. It is obvious from Fig. 1 that 3D interconnection offers a much cleaner solution. For such an I/O bus only few vias at the periphery of the chip. They can have rather large diameter (about 50 μm) and can be produced fairly easily. Still, this technology has to demonstrate that it can compete with the well established wire bond technology in terms of cost and reliability.

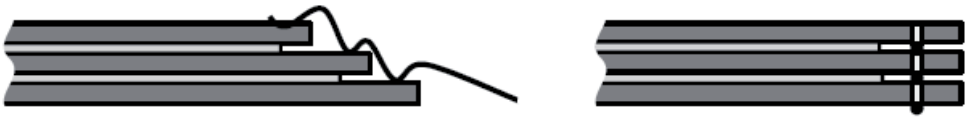

Figure 1: Left: State of the art stack of memory chips. The I/O bus is made by stitched bonds. Right: Same stack using TSVs for the I/O bus.

Another examples of 3D technology becoming used in large volume are interposers. An interposer is a passive silicon layer with vias and re-routing layers on a single or both surfaces. It allows efficient placement and interconnection of several chips to a system (hence often called SOC 'system on chip') and routing of the I/O contacts as illustrated in Fig. 2. This technology can be

seen as an intermediate step towards a 'real' 3D chip, hence it is sometimes called '2.5D'. Again, this application requires only few large diameter vias.

The technology needed for such large vias is becoming mature and is offered by an increasingly number of manufactures and institutes (e.g. AMS, CEA-LETI or IMEC) especially as via last postprocessing. On the other hand, high density, narrow vias in via first technologies are only rarely offered commercially (e.g. the Tezzaron technology as MPW by CMP [3].)

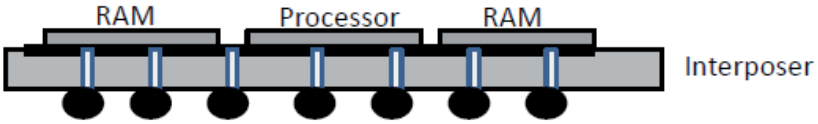

Figure 2: System on chip with a processor and memory chips. The interconnection between the chips is done via a routing layers on the passive silicon interposer. TSVs are used for the I/O connections to the bump bonds.

3. Motivation in HEP

Of course all kind of ASICs used in particle physics can in principle be made in 3D technology profiting from the advantages mentioned above. However, one has to admit that the main drivers for industry do not really apply here:

- Circuit density: State of the art HEP ASICs are made in 130nm technology, some advanced projects try to employ 65 nm technology. Thus HEP can still profit from several generations of scaling before hitting the difficulties industry is fighting with.

- Speed: Again, most of the HEP applications are at least an order of magnitude away from the speed of industry applications and do not reach the limits which can only be overcome going to 3D.

What remains, however, is the possibility to interconnect several layers of heterogenous technologies. The most obvious candidate is the hybrid pixel detector. The sensor layer uses high resistive material with rather coarse processing while the readout layer uses high density CMOS technology. Using 3D interconnection the major drawbacks of this concept can be overcome:

- High density interconnection: State of the art devices reach a pitch of about 50 μm, limited be the bump bonding technology available. High resolution vertex detectors in future experiments need a reduced pitch which can only be accomplished using interconnection technologies developed for 3D. Of course, if very small pixels limit the area for the readout circuitry (which is so far not the case) and multi-tier ASICs may be required, another argument in favor of 3D.

- Material reduction: Hybrid pixel detectors are known to have too much material, excluding them for high precision applications especially if low momentum tracks need to be reconstructed, like in b-factories. Since the multi tier architecture of 3D devices necessarily requires thin chips in order to achieve the high via densities with the aspect ratios available, material reduction comes naturally. Further improvements can result from optimized I/O connections (as discussed below).

In first approximation such detectors can simply be made bonding two layers (sensor and read out ASIC) face to face without need of TSVs. TSVs become interesting for the I/O: They allow routing the service contacts to the backside where they are easily accessible, avoiding the cantilever of present pixel sensor designs which add dead space and material, as illustrated in Fig. 3. 3D technology allows true 4-side buttable ASICs (which should then be complemented by edgeless sensors). This is even more interesting for x-ray sensors where seamless coverage of large areas is required.

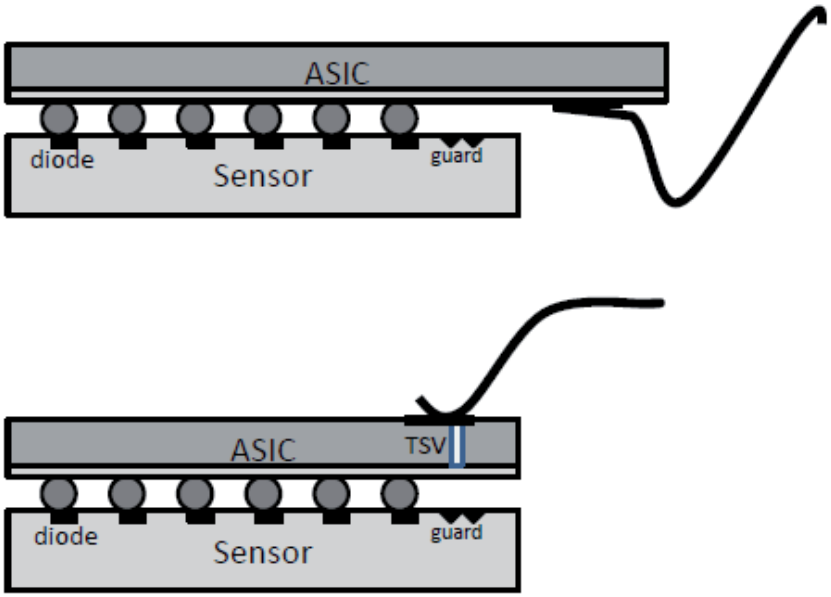

Figure 3: Top: State of the art layout of a hybrid pixel detector (Readout ASIC bump bonded onto a pixel sensor). In order to access the I/O pads of the chip it has to cantilever beyond the sensor causing dead space. Bottom: Using TSV the I/O can be routed to the backside of the chip making the cantilever obsolete.

4. Current R&D Projects

The earliest initiative started in the US. Fermilab [4] designed a 3-tier readout ASIC to be fabricated at Lincoln Lab. The projects finally succeeded with a few working prototypes but re-

vealed problems with yield and reliability of the CMOS process used. Fermilab then decided to use a commercial supplier. TEZZARON offered a 3D technology based on Charterd's 130nm CMOS process. It is a via middle technology allowing very small vias (2μ m diameter) and using copper-copper bonding to fuse the two tiers. Fermilab organized a collaboration (3DIC) of several institutes to contribute to a MPW in this technology. After considerable technical problems and delays, mainly caused by the takeover of Charted by Global Foundries, a few wafers were successfully completed and shipped recently. First tests show that the chips work nicely, an example of an chip for x-ray imaging is discussed in these proceedings [5].

In Europe MPI Munich started a project using the SLID and ICV process by Fraunhofer EMFT [6] to connect ATLAS FEI3 readout chips to thinned silicon pixel sensors. The TSVs could be placed in the wire bond pads for I/O, which had no active structures underneath allowing etching of the TSVs in a via last process. The SLID interconnection is a bumpless solder process with copper tin deposition by through mask electroplating. The process allows very fine pitch, basically limited only by the precision of the pick and place process. First sensor/ASIC assemblies showed 100% connected pixels with a performance equally or slightly better than the standard bump bonded assemblies [7]. The second step, including vias is presently in work. A picture of the TSVs etched in the FEI3 chip before tungsten filling is shown in Fig. 4.

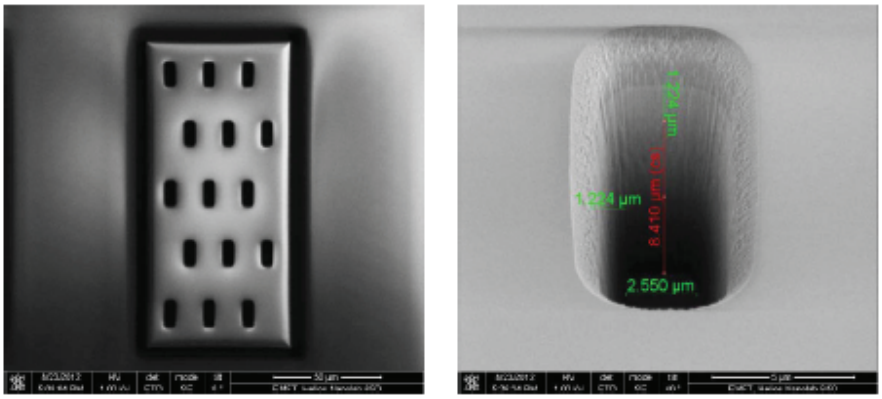

Figure 4: TSVs etched by EMFT into the ATLAS FEI3 chip. In order to have a redundant insulation of the vias from the bulk a protecting trench is etched around the vias. The via dimension is 2.5 μm times 5 μm.

A similar project has been done by the University of Bonn. They used a via process offered by Fraunhofer IZM with copper lined tapered vias of rather large diameter (up to 90 μm), see Fig. 5. This process is perfectly adequate for the large pitch I/O contacts of the FEI3 and is easier to process than the EMFT process (which, however, offer narrower vias). The modified chips were then bump bonded on sensors. Fully functional assemblies were reported [8].

More recently the European Union funded AIDA [9] project, started in 2011, organizes common activities of a network of institutes working on 3D integration (WP3 work package on microelectronics). An aim of AIDA WP3 is to bundle many independent projects into a more coherent R&D program. The program includes following institutions and projects:

- Bonn/CPPM: Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and

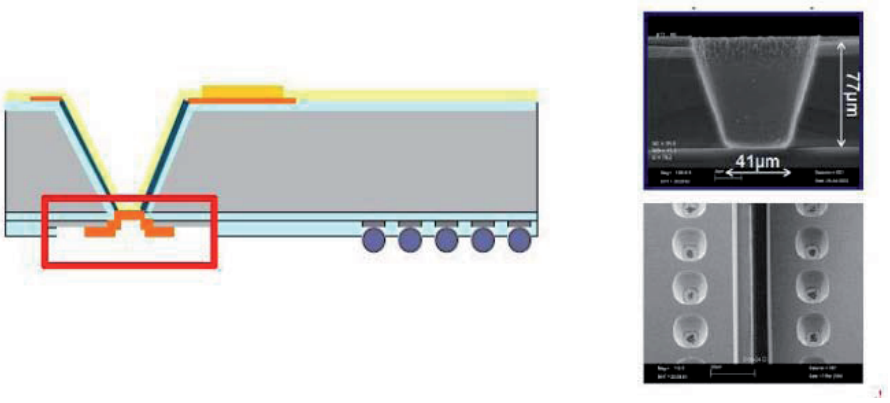

Figure 5: Left: Routing of the I/O to the back side of the chip using tapered, copper lined vias The vias are etched though the bulk from the backside and connected by a copper plug. Right: Pictures of tapered vias processed by Fraunhofer IZM (Courtesy University of Bonn/IZM, Berlin)

TSVs from IZM (large diameter TSV, large interconnection pitch). This is a continuation of the above mentioned activity of the University of Bonn with the more advanced FEI4 chip.

- CERN: Backside connectivity of MEDIPIX3 chips using TSVs. The MEDIPIX3, a successor of the MEDIPIX2 chip, has a '3D friendly' friendly design, namely landing pads for vias on metal 1, which can be reached by vias from the backside. Furthermore the edges of the chip with the wirebond pads can be cut off if the 3D interconnection is used reducing substantially the dead area of the chip. The vias, with a diameter of 60 μm, are processed by CEA-LETI in the framework of their 'open 3D initiative' [10].

- INFN/IPHC-IRFU: CMOS sensors in a two tier technology. The p-MOS transistors which act as parasitic charge collection nodes are transferred from the sensor tier to the second tier containing the complex signal processing. This will lead to a CMOS sensor with optimal charge collection and sophisticated in-pixel readout circuitry. This requires a fairly high via density. The tiers are produced by Tezzaron. Alternatively 3D readout ASICs (from Tezzaron) will be connected to edgeless pixel sensors using the interconnection technology of T-MICRO.

- LAL/LAPP/LPNHE/MPP: Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process. This project aims to design readout chips in an advance 65 nm technology optimized for 3D postprocessing.

- MPP/GLA/LAL/LIV/LPNHE: Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV from EMFT. This is a continuation of the above mentioned MPP project with the ATLAS FEI4 chip. In contrast to the similar project by Bonn/CPPM the emphasis is on narrow vias with high aspect ratio.

- RAL/UPPSALA: Integration of a 2-tier readout ASIC for a CZT pixel sensor using the EMFT SLID technology. TSVs will be used to redistribute I/O connections to the backside

for a 4-side buttable device.

The different 3D integration processes from different vendors will be evaluated in order to give guidance to future projects.

Some of the projects use relatively mature technologies which are already offered by industry. Via diameters are rather large but can well be used to achieve backside connectivity of I/O contacts. Other projects employ small vias enabling high via density for pixel by pixel interconnection. These projects are more challenging and require more R&D but offer substantial improvement of detector performance.

The following example illustrates the problems encountered: The FEI3 chip has no active and passive layers under the wire bond pads. Hence it is rather easy to etch narrow vias 50 μm deep from the circuit side and fill them with tungsten. These tungsten plugs are then opened by back thinning the chip and can be connected to a re-routing layer. The FEI4 chip does not have this feature (absence of active layers). Instead, the first metal layer (closest to the bulk) has a landing pad connected to the I/O. Vias can be etched from the back side till they reach this metal layer. For narrow vias with a large aspect ratio, however, it turns out that it is extremely difficult to ensure a good electrical connection. The need to insulate the via from the bulk creates an insulation layer on the already free metal pad. Due to the narrowness of the via it is not possible to remove this layer without destroying the wall insulation. The situation is completely different for large diameter or tapered vias. In this case the plasma etching has good selectivity to remove only the coating of the copper pad without affecting much the wall insulation. This example shows that technologies with large via diameter have reached some maturity allowing their use basically now. On the other hand the processing of narrow vias with high aspect ratio, which have of course much more potential for high performance chips, pose more challenges and need still considerable R&D.

5. Conclusions

3D integration technology based on TSVs offers many advantages for electronic in HEP especially for pixel detectors. 3D interconnection of a sensor and readout ASIC appears as a natural evolution of the hybrid pixel detector concept into a new monolithic detector with superior performance (smaller pixels, less material, 4-side buttable, complex signal processing). 3D technology is driven by industry, though for slightly different reasons, but this allows HEP projects to profit from progress in industry. R&D has started and some projects show first, encouraging results. Technologies offering large diameter vias (50 μm) become available and one can predict that this technology will soon see first real applications. However, more challenging concepts demanding high density (pixel by pixel) interconnections in a via last process still need considerable R&D effort.

References

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[10] see: http://www.leti.fr/en/How-to-collaborate/Collaborating-with-Leti/Open-3D