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Fast, granular and ultra–light pixelated double sided ladders based on CMOS sensors for an ILC vertex detector adapted to the ultimate collision energy

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The future International Linear Collider (ILC) is expected to provide an ideal environment for high precision measurements. In order to fully exploit it, very sensitive detectors are required. This applies in particular to flavour tagging, which relies on the realisation of a particularly granular and low mass vertex detector. CMOS pixel sensors are considered since long as an option for a vertex detector of ILD, one of the two experimental concepts developed for the ILC. The required, non-trivial, trade-off between high granularity, fast enough read-out and low power is achieved by combining a rolling shutter sensor architecture with a double-sided ladder design. This approach is followed in the ILD Detector Baseline Document (DBD) to be handed over to the review committee IDAG by the end of 2012, and will be presented in the first part of the proceedings.

In the second part, a faster sensor architecture will be addressed, based on in-pixel discrimination and highly parallelised rolling-shutter read-out. Expected to accelerate the read-out by nearly an order of magnitude, it exploits a newly addressed CMOS technology with $0.18\,\mu m$ feature size (instead of the $0.35\,\mu m$ process used previously). We will overview the perspectives and activities of this new step of the R & D, which is expected to allow for vertex detector based standalone tracking and to face the enhanced beam background [1] foreseen at the highest energy operation of the ILC ($\geq 1 TeV$). In particular, the test beam results obtained with the first sensor prototypes will be summarised, focusing on the charged particle detection performances of the technology.

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1. The ILD Vertex Detector

The ILC physics program requires a Vertex Detector (called VXD hereafter) that exhibits excellent performance in terms of heavy flavour tagging (b–, c–jets and τ leptons identification) and track reconstruction, especially for low momentum tracks. Flavour tagging is essential for numerous studies. A prominent example is the precise measurement of the Higgs boson couplings to the fermions. The key for the flavour tagging is the efficient reconstruction of the displaced vertices.

The VXD is composed of ladders, arranged in concentric cylindrical layers to form barrels. There are two main VXD candidate geometries. One is composed of 5 single–sided layers, meaning that each layer is equipped with silicon pixel sensors mounted on one side of a light mechanical support. The other consists of 3 double–sided layers, meaning that silicon pixel sensors will equip both sides of the mechanical support, with a 2 mm spacing between them, providing this way two very high precision measurements per layer.

1.1 VXD Requirements

As mentioned earlier, the VXD should allow identifying charm hadrons and τ leptons. Their decay length, in the order of $O(100\,\mu m)$, imposes a precision of $O(10\,\mu m)$ for the reconstruction of displaced vertices. On the other hand, the detector should also allow coping with the running constraints of the experiment. Satisfying the requirements imposed by both the physics goals of the experiment and its running conditions is a major challenge, since these requirements are often in conflict.

1.1.1 Physics Driven Requirements

For the purpose of the reconstruction of displaced vertices, one has to assign each track to its corresponding vertex. In order to do so, the impact parameter of the tracks has to be measured with the highest possible accuracy. Thus the impact parameter resolution (σ_{IP}) can be considered as the figure of merit for a vertex detector. It can be expressed by the following parametric equation, $\sigma_{IP} = a \oplus b/p \cdot \sin^{\frac{3}{2}}(\theta)$ where p is the particle's momentum and θ the polar angle. The parameter a depends on the single point resolution $\sigma_{s.p.}$ and on the lever arm. The latter is usually defined as the difference between the innermost and the outermost layer radii. In practice, however, the outermost layer of the tracker may have a higher impact on the tracking lever arm for the most energetic tracks than the VXD outer layer. The parameter b depends on the distance of the innermost layer to the Interaction Point (IP) and on the material budget. It becomes the dominant factor for either low momentum particles or particles crossing the VXD layers at a rather shallow angle, while a dominates for high momentum particles.

The ILD collaboration has set as target values for the parameters $a \leq 5\,\mu m$ and for b $\leq 10\,\mu m \cdot GeV/c$. Such a high impact parameter resolution has never been achieved by collider experiments. To reach these values, one has to target very thin sensors with particularly fine granularity, the lightest possible detector's ladders placed at a minimal distance from the IP and a large enough lever arm, while keeping the power consumption of the sensors at low levels. The ILD indicative sensor's and ladder's design specification required to achieve the desired performances are a single

point resolution of $\lesssim 3\,\mu m$, a radius of the first layer ~ 15 mm, and a material budget of the first layer restricted to a few per mil of radiation length.

1.1.2 Running Constraints

The running constraints of the ILC environment play a major role on the VXD design. They are mostly defined by the beam related background due to beamstrahlung. Beamstrahlung e^+e^- pairs define the pixel occupancy of the detector, since they dominate its hit density (see [2]). For a given hit density, the occupancy depends on the pixel pitch, the thickness of the sensitive volume of the sensor, the cluster multiplicity and the detector's time resolution. Experience acquired in previous experiments and intuition indicate us that the occupancy should be maintained below $\sim 1\%$. To achieve this goal, a relatively swift readout of $O(10\,\mu s)$ for the innermost layer is required. If the collision energy is upgraded to 1 TeV, the time resolution should be improved by a factor of ~ 5 (the beamstrahlung hit density is estimated to be 3–5 times higher for $\sqrt{s} = 1\,TeV$ than for 500 GeV). For the outer layers, this value can be relaxed up to $O(100\,\mu s)$.

The beamstrahlung consists also the main source of radiation damage for the VXD sensors. For a collision energy of 500 GeV, the estimated ionising radiation dose on the innermost layer may reach ~ 150 kRad per year. The annual bulk damage is expected to be equivalent to $\sim 10^{11}\, n_{eq}/\,cm^2$ (see [3]). A safety factor of three has been included for the estimation of both values. The radiation tolerance requirements may thus be considered as rather moderate.

Concluding, the ILD vertex detector requires highly segmented (pixel pitch of $O(10\,\mu m)$) ultra light sensors, being read swiftly and able to survive in a moderate radiation environment. A pixel pitch of $\sim 10\,\mu m$ means about 10^6 pixels per sensor. The main challenge is how 10^6 pixels can be read out fast, while keeping the power consumption low.

Pixel sensors being used by present and past collider experiments fail to face the above challenge. If one reads all the pixels simultaneously, the power consumption and the material budget will rise to unacceptable levels. While if the pixels are read out serially one by one, the required time will be in the order of milliseconds for a real size sensor. Novel pixel technologies have therefore been developed, which would provide the necessary trade–off between conflicting parameter optimisation. CMOS Active Pixel Sensors (CPS) is a promising candidate. For their principle of operation and main basic features the reader may refer to [4]. In the following sections we will describe the baseline CPS architecture, which offers an optimised trade–off between the various requirements, and then we will address the development of a VXD based on CPS, fully adapted to the ILC.

2. CMOS Sensors Baseline Architecture

A trade–off between the integration time and the power consumption can be achieved using the rolling shutter readout mode. The rolling shutter consists in reading the pixel matrix sequentially, single row after single row, and in transmitting the pixel analog signals to discriminators implemented at the sensor periphery, where they get digitised. In this way, the large amount of pixels consecutive to their small size ($\sim 16\,\mu m$ pitch) generates a moderate pixel matrix consumption, restricted to the row being read out. MIMOSA 26 [6] is an example of a CPS that demonstrates this baseline architecture. It is the first full scale digital sensor of the MIMOSA series with integrated

signal processing, and has been developed in order to equip the EUDET [7] beam telescope. It was fabricated in 2008–2009 with an industrial $0.35\,\mu m$ OPTO process, featuring a high resistivity epitaxial layer. It features 660 thousands pixels of $18.4\,\mu m$ pitch, arranged in 1152 columns and 576 rows. The sensor is thinned down to $50\,\mu m$ for most of its applications. Its performances have been tested in detail in laboratory and beam test campaigns. The measured detection efficiency was $\sim 99.8\,\%$ for a corresponding fake hit rate per pixel of 10^{-5}, while the spatial resolution was measured to be $\sim 3-3.5\,\mu m$. The integration time is $\sim 100\,\mu s$. MIMOSA 26 covers the VXD requirements for a highly segmented ultra light sensor but requires a significant read–out time shortening. This main challenge results from the beamstrahlung hit rate expected in the innermost layer. The necessary improvement is about one or two orders of magnitude for a collision energy ($\sqrt{s}$) of 500 GeV and 1 TeV respectively.

3. VXD Design for $\sqrt{s} \lesssim 500$ GeV

We will address the issue how the time resolution can be improved from $100\,\mu s$ to $10\,\mu s$. This approach is based on the rolling shutter readout, the double sided ladder structure [8] and the $0.35\,\mu m$ CMOS technology. This approach was first illustrated in [9]. The running constraints on the innermost layer are significantly different from the outer layers. The reason is that the beamstrahlung induced hit density decreases almost exponentially with the distance from the Interaction Point (IP). We will take advantage of this fact, and follow separate approaches for the design of the innermost and outer layers sensors. This proposal is viable due to the high flexibility and relatively low cost of the CPS.

3.1 Design of the Innermost Layer

The priority of the innermost layer's design is set to the time and spatial resolutions. In the rolling shutter, the readout time is proportional to the number of pixels per column. Therefore if one reads the sensor from both sides, and not only from the bottom as it is the case for MIMOSA 26, one automatically gains a factor of two, allowing for a $50\,\mu s$ read–out time. The price to pay is an increase of the insensitive area of the sensor and the power consumption. However this increase can be compensated by moving to smaller feature size CMOS processes (e.g. 25–50 % reduction of the insensitive area is expected when using a $0.18\,\mu m$ process). Moreover the smaller capacitance of the metal lines may allow us to increase the operational frequency, which will also benefit the readout speed. The integration time of the sensor may thus be pushed down to $40\,\mu s$.

To further improve the time resolution, in order to meet the VXD requirements, we will exploit the benefits arising from the double sided structure of the ladders. One side will be equipped with highly segmented square pixels providing the necessary high spatial resolution, while on the other side the pixels will be elongated in the column direction in order to achieve a high time resolution (figure 1). Equipping the innermost side with square pixels of $16\,\mu m$ pitch and binary readout, the desired $\lesssim 3\,\mu m$ spatial resolution can be achieved. A crucial step here is to extend the MIMOSA 26 pixel architecture from a pitch of $18.4\,\mu m$ to $\sim 16\,\mu m$. Moving towards a deep submicron process as the $0.35\,\mu m$ process used for MIMOSA 26 can make that feasible.

On the other side of the ladder, the sensors will have pixels with a 4–5 times longer pitch in the column direction. A pitch increase by a factor of 4 in this direction results in a subsequent

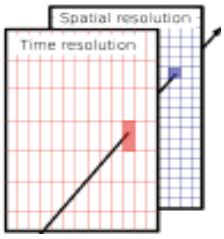

Figure 1: Structure of the double sided ladder for the innermost layer.

reduction of the number of pixels per column, and thus of the integration time by the same factor, reaching $\sim 10\,\mu s$. The key point of this approach is that hits generated on both, $\sim 2mm$ distant, sides of a ladder by the same traversing particle can be correlated. In this way, the elongated pixels side will timestamp the hit.

The reason why a $16\,\mu m$ pitch is expected to provide the ambitioned, $\lesssim 3\,\mu m$, spatial resolution, may be understood from figure 2, which shows how the resolution of square pixel sensors varies with the pixel pitch and charge encoding precision. The upper curve (brown dashed line) corresponds to the digital resolution (i.e. pitch divided by $\sqrt{12}$). The bottom blue line corresponds to the measured resolution of MIMOSA sensors with analog output (12–bit charge encoding) fabricated several years ago [10]. The intermediate lines and points correspond to the measured spatial resolution of sensors with binary charge encoding, when charge sharing between pixels is taken into account. The improvement with respect of the digital resolution is striking. By extrapolating the purple line, the predicted resolution of a digital sensor featuring $16 \times 16\,\mu m^2$ pixels is better than $3\,\mu m$.

The spatial resolution of elongated pixels has been studied with the MIMOSA 22 AHR sensor, which has submatrices equipped with pixels with dimensions of $18.4 \times 73.6\,\mu m^2$ placed in a staggered geometry. The submatrix provided digital output. The measured resolution was $\sim 6\,\mu m$ in both directions [11].

During the last quarter of 2011, a prototype sensor (MIMOSA 30) was fabricated aiming to demonstrate the feasibility of the VXD inner layer sensors. It was manufactured in the $0.35\,\mu m$ OPTO process mentioned earlier, using a high resistivity epitaxial layer. It consists of two parts featuring the designs of the sensors devoted for each side of a detector ladder. The first part, optimised for high spatial resolution, is composed of square pixels of $16\,\mu m$ pitch; the second part, optimised for timestamping, is composed of elongated pixels of $16 \times 64\,\mu m^2$. The Correlated Double Sampling (CDS) [5] takes place inside each pixel. The pixel matrices are read with a double sided column parallel readout. Each column ends with a discriminator, providing this way digitised output. The expected performances for the first part of MIMOSA 30 is a spatial resolution of $< 3\,\mu m$ and a readout time of $\lesssim 50\,\mu s$; while for the second part, the expected spatial and time resolution are $\sim 6\,\mu m$ and $\sim 10\,\mu s$ respectively. First test results of the sensor show that these integration times are indeed achieved.

3.2 Design of the Outer Layers

Due to the reduced beamstrahlung induced hit density (1 and 2 order of magnitude less for

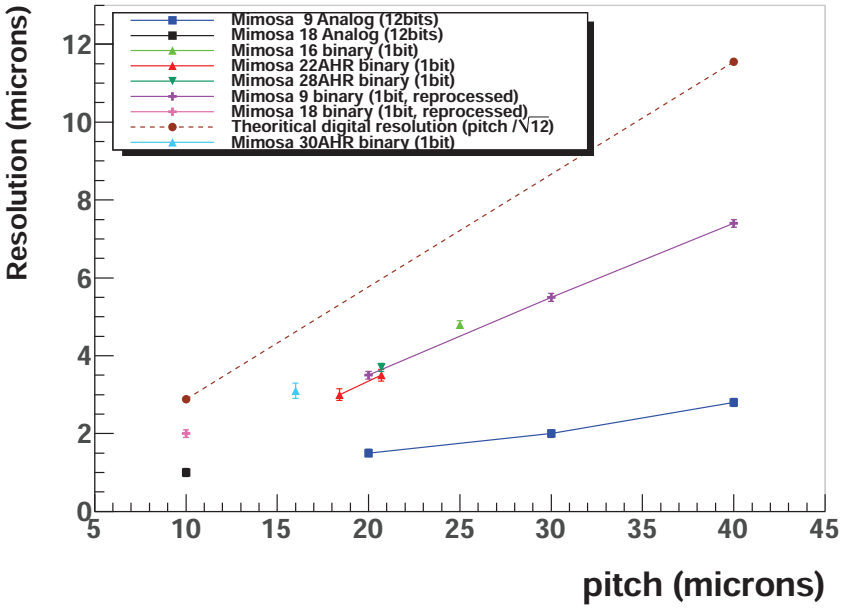

Figure 2: Spatial resolution as a function of the pixel pitch for various charge encoding precisions. The brown dashed line indicates the digital resolution, when charge sharing is not accounted for. The solid blue curve and square points at the lower part of the figure correspond to the spatial resolution of analog output sensors, while the intermediate curve and points stand for the spatial resolution of digital sensors (1 bit charge encoding).

the intermediate and outer layers respectively), a sensor integration time of $100\,\mu s$ is considered as adequate. Moreover, these two layers cover $\sim 90\,\%$ of the whole VXD sensitive area. Therefore, the corresponding sensor is designed giving priority to reduce power consumption and data flow. In the rolling shutter readout, the power consumption is proportional to the number of columns; the design is therefore oriented towards a reduction of this number. The sensor will thus be read only from one side and is going to be equipped with large square pixels of $34 \times 34\,\mu m^2$. This way the number of columns, thus the power consumption, is reduced by a factor of four with respect to the innermost layer. The loss in spatial resolution consecutive to the large pixels will be restored by replacing the end of column discriminators with ADCs. A square pixel with a pitch of $34\,\mu m$, being read with a 3–4 bits ADC, is estimated to provide a $\sim 3.5\,\mu m$ spatial resolution.

The power consumption of one column of MIMOSA 26 is $520\,\mu W$. If the column ends with a 3–4 bits ADC the consumption has been evaluated to stay well below 1 mW. The instantaneous power consumption of the whole VXD it is estimated to be $\lesssim 700$ W, if the sensors are fabricated in the aforementioned $0.35\,\mu m$ process. Moving to a smaller feature size technology ($\leq 0.18\,\mu m$), is expected to further decrease the power consumption due to the lower voltages used. Taking into account the ILC beam time structure (0.5 % duty cycle), and using a conservative assumption of a duty cycle of $\leq 2\,\%$ for the sensors to be switched on, the estimated average power consumption of the full VXD is estimated to be $\lesssim 15$ W. This value can allow for a light cooling system, using air flow at moderate speed.

A prototype of the sensor envisaged for the outer layers of the VXD, called MIMOSA 31, was fabricated during the last quarter of 2011. The size of the prototype is about 1/10 of the

size of the sensor envisaged for the VXD. It consists of 48 columns of 64 pixels, having a pitch of $35 \times 35\,\mu m^2$. Each column ends with a 4–bits ADC, which is expected to allow for a spatial resolution of $\sim 3.5\,\mu m$. The chip is currently being tested.

4. VXD Design for $\sqrt{s}$ of 1 TeV

At a collision energy of 1 TeV, the beamstrahlung induced hit density is expected to increase by a factor of 3 to 5 with respect to its 500 GeV value. Therefore we need to improve the time resolution of the VXD in order to keep the occupancy at a level of $\lesssim 1\%$. Spatial and time resolutions for each layer adapted to these more demanding conditions are summarised in table 1. A substantial improvement of the innermost layer's time resolution (factor of ~ 5) is desirable, while the spatial resolution should be preserved. Additionally, the extension to the outer layers of the timestamping strategy using different sensors on the two sides of a ladder, would help facing the increased hit rate.

Layer	Radius (mm)	Spatial resolution (μm)	Time resolution (μs)
DL1	16 / 18	3 / 6	50 / 2
DL2	37 / 39	4 / 10	100 / 7
DL3	58 / 60	4 / 10	100 / 7

Table 1: Ambitioned spatial and time resolutions for each VXD double–sided layer, for $\sqrt{s}$ = 1 TeV.

A conservative approach to improve the time resolution, which may be envisaged with the $0.35\,\mu m$ fabrication process, is to implement two discriminators per column. This way, two rows can be read out simultaneously, reducing the integration time by a factor of 2, down to $\sim 5\,\mu s$. The columns should however be enlarged well beyond $20\,\mu m$ (at the expense of the spatial resolution), and the limited number of the metalisation layers (i.e. 4 at most) hampers the possibility of achieving a compact data compression circuitry integrated in the chip.

Moreover, in order to further improve the time resolution down to the desired value of $\lesssim 2\,\mu s$, the discriminator should be implemented inside the pixel itself. This is only feasible with a smaller, $\leq 0.18\,\mu m$, feature size technology. When the discriminator is inside the pixel, a factor of two is gained directly, since there is no need to drive the analog signal to the end of the column. Additionally, more than one row can be read out simultaneously. For example, if one reads 4 rows simultaneously, the total gain in readout time is 2×4, thus from $10\,\mu s$ readout time one can go down to $\lesssim 2\,\mu s$.

Care should be given to the power consumption: more rows switched on means more power dissipated. On the other hand, that will be at least partially compensated by moving to smaller feature size processes, since they offer intrinsically reduced power consumption. The average power consumption of the whole VXD is therefore expected to be $\sim 12\,W$, a value which complies with a lightweight cooling system.

An alternative challenging approach is the following: the standard approach for the rolling shutter is to perform the latter from both the top and the bottom of the sensor, which means two rolling shutters per pixel matrix. One could envisage to further subdivide the pixel matrix into

submatrices, that will be read out in parallel. According to the number of the submatrices, we can gain in direct proportion in terms of time resolution, however again at the expense of an increased power consumption.

Addressing a prototype sensor manufactured in a $0.18\,\mu m$ process is an important step of the VXD R & D effort. In the following section we will discuss the results from the test beam of MIMOSA 32, the first prototype sensor of this type exploring this technology.

4.1 0.18 μm Prototype Sensor

The scope of MIMOSA 32 is to explore an industrial CMOS imaging process with $0.18\,\mu m$ feature size. The process was accommodated with wafers featuring a resistivity epitaxial layer $(1 \rightarrow 5\,k\Omega \cdot cm)$, offering up to 6 metal layers [1]. The design exploited the quadruple well option of the technology, which allows to alleviate the limitation of using only NMOS transistors for in–pixel signal processing. PMOS transistors can be hosted on deep P–wells, without compromising a priori the detection efficiency.

Various pixel designs have been implemented in the sensor. We will focus on the square pixel designs called P1, P6 and P9 which feature a pitch of $20\,\mu m$, and on the elongated ones called L4_1 and L4_2, with dimensions of $20 \times 40\,\mu m^2$ and hosting 1 and 2 sensing diodes respectively. P1 and P6 are simple basic designs, with a source follower implemented in the pixel. In P1 the diode leakage current is compensated by a biasing diode, while in P6 this is achieved by a reset transistor. The pixel P9 is addressing the quadruple well technology and integrates a reset transistor similar to the one of P6.

Non–irradiated chips, and chips irradiated with a total dose of 1 MRad and a fluence of $10^{13}\,n_{eq}/\,cm^2$ have been tested with O(100) GeV charged particles at the CERN–SPS, at operating temperatures of $15^0 C$ and $30^0 C$. The measured Most Probable Values (MPV) of the Signal over Noise (S/N) ratio at $15^0 C$, are summarised in table 2 for the aforementioned pixel designs.

We observe that the square pixels exhibit satisfactory S/N ratio and detection efficiency, even for radiation loads much higher than those expected at the ILC (see sub–section 1.1.2). Of particular importance are the results of the P9 design, which validate the performances of the quadruple well technology. Concerning the elongated pixels, their performances are degraded after this high irradiation level. But their performances are expected to be fully satisfactory for the ILC environment. Figure 3 shows the measured distributions of the S/N ratios for the P9 and L4_1 pixel designs, for various combinations of irradiation and temperature levels. We should stress the very promising results of the quadruple well technology pixel design, since that even for the less favourable case of $1\,MRad + 10^{13}\,n_{eq}/\,cm^2$ radiation dose and $30^0 C$ temperature, the MPV of the S/N is still ~ 20.

5. Summary–Outlook

These proceedings addressed an option of the ILD vertex detector based on CPS, and the related CPS R & D issues. The experiment's running constraints depend strongly on the collision energy, thus two different designs have been examined. The approach for $\sqrt{s}$ = 500 GeV uses the

[1] for the sake of minimal changes in the sensor design used with the aforementioned $0.35\,\mu m$ process, only 4 metal layers were used in MIMOSA 32.

Pixel design	Radiation load	S/N	Efficiency (%)
P1	0	35.1 ± 0.4	99.97 ± 0.03
P1	$1\,MRad + 10^{13}\,n_{eq}/cm^2$	25.4 ± 0.3	99.67 ± 0.12
P6	0	32.3 ± 0.4	99.84 ± 0.07
P6	$1\,MRad + 10^{13}\,n_{eq}/cm^2$	22.3 ± 0.3	99.87 ± 0.08
P9	0	30.9 ± 0.4	99.91 ± 0.06
P9	$1\,MRad + 10^{13}\,n_{eq}/cm^2$	22.6 ± 0.4	99.92 ± 0.08
L4_1	0	22.6 ± 0.2	99.86 ± 0.06
L4_1	$1\,MRad + 10^{13}\,n_{eq}/cm^2$	13.9 ± 0.3	99.51 ± 0.25
L4_2	$1\,MRad + 10^{13}\,n_{eq}/cm^2$	13.3 ± 0.2	99.0 ± 0.2

Table 2: Detection efficiency and S/N ratio observed with O(100) GeV particles with various pixel designs of non–irradiated and irradiated MIMOSA 32 chips, when the operation temperature is $15^0\,C$. The radiation load considered reflects the requirements of more demanding applications than the ILD–VXD. Results are preliminary and uncertainties are only statistical.

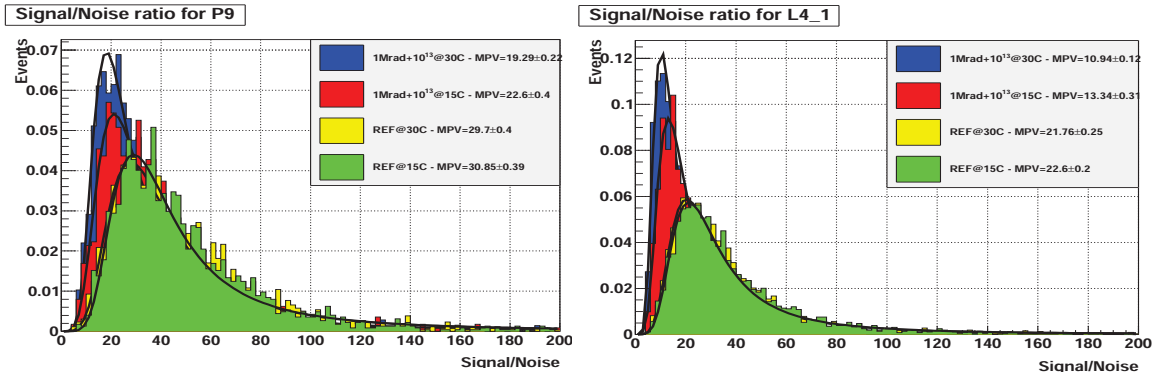

Figure 3: S/N ratio, before irradiation at $15^0\,C$ (green) and $30^0\,C$ (yellow), and after irradiation (1MRad + $10^{13}\,n_{eq}/cm^2$) at $15^0\,C$ (red) and $30^0\,C$ (blue), for the P9 design (left) and for the L4_1 (right).

well tested $0.35\,\mu m$ CMOS fabrication process, and is based on the rolling shutter architecture. An approach was proposed to timestamp tracks by combining different pixel dimensions equipping both sides of double sided ladders, while keeping the necessary spatial resolution. Exploiting the substantially different running constraints at the innermost and the outer layers, the power consumption could be restricted to levels compliant with air flow cooling. Two different prototypes sensors have been fabricated in $0.35\,\mu m$ technology, MIMOSA 30 for the inner and MIMOSA 31 for the outer layers. The ambitioned $10\,\mu s$ read–out time of the elongated pixel array of MIMOSA 30 was verified experimentally.

However, the enhanced beam background expected at a $\geq 1\,TeV$ machine imposes stricter requirements on the time resolution. This motivated us to move to a smaller feature size of $0.18\,\mu m$, which allows to exploit further the benefits offered by CPS. The quadruple well technology gives the possibility to implement both NMOS and PMOS transistors in the same pixel, without introducing a parasitic N–well charge collecting contact with the epitaxial layer. This, together with the

increased number of metal layers (6–7), allows to substantially increase the complexity of the logic integrated inside the pixel. We have illustrated how the in–pixel signal digitisation, along with a highly parallelised readout, is expected to provide the required time resolution while preserving the other performances of the sensor. The expected average power consumption ($\sim 12\,W$) stays in fully acceptable levels assuming a 2 % duty cycle of the sensors. Overall, the $0.18\,\mu m$ imaging process presented in this paper, is the first CMOS technology adapted to the ILD vertex detector requirements for the ultimate ILC collision energy.

MIMOSA 32 was the first prototype sensor of the MIMOSA series fabricated in this process. It has been tested both in the laboratory and in beam. The preliminary results shown in these proceedings, in particular for the elongated and the quadruple well pixel design, validate the technology's S/N ratio and detection efficiency, even for irradiation levels much higher than the ones expected at the ILC.

The future steps foresee the tests of MIMOSA 32ter, an updated version of MIMOSA 32 using all 6 available metal layers. It includes pixel arrays exploring in–pixel signal amplification. The prototype AROM 0 (submission in 2013) will address the in–pixel signal discrimination. Another prototype will be manufactured in 2013, which addresses the simultaneous read–out of 2–4 rows.

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