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The $\overline{\text{P}}$ANDA microvertex detector: design and prototype results

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The $\overline{\text{P}}$ANDA experiment at FAIR will exploit cooled antiproton beams in the momentum range from 1 to 15 GeV/c to perform high precision studies of QCD. Different targets, from hydrogen up to gold, will be used and a maximum interaction rate of 2×10^7 events per seconds is expected. Located in the innermost part of the experimental apparatus, the MicroVertex Detector (MVD) employs hybrid pixels and double sided silicon strip sensors to find the interaction vertices and improve the momentum resolution. Particular emphasis is given to the reconstruction of the displaced decay vertices of strange and charmed hadrons. Identification of low momentum particles through dE/dx measurements is also supported. The detector will operate with a triggerless read-out scheme, time-stamping the particle hits with an accuracy better than 10 ns. The system will contain about 10 million pixel channels and 200000 strips. In this paper, the design of the MVD is reviewed and recent results obtained on prototypes of key components are discussed.

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1. The $\overline{\text{P}}$ANDA Detector at FAIR

The Facility for Antiproton and Ion Research (FAIR) [1, 2] is a new complex of particle accelerators under construction near Darmstadt, in Germany. Located on the site of the present GSI laboratory, the facility will supply antiproton and ion beams for both basic and applied research purposes. One of the key elements of FAIR is the High Energy Storage Ring (HESR), designed to run with antiprotons in two operation modes. In the high resolution mode, the antiproton momentum can be varied from 1.5 to 8.9 GeV/c and the momentum resolution $\delta p/p$ is 10^{-5}. In this configuration, 10^{10} antiprotons can be stored in the HESR. The high intensity mode allows to increase the number of antiprotons circulating in the machine to 10^{11} and to boost their momentum to 15 GeV/c. This comes at the expense of a ten-fold coarser momentum resolution ($\delta p/p = 10^{-4}$). The HESR will use both electron and stochastic cooling.

Optimized for high precision QCD studies in the non perturbative regime, $\overline{\text{P}}$ANDA [3] is the dedicated detector of the HESR. The experiment is addressing topics such as very high precision charmonium spectroscopy, the search for glueballs and hybrids, the study of modifications of hadron properties in the nuclear medium. In addition, hypernuclear physics and electromagnetic reactions will also be explored. To cope with its broad physics program, $\overline{\text{P}}$ANDA is designed as a multipurpose apparatus and one of the key ingredients of its flexibility is the triggerless readout. All the subsystems must send properly time-stamped data to the DAQ, where a network of computing nodes selects in real time the interesting events for disk storage and subsequent off-line analysis. The DAQ algorithms can hence be adapted to best suit the particular physics channel under study. A 4π geometrical coverage is required to efficiently detect the reaction products in all the foreseen experimental conditions. The $\overline{\text{P}}$ANDA detector is therefore arranged as an asymmetric double spectrometer. The target spectrometer covers the high polar angles with a barrel geometry and is embedded in a 2 T solenoid. The forward spectrometer employs a resistive dipole magnet providing a bending power of 2 T·m. More information about the $\overline{\text{P}}$ANDA detector and its physics case can be found in [3].

2. The MicroVertex Detector

The MicroVertex Detector (MVD) is the innermost subsystem of the PANDA apparatus and is located close to the intersection between the target and the beam pipe. The key function of the MVD is the identification of the primary and secondary vertices. In particular, D mesons tagging is a crucial task for the $\overline{\text{P}}$ANDA physics program. The short decay length of these particles ($c\tau \approx 150\ \mu$m for $D_s^{\pm}$ and 312 μm for $D^{\pm}$) calls for a space resolution of 40 μm or better in the bending $\rho\phi$ plane. Furthermore, the MVD allows to improve the momentum resolution on all tracks and provides information for the identification of low momentum particles through dE/dx measurements. The detector is designed to give at least four hits per each track. In $\overline{\text{P}}$ANDA a maximum interaction rate of 2×10^7 events per second is expected. A good time resolution is hence mandatory to associate unambiguously each track with its parent interaction. In the present design, the MVD can provide a time resolution down to 2 ns rms. Finally, the sensors and the electronics components must have an adequate radiation tolerance. In the scenario of a 10 years experiment life-time with 6 months of data taking per year, the innermost layer of the MVD, located at 2.5 cm

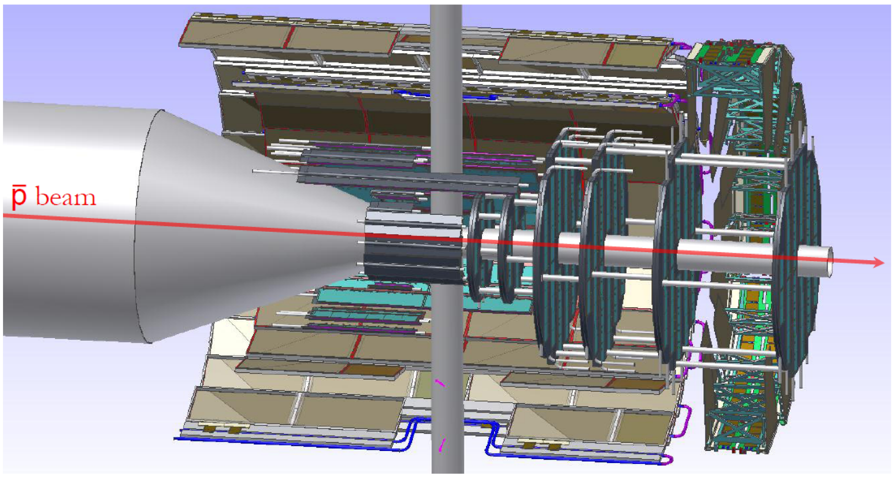


Figure 1: Conceptual design of the $\overline{\text{P}}$ANDA MVD.

from the interaction point, must sustain a total ionizing dose of 10 Mrad and a fluence of 10^{14} 1 MeV equivalent neutrons per cm^2. This radiation load has been estimated for $\bar{p}p$ collisions with a beam momentum of 15 GeV/c.

Fig. 1 shows a schematic view of the MVD [4]. The barrel part is equipped with two layers of hybrid pixels and and two layers of double sided silicon microstrip sensors. Due to the higher occupancy, the forward region is instrumented with six layers of pixel disks, the last two being supplemented by outer crowns of microstrip detectors. Hybrid pixel and strip sensors have been chosen since they are mature and reliable technologies offering both fast charge collection (which is necessary to achieve a good time resolution) and adequate radiation hardness. Supported by a light-weight carbon fiber structure, the MVD is 46 cm long in the beam direction and has a diameter of 30 cm. Such a compact geometry poses challenges to the service distribution. Since the downstream region is occupied by the forward spectrometer, access to the MVD is only possible from the upstream direction, where the space is further limited by the conic expansion of the beam pipe. This leads to inhomogeneities in the distribution of the material budget. The service layout concentrates most of the material either out of acceptance or at high polar angles, where it is less harmful for the physics performance. An effort has been made to keep the average material budget of the full MVD below 8% of a radiation length for most of the sensitive area. This is achieved through the use of custom Al-Kapton cables for power supply distribution and signal transmission and thanks to a light-mass cooling system, which employs demineralized waters under atmospheric pressure to maintain the MVD close to room temperature.

3. The Pixel Detectors

The pixel part of the MVD contains about 10 million independent channels. An elementary cell size of 100 μm$\times$100 μm has been selected as the one giving the best compromise in space resolution for both the forward and the barrel regions. Within the MVD collaboration, a dedicated

R&D effort has been undertaken to explore the possible use of epitaxial silicon sensors as they offer better radiation hardness than the one provided by standard Floating Zone (FZ) material [5]. Prototype sensors have been fabricated by FBK in Trento, starting from wafers provided by ITME (Warsaw). In the raw wafers, the epi-layer with a resistivity ranging from 2 to 5 kΩ·cm is grown on a Sb-doped Czochralski substrate having a resistivity between 0.01 and 0.02 Ω·cm. In the first step of the R&D, simple diodes and full sensors with an epi-thickness of 50, 75 and 100 μm were produced. The sensors were bump bonded to the pixel front-end ASIC developed for the ALICE experiment at CERN [6] and tested, investigating in particular the response to non-ionizing energy loss [7]. The samples were exposed to total fluences of $5.13 \cdot 10^{13}$, $1.54 \cdot 10^{14}$ and $5.13 \cdot 10^{14}$ 1 MeV equivalent neutrons per cm^2. The thinnest sensors showed as expected the best radiation tolerance. A 100 μm thick sensor with a resistivity of 2 kΩ·cm has been chosen as the optimal compromise, combining better signal-to-noise ratio in the first years of running with acceptable performance towards the end of the experiment life-time. In fact, after ten years, a pixel with a volume of 100 μm$\times$100 μm$\times$100 μm is expected to have a leakage current of 60 nA, which can be tolerated by the front-end electronics. The charge collection efficiency should still allow the detection of minimum ionizing particles. More details on the irradiation test results can be found in [7]. In the innermost part of the experimental apparatus, the structure of the beam and target pipes complicates the achievement of a full geometrical coverage. To minimize the number of different module designs a basic unit, corresponding to a single front-end chip with 116$\times$110 pixels, has been defined. All sensors are then built by tiling together a suitable number of these fundamental matrices. By employing modules which are read-out respectively by two, four, five and six chips one can reach an optimal coverage of both the barrel and the forward regions. Fig. 2 shows one 4-inch wafer with the different sensors, together with a zoom on the pixel matrix, where the pads for bump bonding are also visible.

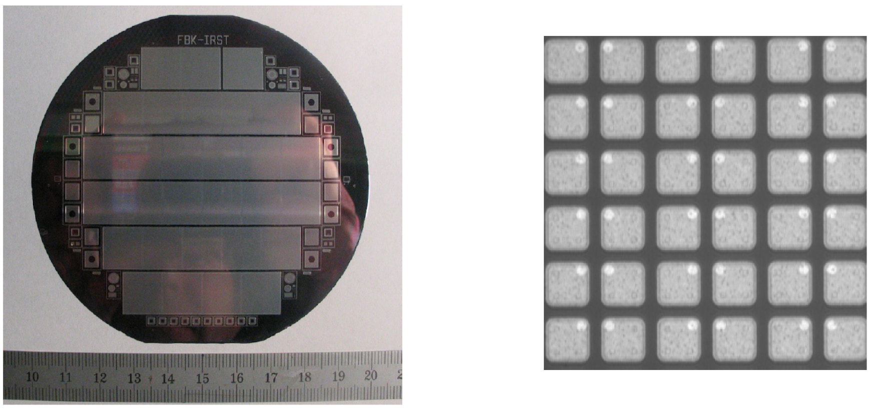


Figure 2: Picture of an epitaxial sensor wafer with a zoom on the pixel matrix on the right.

For the read-out the pixel sensors, a custom front-end ASIC, called ToPiX, is under development in a 0.13 μm CMOS technology. To be compliant with the $\overline{\text{P}}$ANDA triggerless DAQ, the chip employs a free running architecture, in which all the events above a preset threshold are time-stamped and transmitted off-chip. The timing information is provided by a centralized clock counter, whose outputs are Gray-encoded and distributed to the pixels. In each cell, the charge released by the particle impinging on the sensor is integrated on the feed-back capacitor of a Charge Sensitive Amplifier (CSA). A constant current source restores the CSA baseline, allowing for a linear measurement of the deposited charge through the encoding of the Time over Threshold (ToT) [8]. The ToT is obtained by latching into local registers the counter values corresponding to the leading and trailing edge transitions of the output of the voltage comparator that follows the CSA. The charge measurement adds a very limited overhead in term of circuit complexity and a moderate burden on the data transmission bandwidth, while offering a few significant performance enhancements. First, the availability of the ToT information allows to apply time walk corrections. In this manner, a slow and lower front-end can be adopted even though a time resolution of 10 ns or better is envisaged. In the present implementation, the CSA has a rise time of 60 ns and the full analog front-end dissipates only 15 μW from a 1.2 V power supply. Second, the pixels system can contribute to the identification of low momentum particles. This is particularly relevant for the forward disks, where the six layers allow for a good separation power despite the sensor thickness of only 100 μm. Finally, center of gravity algorithms can be exploited in case of charge sharing to improve the spatial resolution. The very front-end of the pixel system is described in [9], while results obtained on the most recent prototype of the ASIC are reported in [10]. In the final set-up, low mass Al-Kapton cables bring power to the modules and route out the signals on high speed (320 Mbit/sec) differential lines with 100 Ω characteristic impedance[11]. The data are transported electrically out of acceptance, where electro-optical conversion and long-distance transmission is performed by the GBT, a radiation tolerance chipset developed at CERN for the LHC detector upgrades [12].

4. The Strip Detectors

The strip sensors are based on the double sided technology. Fig. 3 shows a 4-inch wafer with the sensors for the barrel part. The sensors labeled as "S1" and "S2" are optimized for final use in the experiment, while the smaller units are intended for test purposes only. Due to the low occupancy in the barrel part, both S1 and S2 employ orthogonal strips. The sensors cover respectively an active area of 58.275 mm$\times$33.315 mm (S1) and 33.315 mm$\times$33.315 mm (S2). The strips have a pitch of 65 μm. Strip isolation on the n-side is achieved through the p-spray technique, while a punch-through biasing scheme has been implemented in the first prototypes. Produced on FZ wafers, the sensors are 285 μm thick and have been fabricated by CiS GmbH in Erfurt, Germany. Fig. 4 shows the conceptual design of the strip modules for the barrel and the disk layers. In the barrels, the front-end electronics is located at the edge of the sensors. The short strips are connected to the ASIC inputs with a short fan-out, while the strips on the longer side necessitate a fan-out where the signal lines are folded by 90°. All the interconnections are realized with low-mass flex cables, with the sensors being supported by a carbon fiber structure. The cooling pipe is routed underneath the front-end chips, mounted at the sensor edges. The sensors instrumenting the forward disks have a trapezoidal geometry. To cope with the higher occupancy in this region, the strips on the two opposite sides of a sensor are tilted by a small stereo angle (15°). One module contains two sensors belonging to two different disks. A common central support holds the two detectors, while the front-end electronics is located on the top of the support structure, where it is

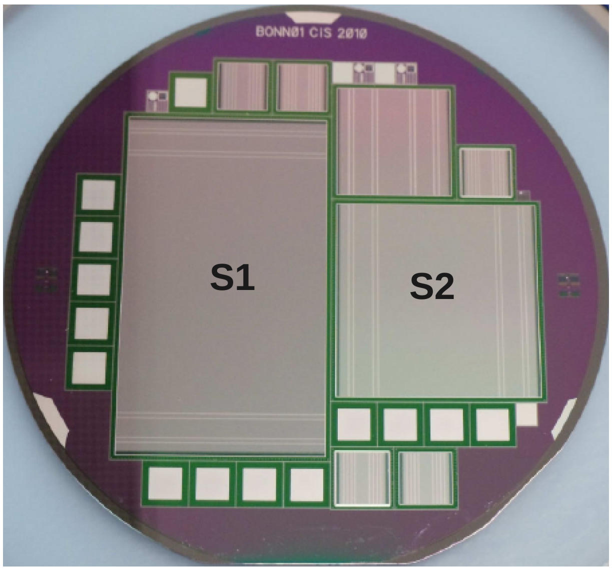
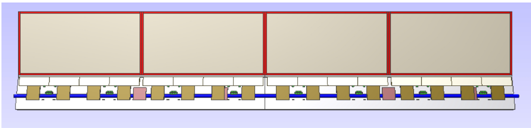
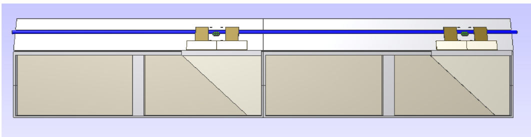


Figure 3: Silicon microstrip wafer with sensors for the barrel part.

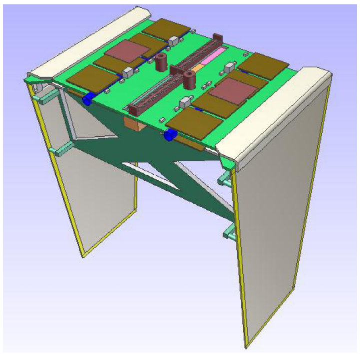
less harmful to the material budget. Several options are under consideration for the strip front-end ASIC, which has to combine a low power consumption (less than 5 mW per channel) with a 10 bit dynamic range and a fast, self-triggered read-out. The use of a time-based read-out with charge-encoding through Time-over-Threshold with a scheme similar to the one used in ToPiX in one of the options under study.



Barrel module with the short strips connected to the front-end electronics.



Barrel module with the long strips connected to the front-end electronics with a folded cable.



Disk modules with the mechanical support.

Figure 4: Concept of the strip module for the barrels (on the left) and the forward disks (on the right).

5. Prototype Results

Several prototypes of the critical MVD components have been produced and tested. For the pixel part, small scale versions of the ToPiX front-end ASIC have been designed by INFN in Torino using a commercial CMOS 0.13 μm process and fabricated through Multi-Project Wafers.

The most recent version of the chip incorporates 640 pixel cells, organized in two double columns containing 2×128 pixels and two short double columns with 2×32 pixels. The cells within a double column share the time stamp and data buses. The long columns have a folded layout, which leads to a reasonable form factor of the matrix while preserving the full length of the data and power connections. This allows to anticipate issues related to power supply distribution and signal routing over long lines expected for the final ASIC. The short columns provide a best case and serve as a reference. The chip has been bump bonded by IZM to a sensor and the assemblies have been extensively tested both on the bench and in beam tests. For the strips, final versions of the barrel sensors have been fabricated. The results obtained on prototypes for both pixel and strip sensors are extensively discussed in [13].

Two tracking stations, one made of pixels and another of strips, have been assembled. The pixel tracking station, designed and mounted by INFN in Torino, is made of four boards, each hosting a sensor bump bonded to a front-end chip. The 640 pixels occupy an active area of 3.2 mm×3 mm. The strip tracking station, developed at the University of Bonn, is also formed by four boards, instrumented with double-sided sensors of 1.98 cm×1.98 cm with 50 μm pitch. The APV chip [14] is used for read-out. This ASIC needs an external trigger, which is provided by scintillators coupled to photomultiplier tubes. The architecture of the pixel front-end electronics is already compliant with the $\overline{\text{P}}$ANDA triggerless read-out scheme. Both tracking stations have been used in a beam test performed at the COSY accelerator of the Forschungszentrum in Jülich, with beams of 2.75 GeV/c protons, and at CERN. The results discussed in the following were obtained with the data of the Jülich beam test. The main purpose of this test was to perform a first characterization of the ToPix front-end chip bump-bonded to epitaxial pixel sensors and to run simultaneously the pixel and strip data acquisition systems. Several set-up configurations were employed: two strip planes followed by one pixel station and again two strip planes or two strip planes followed by four pixel stations and additional two strip planes. The distance between the strip and the pixel modules was also changed to study the impact of the multiple scattering. Figure 5 shows

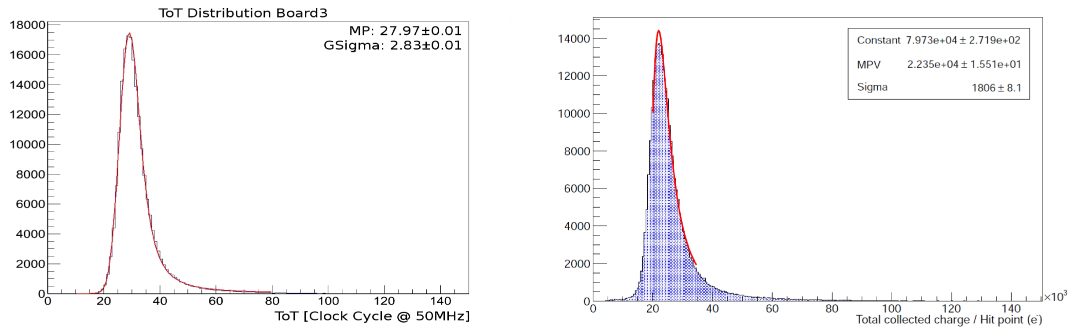


Figure 5: Landau distributions measured by pixels (left) and strips (right) of the two tracking stations.

examples of Landau distributions obtained from pixels (on the left) and strips (on the right). For the pixels, the measurements were performed running the system with a clock of 50 MHz, since a layout issue prevents the long columns from working at full clock speed. A low noise of 100 electrons rms allowed to apply thresholds down to 600 electrons. The feed-back current was tuned to 2.5 nA, therefore for one minimum ionizing particle (m.i.p.) in 100 μm silicon (1.35 fC) one expects a ToT of 27 clock cycles at 50 MHz, which is compatible with the results. The charge collected by the strips corresponds to the expected value (22500 electrons) for a 300 μm sensor. To study the time walks of the pixels, one board was tilted by 40° with respect to the beam to maximize the number of double clusters. The timing difference between the smaller and the bigger hit of every cluster was measured. The results are shown in Fig. 6. The left and the central plot in the figure shows the ToT values for the two hits. The plot on the right correlates the time difference between the two hits with the amplitude of the smaller one. One can see a clear correlation, with the smaller hits experiencing larger delays as expected. A study on optimized algorithms to exploit the ToT information for time walk correction is underway. Finally, Fig. 7 reports the hit multiplicity (on

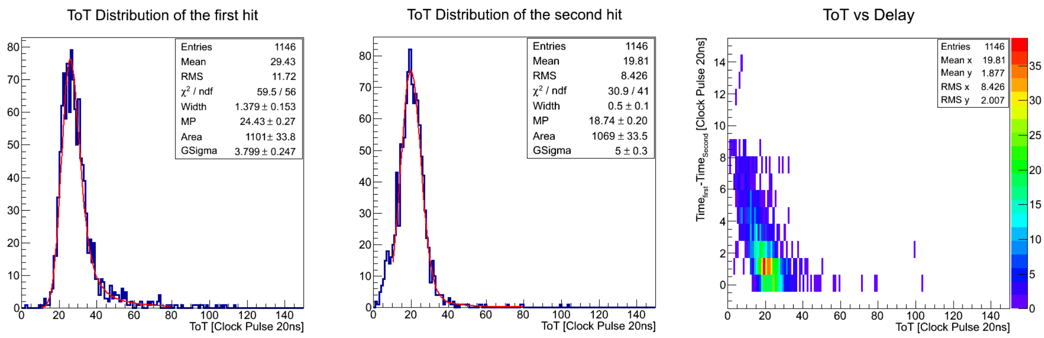


Figure 6: Time delay as a function of the ToT for two hits belonging to the same cluster. See text for details.

the left) and the hit position error (on the right) calculated for the single microstrip plane. The multiplicity takes into account the number of hit strips on both sides, so the minimum value is 2. The worst hit position error corresponds to the pitch/$\sqrt{12}$, obtained when only one strip is hit. In the other cases, the use of the center of gravity algorithm allows the reduction of the error to a few microns. In this beam test, both set-ups were not optimized in terms of material budget, hence the residual distribution was fully dominated by multiple scattering. For the pixel board, the single cluster resolution was degraded from the theoretical value of 29 μm to 38 μm. Boards with improved layout were used in following beam tests and preliminary results indicate that the expected theoretical value is within reach. The multiple scattering introduced by the pixel stations limited the combined resolution of the four strip planes to O(90 μm).

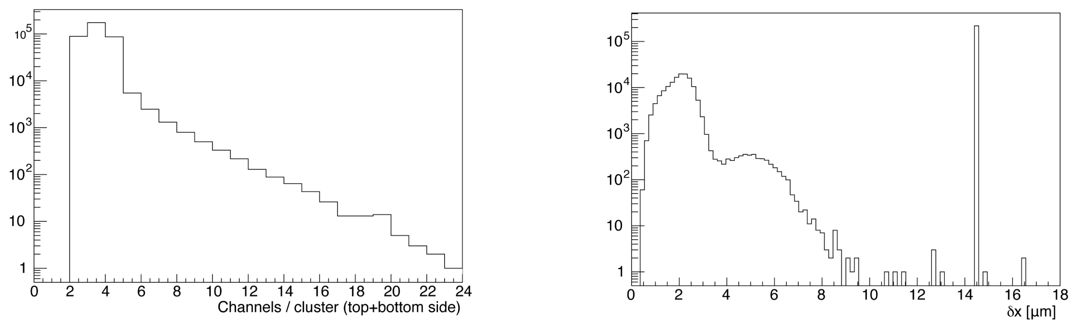


Figure 7: Strip cluster multiplicity (left) and hit position error of a single plane (right).

6. Conclusions

The design of the microvertex detector of the $\overline{\text{P}}$ANDA experiment is well advanced, with the R&D phase near completion. The system makes use of well proven silicon technologies, namely hybrid pixels and silicon strips, to provide at least four hit points per track with good space and time resolution. Tracking stations employing reduced scale sensors have been built for both strip and pixels and used together in beam tests. Triggerless operation with the pixel front-end electronics was demonstrated, together with space resolution close to the nominal value. The design of the low-mass support mechanics is completed and integration studies are progressing. The next major steps now ahead are the implementation of full scale front-end ASICs and of the final data transmission system.

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