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Vertex-Detector R&D for CLIC

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The CLIC vertex detector must have excellent spatial resolution, full geometrical coverage extending to low polar angles, extremely low mass, low occupancy facilitated by time-tagging, and sufficient heat removal from sensors and readout. These considerations, together with the physics needs and beam structure of CLIC, push the technological requirements to the limits and imply a very different vertex detector than the ones currently in use elsewhere. This paper reviews the experimental conditions and the requirements for the vertex detectors at CLIC, presents the proposed vertex-detector layouts and discusses recent results on detector simulations, pixel-readout development, power delivery and cooling.

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1. Introduction

The proposed Compact LInear Collider (CLIC) concept of a linear electron-positron collider with a centre-of-mass energy of up to 3 TeV has a large physics potential, complementing and extending the measurements of the current LHC experiments [1, 2, 3]. It will allow for precision measurements of standard model physics (e.g. Higgs, top) and of new physics potentially discovered at the LHC (e.g. SUSY). Moreover, direct and indirect searches for new physics over a large range of mass scales will be performed. The demands for precision physics in combination with the challenging experimental conditions at CLIC have inspired a broad detector R&D program. In particular the vertex-detector systems have to fulfil unprecedented requirements in terms of material budget and spatial resolution in a location close to the interaction point, where the rates of beam-induced background particles are very high. The ongoing CLIC vertex-detector studies focus on ultra-thin hybrid pixel detectors and aim for integrated solutions taking into account constraints from mechanics, power delivery and cooling.

2. The CLIC machine environment

The CLIC project studies the feasibility of a linear electron-positron collider optimized for a centre-of-mass energy of 3 TeV with an instantaneous luminosity of a few $10^{34}\text{cm}^{-2}\text{s}^{-1}$, using a novel technique called two-beam acceleration [1]. A drive beam of rather low energy but high current is decelerated, and its energy is transferred to the low-current main beam, which gets accelerated with gradients of 100 MV/m. The two-beam acceleration scheme thus removes the need for individual RF power sources along the accelerating main LINAC. It is expected that the machine will be built in several stages with centre-of-mass energies ranging from 500 GeV or less up to the maximum of 3 TeV, corresponding to an overall length of the accelerator complex from approximately 11 to 48 km. In order to reach its design luminosity of $6 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ at a maximum centre-of-mass energy of 3 TeV, CLIC will operate with very small bunch sizes ($\sigma_x \times \sigma_y \times \sigma_z \approx 40\text{nm} \times 1\text{nm} \times 44\mu\text{m}$). 12 GHz accelerating structures drive the two main beams and collisions occur in bunch crossings (bx) every 0.5 ns for a train duration of 156 ns. The train repetition rate is 50 Hz. The short train duration implies that trigger-less readout of the detectors once per train will be implemented. The power consumption of the detetors and thereby the material required for cooling infrastructure can be reduced by switching off parts of the frontend electronics during the 20 ms gaps between trains.

3. Beam-induced backgrounds

The very small beam sizes lead to strong electromagnetic radiation (Beamstrahlung) from the electron and positron bunches in the field of the opposite beam. The creation of the Beamstrahlung photons reduces the available centre-of-mass energy of the e^+e^- collisions and their interaction leads to lepton pairs and hadrons, most of which are produced at very low polar angles and therefore contained in the beam pipe by the axial magnetic field [4]. The dominant backgrounds in the inner detectors are incoherently produced electron-positron pairs (approximately 60 particles / bx) and $\gamma\gamma \rightarrow$hadrons events (approximately 54 particles / bx). The electron-positron pairs are predominantly produced at very small transverse momenta and low polar angles. The detector occupancies

in the innermost layers can therefore be reduced to an acceptable level by a careful design optimisation of the inner- and forward-detector regions: The central beam pipe walls have to be placed outside the high-rate region and the inner detectors have to be efficiently shielded from back-scattered particles originating from the forward region. The particles produced in $\gamma\gamma \rightarrow$hadrons interactions, on the other hand, show a harder transverse momentum spectrum and a more central polar-angle distribution, resulting in large rates of background particles with every bunch crossing, reaching also the outer detector layers. While at most one interesting physics event is expected in each train, ≈ 1000 hadronic background events are produced. Pile-up rejection algorithms based on hit time stamping are needed to separate the physics from the background events.

The radiation exposure of the main detector elements is expected to be small, compared to the corresponding regions in high-energy hadron-colliders. For the non-ionizing energy loss (NIEL), a maximum total fluence of less than $10^{11}\mathrm{n}_{eq}/\mathrm{cm}^2$/year is expected for the inner barrel and forward vertex layers. The simulation results for the total ionizing dose (TID) predict approximately 200 Gy/year for the vertex-detector region.

4. Vertex-detector requirements

The vertex detectors at CLIC are integral parts of the full coverage tracking systems, designed to improve the accuracy of the track reconstruction in particular for low transverse momenta. Their primary purpose is to allow for efficient tagging of heavy quarks through a precise determination of displaced vertices. Monte Carlo simulations show that these goals can be met with a high-momentum term in the transverse impact-parameter resolution of $a \approx 5\mu$m and a multiple-scattering term of $b \approx 15\mu$m, using the canonical parametrization:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}, \tag{4.1}$$

where p is the momentum of the particle and θ is the polar angle with respect to the beam axis. These requirements on the measurement precision exceed the results achieved in any of the currently existing full-coverage vertex systems. They can be met with multi-layer barrel and endcap pixel detectors operating in a magnetic field of 4-5 T and using sensors with a single-point resolution of $\approx 3\mu$m and a material budget at the level of $< 0.2\%$ of a radiation length (X_0) for the beam pipe and for each of the detection layers. The single-point resolution target can be met with pixels of $\approx 25\mu\mathrm{m} \times 25\mu\mathrm{m}$ and analog readout. The material-budget target corresponds to a thickness equivalent to less than 200 μm of silicon, shared by the active material, the readout, the support and the cooling infrastructure. This implies that no active cooling elements can be placed inside the vertex detector. Instead, cooling through forced air flow is foreseen, limiting the maximum power dissipation of the readout to ≈ 50 mW/cm^2. Such low power consumption can be achieved by means of power pulsing, i.e. turning off most components on the readout chips during the 20 ms gaps between bunch trains.

Time slicing of hits with an accuracy of $\approx$ 10ns will be required to separate beam-induced backgrounds from physics events.

5. Detector concepts

The detector concepts ILD [5] and SiD [6], developed for the International Linear Collider (ILC) [5] with a centre-of-mass energy of 500 GeV, form the starting point for the two general-purpose detector concepts CLIC_ILD and CLIC_SiD. Both detectors will be operated in one single interaction region in an alternating mode, moving in and out every few months through a so-called push-pull system. The main CLIC-specific adaptions to the ILC detector concepts are an increased hadron-calorimeter depth to improve the containment of jets at the CLIC centre-of-mass energy of up to 3 TeV and a redesign of the vertex and forward regions to mitigate the effect of high rates of beam-induced backgrounds.

Both detectors have a barrel and endcap geometry with the barrel calorimeters and tracking systems located inside a superconducting solenoid providing an axial magnetic field of 4 T in case of CLIC_ILD and 5 T in case of CLIC_SiD. In the CLIC_ILD concept, the tracking system is based on a large Time Projection Chamber (TPC) with an outer radius of 1.8 m complemented by an envelope of silicon strip detectors and by a silicon pixel vertex detector. The all-silicon tracking and vertexing system in CLIC_SiD is more compact with an outer radius of 1.3 m.

5.1 Vertex-detector simulation layouts

The detector models used for the simulation of physics benchmark processes include silicon vertex pixel detectors with $20\mu\text{m}\times20\mu\text{m}$ pitch. In case of CLIC_ILD, both the barrel and forward vertex detectors consist of three double layers which reduce the material thickness needed for supports. Figure 1 shows a sketch of the vertex-detector region of CLIC_ILD. For CLIC_SiD, a geometry with five single barrel layers and 7 single forward layers was chosen.

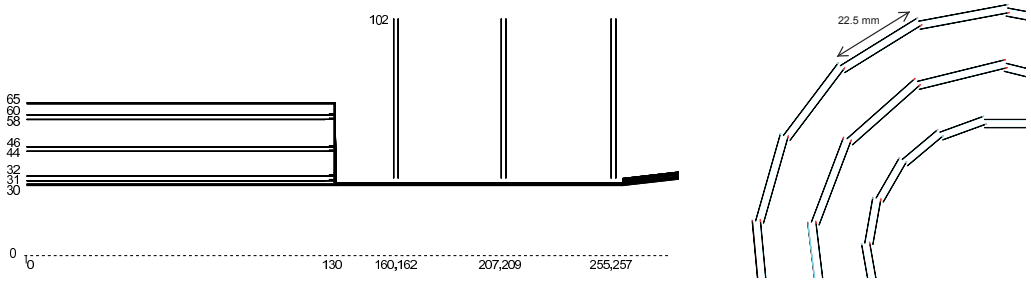

Figure 1: Sketch of the barrel and forward vertex region of the CLIC_ILD simulation model in the *z*-*r* plane (left) and of the barrel vertex region in the *x*-*y* plane (right). Shown are the double layers of the vertex barrel detectors and of the vertex endcap disks together with the barrel support shell and the central beam pipe. The dashed line corresponds to the detector axis. All values are given in millimetres.

For CLIC_ILD the central beryllium beam pipe is placed at a radius of 29 mm, while the larger magnetic field in CLIC_SiD leads to a larger suppression of low-pT charged particles from beam-induced background and therefore allows for a reduced radius of the beam pipe of 25 mm. Stainless steel conical sections with a wall thickness of 4 mm extend in the forward and backward directions and provide shielding against backscattering backgrounds.

The vertex-detector performance with the baseline geometries has been evaluated in benchmarking simulations. In addition, optimisation studies have been performed, to evaluate the effect of changes in the assumed pixel size, material budget, arrangement of sensitive layers and inactive material. The main performance measure in these studies is the impact-parameter resolution projected in the transverse plane $\sigma(d_0)$, which is closely linked to the flavour-tagging capability of the detectors. The resulting impact-parameter resolutions are as precise as 3μm for high-momentum tracks and the momentum resolution of the overall tracking systems reach the required value of $\sigma p_T/p_T^2 \approx 2\times10^{-5}\text{GeV}^{-1}$.

6. R&D on sensors and readout

The R&D on pixel sensors and readout is focussed on hybrid solutions, combining thinned high-resistivity fully depleted sensors with fast low-power and highly integrated thinned readout ASICs through low-mass interconnects. The target thickness for both the sensor and readout layers is only 50 μm each. Slim-edge sensor designs are under study and Through-Silicon Via (TSV) technology is implemented in the readout ASCIs, allowing for an efficient tiling to form larger modules with mimised inactive areas. The hardware R&D on sensors and readout is complemented by silicon signal simulations, to evaluate the impact of the technological parameters on the detector performance under various operation conditions.

6.1 CLICpix hybrid readout chips

Hybrid readout chips in 65 nm CMOS technology and targeted to the requirements of the CLIC vertex detectors are currently under development [7]. The 65 nm technology allows for smaller pixel sizes (10-30% less area for analog part, 60% less for digital part, compared to 130 nm technology) and more functionality in each pixel. In addition, lower noise due to the lower capacitances and improved radiation hardness are expected.

Analog and digital test structures of a commercial 65 nm CMOS process foreseen for the CLICpix readout chips have been produced and their performance and radiation hardness have been evaluated [8]. The results are in agreements with expectations from simulations. As an example, Tab. 1 lists the performance parameters extracted from measurements on preamplifier test structures and compares them to simulations. Good agreement between simulation and measurement is observed.

Table 1: Results of simulations and measurements on 65 nm CLICpix preamp test structures.

	Simulations	Measurements
Rise time	50 ns	65 ns
Gain	30 mV/ke$^-$	29.1 mV/ke$^-$
Linearity	5% at 16 ke$^-$	5% at 16 ke$^-$
Noise	55 e$^-$	$60-70$ e$^-$

The architecture of the CLICpix chips is based on the Medipix/Timepix chip family [9]. Figure 2 (left) shows the pixel block diagram. The pixel size is 25×25 μm. Simultaneous 4-bit Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements are implemented in each

pixel, allowing for a front-end time slicing with less than 10 ns and for analog readout to improve the position resolution. A photon counting mode allows for threshold equalization. A compression logic is implemented with three selectable readout modes: (1) No compression; (2) pixel-to-pixel compression; (3) pixel-, cluster- and column-based compression. The full chip can be read out in less than 800 μs (for 10% occupancy), using a 320 MHz readout clock. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm^2. The total average power consumption can be reduced to a value below the target of 50 mW/cm^2 by means of power gating for the analog part and clock gating. Figure 2 (right) shows the mask design for the CLICpix demonstrator chip, including a fully functional 64 $\times$ 64 pixel matrix. The chip has recently been submitted for production.

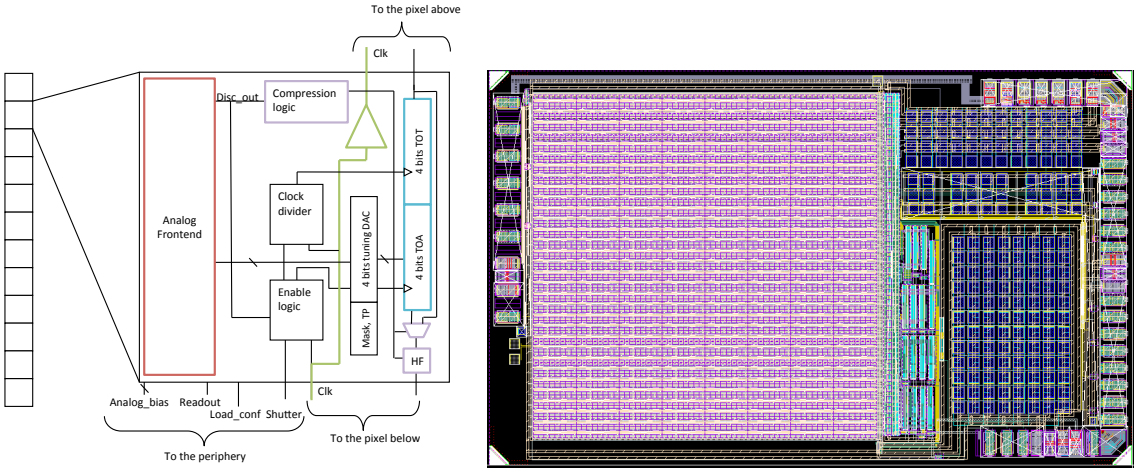

Figure 2: CLICpix pixel block diagram (left) and mask layout of demonstrator chip with 64x64 pixel array (right).

6.2 Through-Silicon Vias

A "via last" TSV process is under development in collaboration with CEA-LETI, aiming at demonstrating the feasibility of TSVs on functional detector chips from the Medipix/Timepix chip family [10]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology, which include TSV landing pads for the I/O circuitry, as well as dedicated TSV test structures at the periphery of the wafers.

The "via last" process proceeds in the following steps: (1) Deposition of the Under-Bond-Metalisation (UBM) on the front-side of the chips. (2) Temporary bonding of the front side to a support wafer and thinning from the back side. (3) Via etching and isolation. (4) Copper deposition and patterning of the via trenches. (5) Passivation and UBM on the backside. (6) De-bonding of the front-side support wafer and attachment of the back side to dicing tape.

Tests on the processed wafers show good results, with a low resistivity of the vias (<1 Ω) and a sufficient isolation to the outside (leakage current <1 μA at 1 V). Functional tests of the chips before and after TSV processing indicate no significant deterioration of the performance.

6.3 Simulation of signals in silicon

The CLIC vertex detectors require an unprecedented combination of thin sensors ($\approx 50\mu$m) with very small pitch (20-25 μm) and readout with fast shaping (< 50 ns). Monte-Carlo simulations and validations in test beams are required to study the signal development in the silicon sensors and extract parameters such as the charge rise time, collection efficiency, charge sharing between pixels and signal/noise ratio. The dependence on the type, momentum and incident angle of the particles and on the electric and magnetic field are studied using several different simulation and digitization frameworks:

- *Detailed TCAD simulation*. A detailed 3-dimensional microscopic simulation of the signal creation in the sensors is performed using the TCAD simulation framework [11]. The electric and magnetic fields are included in the simulation. This slow analytical approach is feasible only for small event samples and is used for the tuning of simpler models.

- *Monte-Carlo charge transport coupled to static TCAD simulation*. In this approach the electric field in the sensors is obtained from a static TCAD simulation. A Monte-Carlo simulation is used to create charge carriers and drift them in the electric field, taking into account diffusion and trapping effects and the Lorentz-angle due to the magnetic field [12, 13]. The simulation is fast and therefore suitable for obtaining sizeable event samples for direct comparison with test-beam data.

- *Geant4 simulation + Digitization model (Mokka/SLIC)*. Full-detector simulations based on Geant4 [17] and on parametric digitization models are used for the mass production of physics events within the CLIC detector-simulation frameworks Mokka [14] and SLIC [15]. The digitization models are tuned with the results from the detailed simulation approaches.

The combination of the electric and magnetic field in the sensors leads to a spread of the charge cloud due to the Lorentz-angle effect. This effect will be of particular importance in the very thin sensors foreseen for the CLIC vertex detector. For a p-in-n sensor with a resistivity of 10 kΩcm and a thickness of 50 μm, the depletion voltage is only $V_{dep} \approx 1$ V, leading to an average field in the sensors of only 200 V/cm. The resulting Lorentz angle between the direction of the electric field lines and the direction of the drifting charge carriers is 33° (7°) for electrons (holes), assuming a magnetic field of 4 T and a temperature of 27 °C [16]. For an increased operation voltage of 40 V, the Lorentz angle is reduced to 19° (6°) for electrons (holes). The result of a Monte-Carlo charge-transport simulation for these operation conditions is shown in Fig. 3. A minimum ionizing particle traverses the detector at perpendicular incident angle. The plots show the mean position of the created charge carriers in the x, y and z coordinate. A local coordinate system is used where the z axis is perpendicular to the sensor surface, pointing towards the back-side and with the origin located in the center of the sensor volume. The magnetic field of 4 T is applied in the x-direction, corresponding to a barrel geometry. The electrons (Fig. 3 left) reach the back side of the sensor ($z = 25$ μm) within 400 ps, while the holes (Fig. 3 right) take approximately 700 ps to reach the readout electrodes ($z = -25$ μm), due to their smaller mobility. The average displacement of the charge carriers in the y direction due to the Lorentz-angle effect is approximately 7 μm for electrons and 2 μm for holes. This displacement can be compensated for by rotating the sensor surfaces by the Lorentz angle.

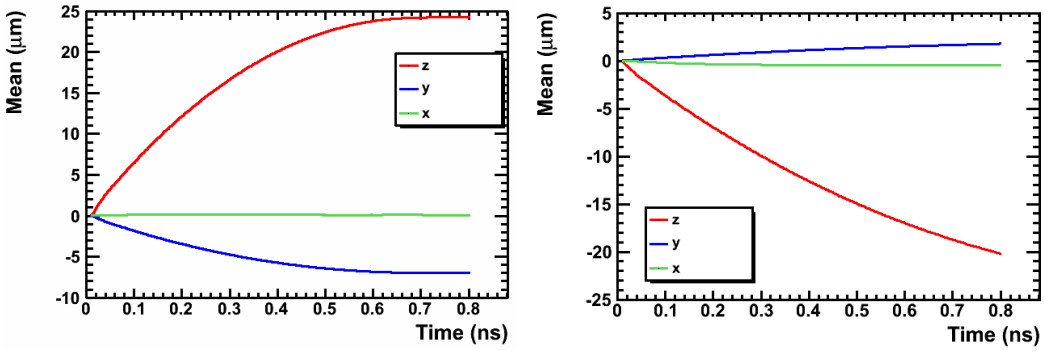

Figure 3: Mean position in the x, y and z coordinate for electrons (left) and holes (right), as obtained from the simulation of the carrier drift in a 50 μm thick fully depleted p-in-n sensor. A local coordinate system is used where the z axis is perpendicular to the sensor surface, pointing towards the back-side and with the origin located in the center of the sensor volume. A voltage of 40 V and a magnetic field in the x direction of $B_x = 4$ T are applied in the simulation.

7. Detector integration

The detector-performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components. The powering, cooling, mechanical supports and the service lines are therefore addressed in an integrated approach already at an early stage in the detector-design phase.

7.1 Powering

The ambitious power-consumption target of less than 50 mW/cm^2 in the vertex detectors can only be achieved by means of pulsed powering, taking advantage of the low duty cycle of the CLIC machine. The main power consumers in the readout circuits will be kept in standby mode during most of the empty gap of 20 ms between consecutive bunch trains. Furthermore, efficient power distribution will be needed to limit the amount of material used for cables. Both the power pulsing and the power-delivery concepts have to be designed and thoroughly tested for operation in a magnetic field of 4-5 T.

A powering scheme based on DC/DC converters, Low Drop-Out regulators (LDOs) and local energy storage with silicon capacitors has been proposed for the power delivery and power pulsing of the CLIC vertex detectors [18]. The scheme takes advantage of the low duty cycle of the CLIC machine, to limit the current and thereby the cabling material needed to bring power to the detectors.

Figure 4 shows the time structure of the CLIC collisions and the time dependence of the power consumption in the CLICpix readout chips for both the digital and analog components in one ladder of the barrel vertex detector, consisting of 24 readout chips covering a surface area of approximately 24 cm^2. The nominal operation voltage for both the analog and digital components in the chips is 1.2 V. Collisions occur only during 156 ns every 20 ms. The minimum time needed with stable conditions in the analog components is approximately 15 μs, in which both digital and analog power are at their peak values of 48 W and 2.4 W, respectively. The rise and fall times can be tuned by design of the readout chips within certain limits and are both assumed to be of the

order of 1 μs. During the remaining time of the 20 ms cycle the analog power can be switched off. For the digital components, on the other hand, an average continous power of 0.54 W per ladder is still required, in order to sequentially send the data off detector and keep the chips in a standby mode.

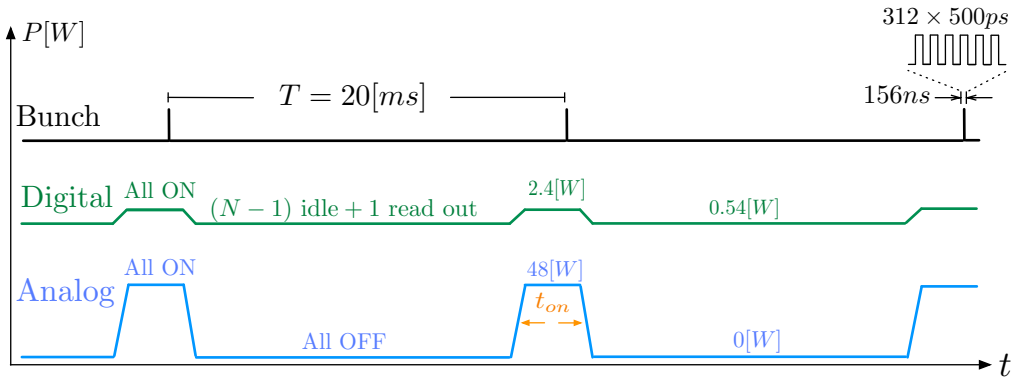

Figure 4: Time structure of the CLIC collision and time dependence of the digital and analog power consumption for one barrel-vertex detector ladder equipped with N=24 CLICpix readout chips. The time t_{on}, in which both the digital and analog parts will be at peak power, corresponds to approximately 15 μs.

It is assumed that each of the barrel vertex ladders will receive analog power from either side, resulting in units of 12 CLICpix chips per half ladder, with a total surface area of approximately 12 cm^2, connected to one power-supply channel. Figure 5 shows a sketch of the proposed powering scheme for the analog components of one half ladder in the barrel vertex detector. Back-end power supplies located off-detector create a continuous voltage of 10 V that is converted to 3.3 V in the DC/DC converters located outside the inner vertex region. Flex cables consisting of aluminum conductors on a Kapton substrate bring the power to LDOs mounted on the individual CLICpix chips of the half ladder. The LDOs are only operated during 250 μs around the 15 μs acquisition time. Low-mass silicon capacitors at the input and output of each LDO of 10 μF and 1 μF, respectively, are used for local energy storage and to achieve a stable output voltage of 1.2 V during the 15 μs.

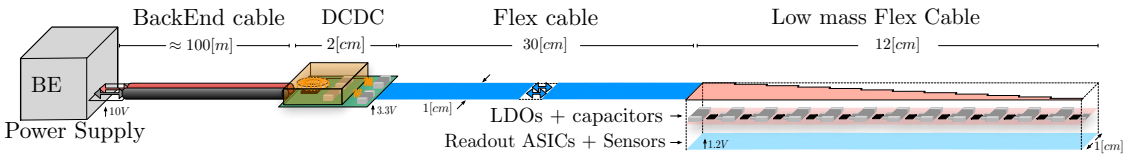

Figure 5: Powering scheme for the analog components of one half ladder in the barrel vertex detector, consisting of 12 CLICpix readout chips.

The average contribution of the flex cable, the LDOs and the silicon capacitors to the material in the ladder area corresponds to 0.145%X_0. The use of thinner conductors and future improvements of the silicon-capacitor technology are expected to decrease the material budget even further. Measurements on a prototype show that the voltage drop during the acquisition time is below the 20 mV required for a stable operation of the CLICpix chips. The measurements are in agreement with equivalent-circuit simulations. The average analog power is 4.6 mW/cm^2, well below the tar-

get value of 50 mW/cm^2 for the total power and therefore leaving enough margin for the power consumption of the digital components.

7.2 Mechanical integration

Low-mass mechanical solutions are required to provide sufficient support for the sensors, the readout chips and the cabling infrastructure, while leaving enough clearance for air flow cooling. Moreover, realistic assembly and in-situ testing scenarios need to be developed.

A support system based on half shells made of carbon fiber composite material is currently being designed. Figure 6 (left) shows the result of an ANSYS finite element analysis [19] of the deformation of a 180 μm thick Carbon-Fiber-Reinforced Polymer (CFRP) support half shell for the CLIC_ILD vertex barrel layers under its own weight. The simulated maximal static deformation is at an acceptable level of 2.7 μm and the first eigen frequency is 215 Hz.

7.3 Cooling

A total power of approximately 500 W will be dissipated in the vertex detectors alone. The small material budget for the inner tracking detectors constrains severely the permitted amount of cooling infrastructure. For all pixel layers, forced air-flow cooling is therefore foreseen.

Feasibility studies have been performed for an inner-detector cooling system with sufficient heat removal capability. A spiral arrangement of the endcap pixel disks allows for air flow through the disks on one side, into the barrel region and out through the endcap-disks on the other side. Figure 6 (right) shows the resulting temperature profile in the pixel detector layers, obtained from an ANSYS finite element simulation. With an air temperature of 0 °C and an average flow velocity of 11 m/s at the inlet, the temperature in the innermost barrel layer reaches up to 40 °C and stays below 30 °C in the other layers. The temperature span between inlet and outlet is approximately 15 °C. Heat transfer through conduction has not been taken into account in the simulation.

Further R&D is required to demonstrate the feasibility of this air-flow cooling scheme. Possible vibrations arising from the high flow velocities are of particular concern.

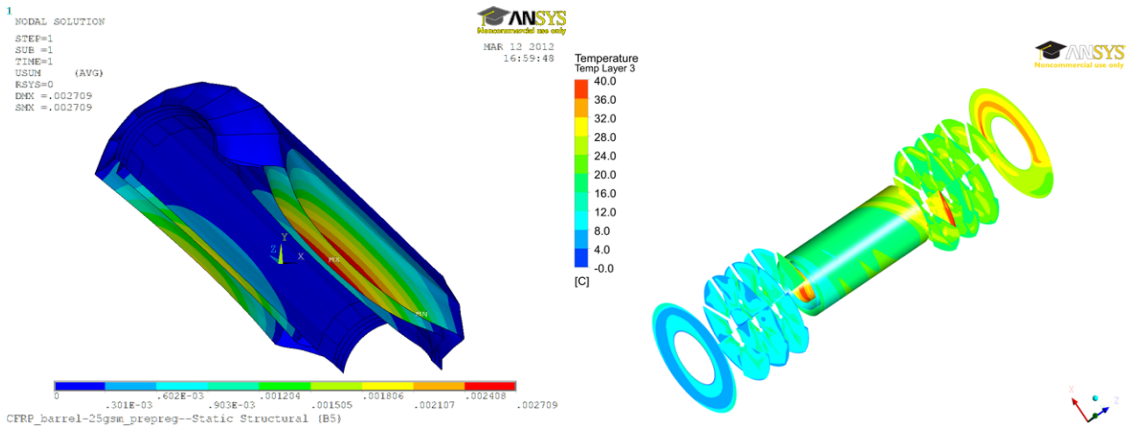

Figure 6: Finite element simulations: static deformation of a 180 μm thick carbon-fibre support shell (left) and temperature profile in the CLIC_ILD barrel and endcap pixel detectors, assuming cooling with forced air flow (right).

8. Conclusions

The CLIC machine environment and the requirements for precision physics measurements place challenging demands on the vertex-detector systems. Initial detector layouts meeting these demands have been proposed. An active R&D program on sensor and readout technologies, simulation, power delivery and power pulsing, mechanical integration and cooling is in place.

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