PROCEEDINGS OF SCIENCE

Belle Tracker Upgrade

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The ongoing upgrade of the KEKB accelerator (SuperKEKB) will increase the instantaneous luminosity by a factor of 40. The Belle detector is upgraded in parallel to offer, among many other improvements, precise vertexing performance at the high luminosity and background of SuperKEKB. Two layers of pixel detectors based on the DEPFET technology and four layers of double-sided silicon strip detectors will provide a low mass vertex detector for the Belle II experiment.

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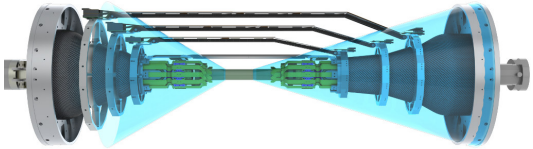

Figure 1: Asymmetric acceptance of the Belle II tracker (cyan), due to the asymmetric beam energies. The DEPFET pixel detector in the middle and 4 layers (1 straight, 3 slanted) of silicon strip detectors are shown.

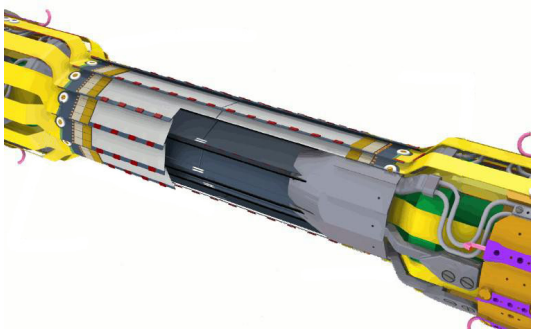

Figure 2: Outer and inner layer of the DEPFET pixel detector mounted on the cooling block and arranged around the beam pipe with overlapping ladders.

1. Introduction

The Belle experiment [1] at the KEK laboratory in Tsukuba (Japan) has been operated successfully for 10 years in the field of B physics. Its asymmetric accelerator KEK-B collided electron and positron beams (8 and 3.5 GeV respectively) and achieved the world record luminosity of $2.11 \times 10^{34} cm^{-2} s^{-1}$ in e+e- collisions. An integrated luminosity of $1 ab^{-1}$ has been recorded by the Belle experiment, mostly at the $\Upsilon(4S)$ resonance. This data allowed the precise study of CP violation and of the CKM matrix elements and proved, together with the BaBar experiment, the validity of the Standard Model, incorporating CP violation as formulated by Kobayashi and Maskawa.

Despite the success of the Belle experiment, the observation of rare processes and the requirement of high statistics to increase the precision further and clarify possible 'tensions' in the SM requires an upgrade of the accelerator. The new SuperKEKB machine ($7 GeV\ e^-$, $4 GeV\ e^+$) will increase the instantaneous luminosity by a factor of 40 compared to KEKB and will ultimately reach $8 \times 10^{35} cm^{-2} s^{-1}$. This increase is achieved by the nanobeam scheme[2], where the beam size at the interaction point is reduced to a cross-section of $10 \mu m \times 60 nm$.

The high luminosity imposes higher occupancies and radiation doses on the detector. As the Belle Silicon Vertex Detector was already at its performance limit, an upgrade is required to cope with the high luminosity environment. All sub-detectors are refurbished to form the new Belle II detector [2], which is to be commissioned in 2015. Time-dependent measurement of CP violation requires excellent vertexing performance. The old Belle vertex tracker is replaced by two layers of DEPFET pixels and surrounded by four layers of double-sided strip detectors (DSSD) (fig. 1) to increase the z-vertex resolution by a factor of two.

2. DEPFET Pixel Detector (PXD)[1]

The DEPFET technology [3] uses a fully depleted high ohmic silicon bulk for signal genera-

[1]Work supported by the German Ministerium für Bildung, Wissenschaft, Forschung und Technologie (BMBF) under contract no. 05H12VHH.

Layer	Radius	#ladders	Length	Ladder active	Pixel size (μm^2)
1	14mm	8	2×68mm	2×45mm	50×55 and 50×60
2	22mm	12	2×85mm	2×62mm	50×70 and 50×85

Table 1: Parameters of 15mm wide Belle II DEPFET pixel detector ladders.

tion. A generated signal electron drifts into a collection electrode ('internal gate') located underneath a FET transistor in the pixel cell. This transistor is a first amplification stage, which allows a low noise amplification. The FET current is modulated by the signal charge accumulated in the internal gate. The charge has to be removed after read-out by a positive voltage pulse on a clear contact placed in each pixel.

The pixel detector is mounted close to the interaction point in the high background environment. It can keep the occupancy at 1% by a fast read-out speed and fine granularity, yielding a good vertex reconstruction. A low material budget is achieved by a thinning process and the use of the all-silicon module approach to limit the multiple scattering. The DEPFET technology is an excellent tracking device because of the high signal to noise ratio caused by the low noise amplification and the large signal of the fully depleted bulk.

2.1 Ladder Design

The Belle II DEPFET pixel detector consists of two concentrical barrels around the 10mm radius beam pipe. The 15mm wide DEPFET ladders are overlapping to cover inactive areas of the ladder frame and to allow alignment. The ladder itself is built by glueing two half modules (fig. 3) with 250×768 pixels together, forming a self-supporting structure, which is mounted at the ends onto a support and cooling block residing on the beam pipe (fig. 2). This self-supporting structure eliminates additional mechanical support and introduces a minimum of material into the acceptance. Steering and read-out chips outside of the acceptance connect to the detector silicon without interposers by flip-chip technology.

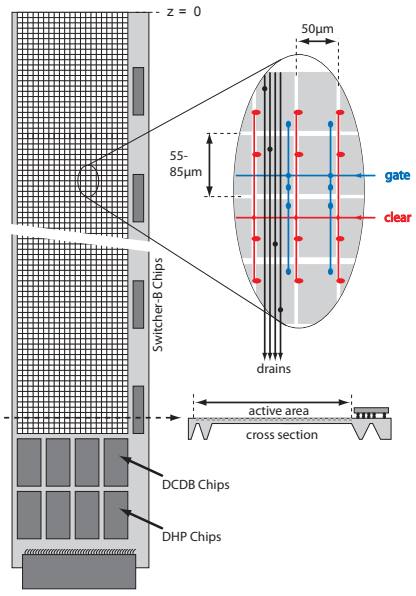

Figure 3: Layout of a DEPFET all-silicon half module. The cross section is showing the thinning principle.

The active pixel area is thinned [4] down to $75\mu m$, while the $450\mu m$ thick frame is only partially thinned to keep the ladder mechanically stable while reducing the material. This configuration allows a low mass detector with an average radiation length of $0.18\%X_0$ per layer. Table 1 lists the layer parameters. Due to the asymmetric angular acceptance of the detector from 17° to 155°, the two layers have different lengths and pixel sizes.

2.2 Cooling

A low material budged is mandatory due to the low momentum of particles at SuperKEKB.

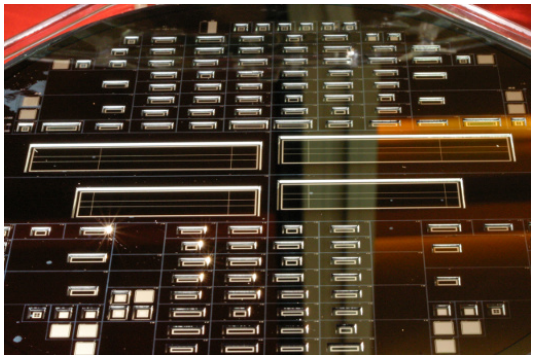

Figure 4: Backside of the PXD6 wafer with $50\mu m$ thin matrix areas on a $450\mu m$ thick substrate

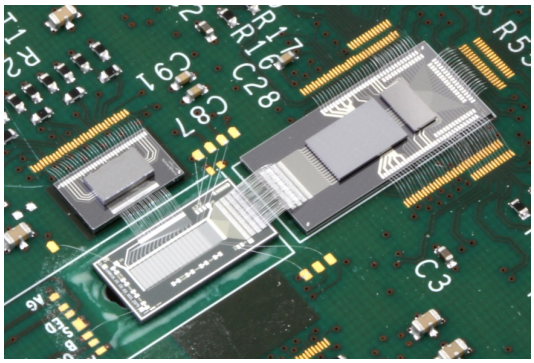

Figure 5: Hybrid system for lab- and beam-tests with small DEPFET matrix (middle) and Switcher and DCD chips on wire bond adapters.

Active cooling of the devices within the acceptance should be avoided to limit the multiple scattering. The steering chips are located on the support frame along the DEPFET pixel matrix within the acceptance. The total power dissipation of 40W of all steering chips (Switcher) and pixel matrices are cooled by dry cold air blown inbetween the two layers (-20°C, $v_{air} = 1m/s$). Much more heat (320W) is generated at the end of the modules by the read-out chips. The support and cooling block, where the modules are mounted to, is manufactured in a sintering process and contains channels for a closed two-phase evaporative CO_2 cooling system, which removes the heat from the module ends directly ($T_{block} = -20°C$). This stainless steel block is located outside of the acceptance and thus doesn't contribute to the material budget.

2.3 Sensor Read-out

Each half ladder is read out individually within $20\mu s$ in rolling-shutter[2] mode. The Switcher chips, located on the lateral balcony, provide fast row-enable and clear signals to the matrix. Each Switcher signal is connected to four pixel rows for an increased parallelism and read-out speed. A load capacitance of 50pF needs to be cycled within 10ns to achieve the 100ns row read-out time. Voltages of up to 27V have to be handled by the chip. The DEPFET drain currents are digitized by 8-bit cyclic ADCs of the Drain Current Digitizer (DCD) chips [5]. A DCD connects to 256 drain lines and includes 512 ADCs. Two ADCs are digitizing alternatingly to achieve low noise of 50nA at the desired row rate. The chip is running at 320MHz and generates a data rate of ≈82Gbps per half module, which is reduced by the Data Handling Processor (DHP) chips [6] to 5Gbps. The DHP subtracts pedestal values, corrects for common mode noise and applies hit finding.

A 50cm long kapton cable connects the silicon module with a passive patch panel. From there the data is transmitted over ≈20m twisted pair cables to a Data Handling Hybrid (DHH), where it is converted to optical links connected to the DAQ based on the Advanced Telecommunications Computing Architecture (ATCA) system [7]. More data reduction is performed in the ATCA by a region of interest finding algorithm implemented in FPGAs. The excellent spacial resolution of the pixel detector is accompanied by a long integration time of $20\mu s$. Many off-time background hits, mostly from irreducible QED background, increase the data volume of the PXD significantly. With

[2]consecutive row-wise read-out

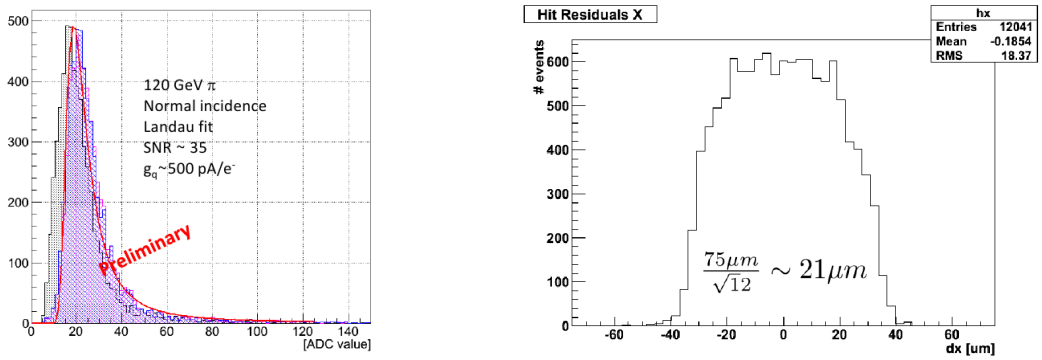

Figure 6: 2012 CERN SPS test beam results: S/N=35, 18μm center-of-gravity residuals

the help of the strip detector, which has a low occupancy due to its fast timing, the background can be efficiently removed in the ATCA system by extrapolating tracks from the SVD into the PXD.

2.4 Prototype tests

With the DEPFET test wafer production (PXD6) several pixel design options are available to evaluate the optimum layout for the Belle II PXD. The PXD6 is a milestone, as it is the first ever DEPFET production with 50μm thin DEPFET matrices (fig. 4). Matrices with 64×32 pixels are connected to the close-to-final Switcher and DCDB chips and are operated at full read-out speed of 100ns/row on hybrid PCBs. A complex setup (see fig. 5) is required, because the ASICs are designed for flip-chip interconnection, but the matrices need to be wire bonded. Wire bond adapters carry the ASICs and connect to the matrix by wire bonds.

These hybrid assemblies were evaluated in the laboratory and in beam tests. Figure 6 shows results of the 2012 campaign at the CERN SPS with 120GeV pions: A signal-to-noise ratio of 35 and center-of-gravity residuals of 18μm were measured.

2.5 Electrical Multi-Chip Module (E-MCM)

Another milestone is the production of the Electrical Multi-Chip Module (E-MCM, fig. 7), which is the first full size half-module electrical layout ('Everything except the DEPFET'). Its purpose is to evaluate the ASICs performance on module level and to exercise the complex layout, production, thinning, assembly and operation of a module. Active DEPFET pixels are replaced by test structures, which reduces the production time significantly.

3. Double-Sided Strip Detector (SVD)

The silicon vertex detector (SVD) of the old Belle detector was based on four layers of double-sided silicon strip sensors. It was operated close to its limits in terms of occupancy and read-out speed. With the 40x increase in luminosity of SuperKEKB, the SVD had to be redesigned to tolerate the high background environment.

The SVD of Belle II uses an improved read-out scheme and a redesigned front end. The four layers are shifted to higher radii and surround the DEPFET PXD.

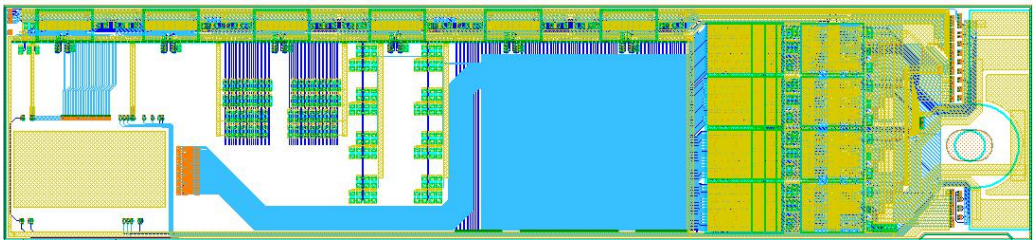

Figure 7: Layout of the E-MCM half module containing everything but active DEPFETs. The inactive area is filled with test structures.

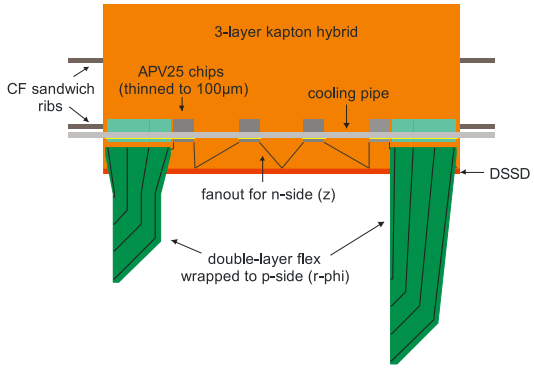

Figure 8: Top view of kapton flex hybrid with pitch adapters to the sensor n-side. Ten APV25 chips are aligned and cooled by a single pipe. Wrap-around flex connects to the sensor p-side.

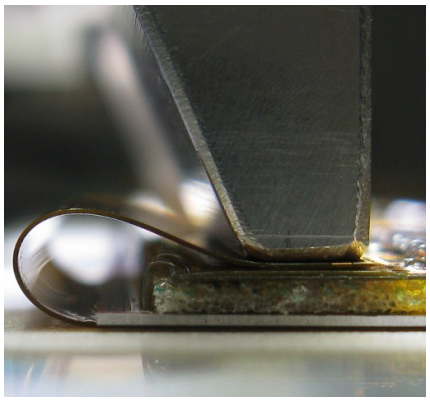

Figure 9: Origami concept: Kapton flex is wrapped around and fixed by a tool during glue curing. It connects the sensor back side to the APV25 chips on the front side. Sandwich structure: kapton hybrid (top), Airex foam and sensor.

3.1 Ladder Design

The future SVD will have a slanted forward part (fig. 1) on the three outermost layers. The slant is introduced to accommodate the asymmetric energies of SuperKEKB beams which results in a boost in forward direction. The slanted forward part increases the spacial resolution and reduces the material budget, the required sensor area and the number of channels, at the cost that the mechanical support structures become more complex.

Up to five sensor assemblies are mounted on two carbon fiber support ribs. A lightweight and low mass sandwich structure of styrofoam (Airex) inbetween two layers of 100μm thin carbon fibers is laminated to form the rib. The sensor assembly itself is also a sandwich structure: A 1mm thick Airex foam insulates the sensor electrically and thermally from a kapton flex hybrid. Figure 8 shows the kapton hybrid with the fan-out for the sensor n-side. Ten aligned APV25 chips, thinned to 100μm, are sitting on top of the readout flex and are CO_2 cooled by a single pipe. The wrap-around flex connects the read-out chips on the front side with the strips on the back side. This 'Origami' concept is shown in figure 9. Origami and chip-on-sensor concepts are used for the inner sensors, while the first and last sensors of a ladder use conventional read-out hybrids located outside the acceptance.

Three types of 12.3cm long, 320μm thick sensors are used. Two types of rectangular devices

are manufactured by Hamamatsu Photonics (Japan) with a width of 3.8cm for layer 3 and 5.8cm for layer 4-6. The trapezoidal sensor for the slanted forward part is produced by Micron Semiconductor (UK) with a width of 3.8 to 5.8cm.

The use of lightweight materials in sandwich structures and thin ASICs reduce the material of the silicon vertex detector to an averaged radiation length of only $0.55\%X_0$ per ladder.

3.2 Cooling

The power dissipation of 350mW per APV25 is cooled by a single, directly attached pipe running across all chips of a Origami module. The 1.6mm diameter pipe with $100\mu m$ wall thickness adds a minimum to the material budget, while withstanding a large safety margin beyond the operating pressure of 20bar. An improvement in S/N of $\approx 15\%$ is achieved by cooling to -20°C compared to room temperature. Evaporative CO_2 cooling will be used to remove the total of 650W dissipated by the SVD. A common cooling concept of PXD and SVD is established, sharing infrastructure and cooling plant.

3.3 Sensor Read-out

The old SVD daisy-chained the strips of up to three sensors and used the VA1TA [9] chip to read out at the edges, outside the active area. This configuration suffered from slow shaping and high dead time. The VA1TA chip is replaced by the APV25 chip [10], which fits the needs of Belle II. It was originally designed for the CMS experiment and offers a fast shaping time of 50ns, compared to the 800ns of the VA1TA. The dead time is removed by the 192 cell pipelined architecture of the APV25, which stores subsequent triggers while reading out previous events.

The APV25's multi-peak mode allows to take multiple samples of the shaping curve, which is used off module to remove off-time background hits by online processing in FPGAs. This hit time reconstruction algorithms [11] and the fast shaping time reduces the occupancy by a factor of 100 compared to the VA1TA.

A drawback of the APV25's fast shaping is the input load dependent noise. The load capacitance needs to be reduced to maintain a good S/N. A daisy chaining of strips would increase the noise unacceptably. The read-out chips have to be placed close to the strips to limit the parasitic capacitance of fan-out structures. This is accomplished by the chip-on-sensor and Origami concepts.

The APV25 is connected by 2m of cable to patch panels, which contain passive components and radiation hard DC/DC converters. 10m of cable connect the analog APV25 output signals to VME systems with custom built 'FADC' modules for digitalization, FIR filtering, pedestal subtraction and zero suppression. Peak time and amplitude are obtained by comparing the measured waveform against pre-loaded values in look-up tables. Optical fibers transmit the reduced data to the common Belle II DAQ and also to the PXD's ATCA system for pixel data reduction (see above).

3.4 Prototype tests

Small test sensors with different p-stop layouts were characterized before and after irradiation with 700kGy of ^{60}Co gammas to identify the optimal layout in terms of signal-to-noise ratio. The atoll type layout has been identified as optimal and is used as a baseline for production [12].

Several full-size Origami modules were built and characterized in the laboratory and in beam tests. A signal-to-noise value of 14 was achieved for the p-side (long strips and Origami wrapping) and 23 for the n-side (short strips and small fan-out) at -10°C.

4. Summary

The upgrade of the KEKB accelerator to SuperKEKB will increase the instantaneous luminosity by a factor of 40. An upgrade of the Belle detector is mandatory to achieve the high precision required to fulfill the physics program. The vertex detector is upgraded together with other detector subsystems and is to be commissioned in 2015.

Two layers of DEPFET pixels together with four layers of double-sided silicon strip sensors will replace the old Belle vertex tracker. The pixelated inner two layers can accommodate the high luminosity induced occupancy and provide a precise position information. The all-silicon self supporting module concept with a only $75\mu m$ thin active area features a low radiation length of $0.18\%X_0$ and minimizes the multiple scattering of the low momentum tracks of SuperKEKB. The improved four layers of double-sided silicon strip sensors reduce the occupancy by a factor of 100 by utilization of the APV25 chip together with hit time reconstruction. A low material budget of $0.55\%X_0$ is achieved with the Origami chip-on-sensor concept together with lightweight support structures. The slanted forward part of the Belle II SVD improves the data quality while reducing the number of channels.

The Belle II vertex detector's PXD and SVD build a high accuracy tracking device which improves the z-vertex resolution significantly by a factor of two to $15\mu m$ compared to the previous Belle tracker.

References

[1] A. Abashian, et al., *The Belle Collaboration*, *Nucl. Instr. and Meth.* A479 (2002) 117

[2] T. Abe, et al., *Belle II Technical Design Report*, *KEK Report* 2010-1, arXiv:1011.0352v1 [physics.ins-det]

[3] J. Kemmer, G. Lutz, *Nucl. Instr. and Meth.* A253 (1987) 365.

[4] H.-G. Moser, L. Andriček, R. Richter, G. Liemann, *Thinned Silicon Detectors*, *PoS*(Vertex 2007) 013

[5] I. Peric, et al., *DCD - The Multi-Channel Current-Mode ADC Chip for the Readout of DEPFET Pixel Detectors*, *IEEE Trans. Nucl. Sci.* vol. 57 p.743 doi:10.1109/TNS.2010.2040487

[6] M. Lemarenko, et al., *The Data Handling Processor for the Belle II Pixel Vertex Detector: efficiency optimization* , 2012 JINST 7 C01069 doi:10.1088/1748-0221/7/01/C01069

[7] H. Xu, et al., *An ATCA-based High Performance Compute Node for Trigger and Data Acquisition in Large Experiments*, *TIPP2011* doi:10.1016/j.phpro.2012.02.509

[8] T. Bergauer, *The Silicon Vertex Detector of the Belle II Experiment*, *PoS*(VERTEX2010) 044

[9] Gamma Medica – Ideas AS (Norway), `www.ideas.no`

[10] M. French, et al., *Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker*, *Nucl. Instr. and Meth.* A466 (2001), 359-365

[11] C. Irmler, M. Friedl, M. Pernicka, *Online data processing and hit time reconstruction for silicon detector readout*, *Nucl. Instr. and Meth.* A617 (2010) 280

[12] M.Valentan et al., *Optimization of Strip Isolation for Silicon Sensors*, *Physics Procedia* **37** (2012) 891–898