

## The ATLAS Pixel Insertable B-Layer Project (IBL)

---

**Martin KOCIAN\***

*on behalf of the ATLAS IBL collaboration*

*SLAC National Accelerator Laboratory*

*E-mail: [kocian@slac.stanford.edu](mailto:kocian@slac.stanford.edu)*

The IBL (Insertable B Layer) is a new innermost layer for the ATLAS Pixel Detector to be installed in the LHC shutdown of 2013-2014. It consists of 14 staves at a radius of 3.2 cm and provides coverage for  $|\eta| < 2.5$ . The sensors with a pixel size of  $50 \mu\text{m} \times 250 \mu\text{m}$  are 75 % planar devices and 25 % 3D devices. They are bump bonded onto the new FE-I4 readout chip with a size of 20 mm x 19 mm. The modules are mounted onto staves made of a foam filled carbon fiber shell. The total added material amounts to 1.9 % X0. The components as well as the integration, installation, and testing of the IBL are presented here.

*The 21st International Workshop on Vertex Detectors*

*16-21 September 2012*

*Jeju, Korea*

---

\*Speaker.

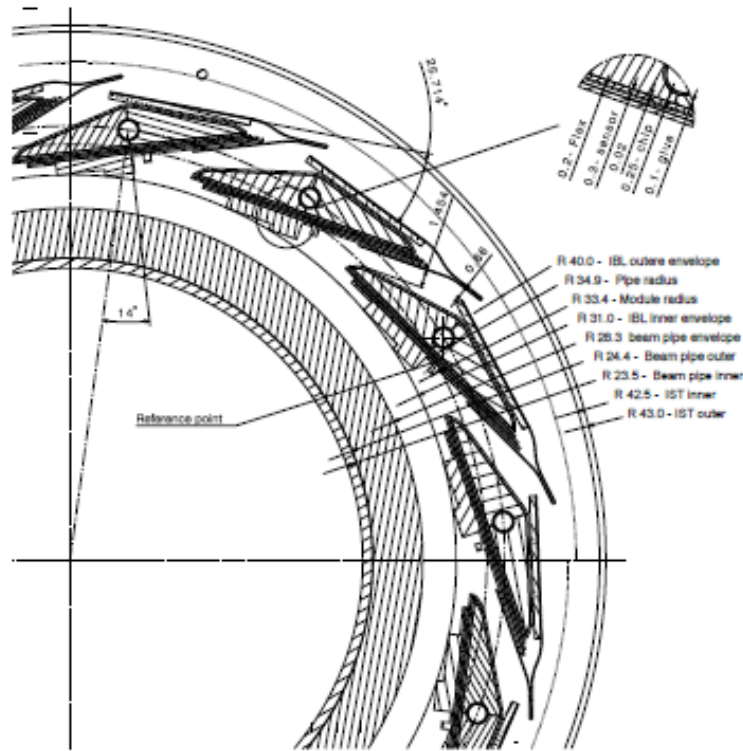


Figure 1: Section of the IBL [7].

## 1. Introduction

The current Pixel Detector [1] of the ATLAS experiment [2] is intended to be used until the end of LHC phase I in 2022 up to instant luminosities of around  $\mathcal{L} = 2.2 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . Due to the high pile-up of minimum bias events at those luminosities the b-tagging performance of ATLAS will be seriously impacted. Also the inefficiency of the innermost layer will reach around 5 % due to high occupancy in the readout chips. In order to provide significant improvement to the vertexing and tracking of the ATLAS detector a 4<sup>th</sup> innermost pixel layer will be installed during LS1 (Long Shutdown 1) in 2013-2014. This new pixel layer is called Insertable B-Layer (IBL). It will be inserted between the beam pipe and the current pixel B-layer at a radius of 3.2 cm. The new layer consists of 14 staves which are arranged in a turbine-like fashion (see figure 1 [7]). To

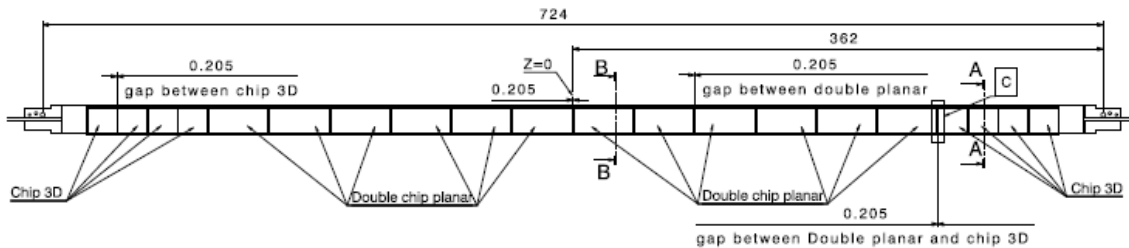


Figure 2: Drawing of an IBL staff [4].

	Planar	3D
Vendor	CiS	FBK/CNM
Wafer Thickness	200 $\mu\text{m}$	230 $\mu\text{m}$
Size in FE chips	2	1
Depletion voltage before irradiation	35 V	15 V
Depletion voltage at end of life	1000 V	180 V

**Table 1:** Comparison of parameters between planar and 3D IBL sensors.

achieve full coverage in  $\varphi$  (azimuthal angle with respect to the beam pipe) the staves are tilted by  $14^\circ$  and overlap. In  $z$  (direction along the beampipe) no shingling is possible because of the lack of clearance.

Each staff contains 12 double-chip sensors in planar technology and 8 single-chip sensors in 3D technology. The single-chip sensors are located on the outsides of the staff. The readout is done through 32 FE-I4 frontend chips. Each frontend is about 2 cm x 2 cm in size which means that the active area of a staff is about 2 cm x 64 cm. The inactive area between two sensors is about 450  $\mu\text{m}$ . A drawing of the staff is shown in figure 2 [4]. The IBL provides coverage in  $|\eta| < 2.5$ .

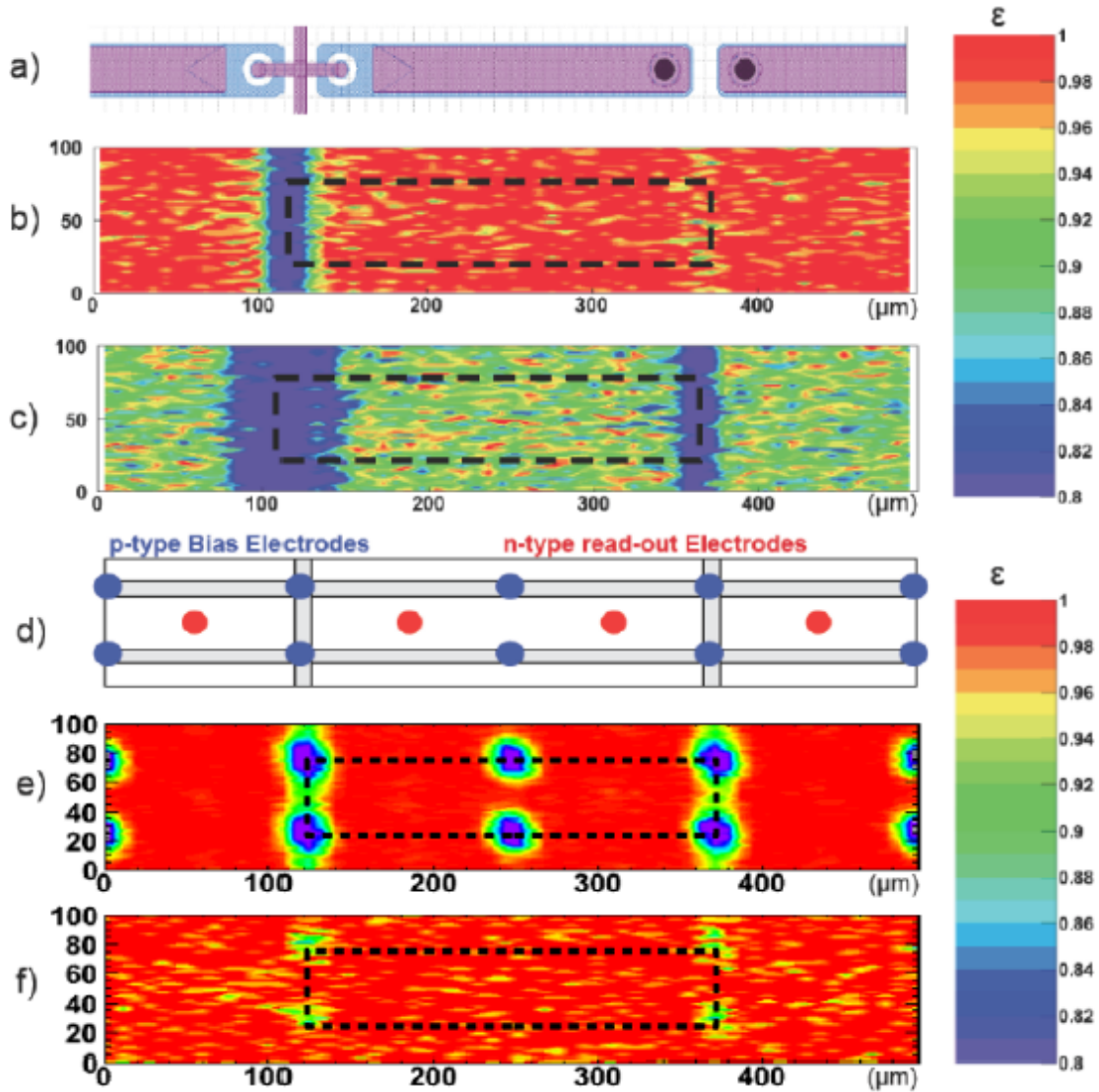
The total amount of material added by the IBL is less than 1.9 %  $X_0$ , compared to the current pixel layers at 3 %  $X_0$ . The need for the IBL to last to the end of phase 1 at a total integrated luminosity of  $550 \text{ fb}^{-1}$  translates into a radiation hardness requirement of 250 MRad TID and  $5 \cdot 10^{15} \text{ n}_{eq}/\text{cm}^2$  NIEL.

In order to make space for the IBL a new beam pipe with a radius of 23.5 mm will be installed together with the IBL. A detailed description of the IBL can be found in [3][4].

## 2. Sensors

Two sensor technologies were proposed for the IBL: Planar n-in-n sensors of the same type that was used for the present ATLAS detector, and 3D sensors, which are a technology that has not been used in a high-energy physics experiment to date. In 3D sensors the electrodes are columns in the silicon [5]. There can be varying numbers of electrodes per pixel which will have an influence on charge collection and noise. For IBL a design with two electrodes per pixel was chosen. While planar sensors are a proven technology that can be produced with a very high yield (90 % for IBL) at a reasonable cost 3D sensors have a number of advantages like fast charge collection and good radiation hardness, and they can be operated at a much lower depletion voltage. As the IBL production yield of 62 % shows 3D technology has achieved a level of maturity that makes it a viable option for the implementation of pixel detectors today.

The properties of the sensors are summarized in table 1. Both sensor types have a slim edge of 200  $\mu\text{m}$  which is needed to avoid gaps in the coverage in  $z$  since shingling of the sensors in  $z$  is not possible for IBL. Instead of choosing one technology over the other it was decided in the end to use a mix of sensors: 75 % planar in the center of each staff, and 25 % 3D on the outsides.



**Figure 3:** Cell efficiency maps: a) lithography sketch for planar sensor, b) and c) 2D efficiency maps for a planar sensor at 1000V (mean efficiency 96.9 %) and at 600V (mean efficiency 86.4 %) using  $15^\circ$  inclined tracks, d) lithography sketch for 3D, e) the 2D efficiency map for a 3D module using normal incident tracks (mean efficiency 97.5 %) and f) the 2D efficiency map for the 3D module using  $15^\circ$  inclined tracks (mean efficiency 99 %). 3D modules are operated at a bias voltage of 160V [7].

Testbeam studies of the sensor efficiency have been performed for planar and 3D sensors both before and after irradiation with neutrons at a level of  $5 \cdot 10^{15} \text{ n}_{eq}/\text{cm}^2$  that corresponds to the end of the projected life of the IBL. For planar sensors the efficiency is 99.9 % before irradiation. After irradiation the efficiency is still 96.9 % when running at a bias voltage of 1000 V, with an efficiency gap in the region of the bias grid (see figure 3 b and c) [7]) and 86.4 % at a bias voltage of 600 V. At higher  $\eta$  this localized inefficiency smears out since the tracks do not cross the sensor perpendicularly.

For 3D sensors there is a dependence of the efficiency on angle since particles going directly through the electrodes do not produce hits. For IBL this configuration is, however, not relevant because the staves are mounted at an angle. The efficiency at an IBL-like inclination of  $15^\circ$  is 99.9 % like for the planar sensors. After irradiation at an IBL fluence of  $5 \cdot 10^{15} \text{ n}_{eq}/\text{cm}^2$  the efficiency no longer fully recovers when tilting the sensor due to the lower overall charge collection. The total efficiency after irradiation is 97.5 % at normal incidence (figure 3 e) and 99 % at an inclination of  $15^\circ$  (figure 3 f). A more detailed description of 3D irradiation results can be found in [6]. For a comprehensive article on the results for irradiated planar and 3D IBL modules see [7].

### 3. Frontend ASIC

The frontend readout chip for IBL is the FE-I4. It was executed in IBM 130 nm technology. One ASIC contains 26,880 pixels which are arranged in 80 columns in  $z$  and 336 rows in  $\phi$ . The size of one pixel is  $250 \mu\text{m} \times 50 \mu\text{m}$ .

A crucial new feature of this chip with respect to the FEI3 readout chip used in the present ATLAS Pixel Detector is that the hits are stored in the pixel cells. A hit is only read out if a trigger request matches its timestamp. Otherwise the hit is deleted. This reduces bandwidth use and power consumption inside the chip and allows for far higher occupancies. The deadtime for a pile-up of 80 events ( $\mathcal{L} = 3 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ ) is therefore only 0.6 %. The chip provides 4-bit time-over-threshold information for each hit. To reduce data size the data of two neighboring pixels in  $\phi$  are sent out in a single 24-bit hit record. The readout rate for IBL is 160 Mb/s. To improve the data transmission quality the data is DC balance through 8b10b-encoding.

The version of the ASIC that will be used for IBL is the FE-I4B which has some bug fixes and additional features compared to the FE-I4A prototype version:

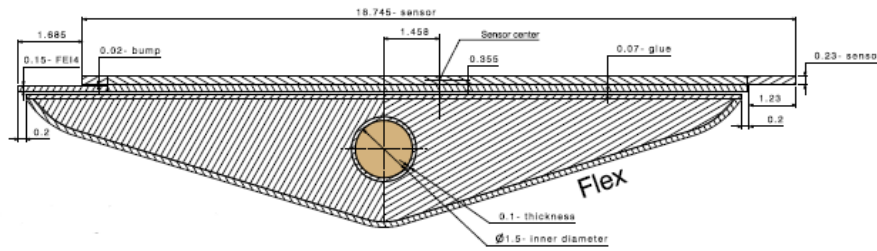
- An ADC for monitoring voltages, leakage currents, and temperatures.
- Shunt LDO (low dropout) regulators for analog and digital power, extended counters for level-1 id and beam-crossing id.
- The ability to truncate event size.

The production yield for the chips is slightly above 50 %.

For details on the FE-I4 readout chip see Lea Caminada's article in this volume ([8]).

### 4. On-Stave Assembly

The sensors are bump-bonded onto the frontend chips. The silicon modules are then glued onto flexible PCBs. The connection between flex and frontend chips is made via wirebonds. Since there are silicon modules that are one and two frontends wide there are also two types of module flexes. The module flex has an NTC soldered to it for temperature monitoring. The module flex has a test connector that allows for verification of the module before putting it on the stave. The connector is then cut off and the connection to the wings of the stave flex is made through wirebonds. The stave flex covers half a stave (16 frontend chips) and has eight connectors at the end (4 low voltage, 1 high voltage, 1 temperature readout, 1 data readout, 1 command and clock). The



**Figure 4:** Cross-section of an IBL stave [4].

flex cable runs along the back side of the stave and connects to the module flex through flexible wings. The low voltage traces on the flex are made of Aluminum for lower mass while the signal traces are made of copper.

Two adjacent readout chips share one clock and one command LVDS-line which means that commands have to be addressed to the chip. The address on the readout chips is set with wirebonds. The stave itself is made of a carbon fiber shell filled with thermal foam. It has a triangular profile with the long side facing the readout chips. A 1.5 mm inner diameter Titanium cooling pipe runs through it to provide evaporative CO<sub>2</sub> cooling to the frontends. The total amount of material in the stave amounts to less than 1.9 % X<sub>0</sub>. A cross-section of the assembled stave is shown in figure 4 [4].

The 14 staves of the IBL will be integrated around the beampipe on an integration teststand which will provide tooling to mount the staves mechanically and to route the services. In the end the complete 9-m long IBL object will be ready for insertion. There are two options for the insertion procedure:

1. **In situ:** Insertion of the 9 m long IBL object into the detector without access within the tracker volume. No removal of the Pixel Detector is needed but it is a very challenging task.
2. **On the surface:** Extract the Pixel Detector to the surface and insert the IBL. Reinsert the entire pixel package. This is easier since there is access outside  $z = \pm 1$  m. On the downside there is a risk to damage the Pixel Detector during extraction and reinsertion, and it requires extended work in a radiation environment.

In both cases the insertion of the inner support tube will be done on the surface which facilitates the IBL installation for both scenarios. There are additional considerations: If a project to install new service quarter panels for the Pixel Detector is approved then the Pixel Detector will be removed anyway in which case option 2 is favored even though option 1 is not excluded even in this scenario. Also the diamond beam monitor (DBM) prefers the area inside the Pixel Detector for installation which is only accessible with option 2. A decision on the installation option is expected to be taken in January of 2013.

## 5. Services

The eight connectors at the end of the stave connect to intermediate corrugated flexes. The corrugation is needed to compensate for the large expansion of about 7 mm of the wires with respect

to the carbon fiber support tube which is caused by the temperature differences during regular running ( $-30^{\circ}\text{C}$ ) and during bake-out of the beampipe ( $+60^{\circ}\text{C}$ ). The other end of the intermediate flexes has connectors which plug into a PC board. This so-called cable board has the wire bundle soldered to it. The wire bundle consists of two parts: A voltage supply bundle with wires for the low voltage, high voltage, and temperature sensing, and a readout bundle with twisted pair wires for clock and command to the frontends and data readout from the frontends. The power bundle is 3.7 m in length and ends in a custom connector just outside the endplate of the inner detector where it plugs into the cable coming from the regulator boards on the outside of the detector. The readout bundle is 5.2 m long and plugs into an optical converter box that is situated on the outside of the inner detector endplate. The placement of the optical components on the outside of the pixel volume makes it possible to access and service the optical boards more easily and also reduces the amount of radiation that they are exposed to. The readout twisted pair cables are a custom design with radiation hard cladding and a specified impedance that matches the rest of the transmission chain. The wire sizes are 28 AWG for the data readout and AWG 36 for clock and command. The electrical readout chain between the frontends and the optical converter consists of the module flex, the stave flex, the intermediate flex, the cable board, the 5.2 m long cable, and the connector board that plugs into the optoboard. This chain has been tested for data, clock, and command and works satisfactorily at the nominal data rates of 40 Mb/s for command, 160 Mb/s for data, and 40 MHz for the clock.

## 6. Cooling

The cooling for the IBL will be provided by an evaporative  $\text{CO}_2$  cooling plant. The cooling power of the plant needed for the IBL is 1.5 kW. The chiller will provide an operational range of  $-40^{\circ}\text{C}$  to  $+20^{\circ}\text{C}$ . A full prototype of the IBL plant is under construction. Several smaller prototypes (TRACI, Transportable Refrigeration Apparatus for  $\text{CO}_2$  Investigation) are already fully functional and are being used for the cooling of the prototype staves.

## 7. Prototype Stave

A first prototype IBL stave was assembled in the first half of 2012. It consists of 32 frontend chips of the prototype version FE-I4A. There are 8 3D single-chip sensors and 12 double-chip sensors like in production. The stave flex is a preproduction prototype. The stave is housed in a temperature controlled box. There is a  $\text{CO}_2$  TRACI cooling unit that is connected to the cooling pipe of the stave. Powering on this stave is done directly from the outside without on-chip regulators which is different from the production setup. The box is also equipped with scintillator panels for cosmic data taking with the stave. There is a linear motor setup that allows for a radioactive source to be moved along the stave.

This setup has been used to exercise the operation of the stave and to qualify the stave hardware before it goes into production. The frontends on the stave were tuned for threshold and signal time-over-threshold response. The results achieved by running calibrations on the stave are comparable to those run on single modules.

A second prototype stave with production-like modules called stave-0B was assembled in early



December 2012. It has production-like powering with shunt LDO regulators and FE-I4B readout chips. This stave is housed in the same box as stave-0A.

## 8. Schedule

The installation of the IBL will take place during the LS1 shutdown in 2013 - 2014. As of now all sensors and readout chips have been produced. Module assembly has started and should be completed by February 2013. Loading of the modules on staves has been exercised successfully with the two prototype staves. Stave production is scheduled to be done in May of 2013. The staves will be loaded onto the beampipe between March 2013 and July 2013. The fully assembled IBL will be installed in the ATLAS detector in early 2014.

## References

- [1] G. Aad et al., *ATLAS Pixel Detector Electronics and Sensors*, JINST 3 P07007 (2008)
- [2] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 S08003 229 (2008).
- [3] ATLAS IBL Collaboration, *ATLAS Insertable B-Layer Technical Design Report*, Technical Report CERN-LHCC-2010-013 (2010).
- [4] ATLAS Collaboration, *ATLAS Insertable B-Layer Technical Design Report Addendum*. Technical Report CERN-LHCC-2012-009. ATLAS-TDR-019-ADD-1, May 2012. Addendum to CERN-LHCC-2010-013, ATLAS-TDR-019.
- [5] S. Parker, C. Kenney, S. Segal, and C. Storment, *Silicon detectors with 3-D electrode arrays: fabrication and initial test results*, IEEE Tr. Nucl. Sci **46** (1999) 1224-1236.
- [6] G.-F. dalla Betta, *3D Irradiation Results*, these proceedings.
- [7] ATLAS IBL Collaboration, *Prototype ATLAS IBL modules using the FE-I4A front-end readout chip*, JINST 7 (2012) P11010, 2012.
- [8] L. Caminada, *ATLAS FE-I4 ASIC*, these proceedings.