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Development of beam-collision feedback systems for future lepton colliders

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Future lepton colliders such as the International Linear Collider (ILC), and the Compact Linear Collider (CLIC) require nanometer-sized beams at the interaction point (IP). We report on the design, protoyping and testing of beam-based feedback systems for steering the beams into collision at the IP so as to maximise the luminosity performance of the colliders. Both all-analogue and digital feedback prototypes have been built and tested for CLIC and ILC, respectively. The latency of such systems needs to be very low so as to match the bunch spacing and bunch-train length. We report on the achievement of systems with 130ns and 23ns latency that meet the beam position resolution and beam kick requirements of both ILC and CLIC, respectively; the prototypes were tested with ILC- and CLIC-like beams at the Accelerator Test Facility at KEK. We have simulated the measured performance and demonstrated the potential of the feedbacks to compensate for ground-motion disruption and recover almost all of the design luminosity.

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1. Introduction

Currently two future high-energy electron-positron linear collider projects are under study: the International Linear Collider (ILC) [1] and the Compact Linear Collider (CLIC) [2]. Some key beam parameters for these two projects are summarised in Table 1. Achievement of their design luminosities will require unprecedentedly-small transverse beam sizes, at the nanometer level (Table 1), and a correspondingly high degree of spatial overlap of the beams at the interaction point (IP). The luminosity vs. relative beam-beam offset at the IP is shown in Figure 1 [3]; significant luminosity loss will occur unless the beams are maintained in collision overlap to within roughly one unit of the vertical beam size. For example, in order to maintain the luminosity to within 10% of its nominal value, the electron and positron vertical beam overlap needs to be stabilised to within ~$1\sigma_y$ for CLIC and ~$0.5\sigma_y$ for ILC. A number of technical systems will be required in order to achieve such a degree of collision stability; see [3] for a brief description. Here we discuss only fast beam-based collision feedbacks.

Property	ILC 0.5 TeV	CLIC 0.5 TeV	CLIC 3 TeV	units
Particles/bunch (N_e)	2.0	0.68	0.37	10^{10}
Bunches/train (N_{train})	2625	354	312	
Train Repetition Rate (f_{rep})	5	50	50	Hz
Bunch Separation	369.2	0.5	0.5	ns
Train Length	969.15	0.177	0.156	μs
Horizontal IP emittance (ε_x^*)	1000	2400	660	nm·rad
Vertical IP emittance (ε_y^*)	40	25	20	nm·rad
Horizontal IP Beam Size (σ_x^*)	639	202	45	nm
Vertical IP Beam Size (σ_y^*)	5.7	2.3	0.9	nm
Bunch length (σ_z^*)	300	44	44	μm
Total luminosity (L)	2.03	2.24	6.0	$10^{34}cm^{-2}s^{-1}$

Table 1: Some nominal design beam parameters for the ILC and CLIC.

2.Beam-based feedbacks for future linear colliders

A number of fast beam-based feedback systems are required at future electron-positron colliders. At the IP a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for any residual ground-motion-induced relative jitter on the final quadrupole magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5-100 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Beam Delivery System.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a normalised position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-

train feedback is shown in Figure 2, for the case in which the electron and positron beams cross with a small angle. The deflection of one outgoing beam caused by the relative offset of the two incoming beams is registered in a BPM and a compensating angular deflection is applied via a kicker to the incoming other beam so as to restore beam overlap at the IP. The design implementation of this concept is illustrated, for CLIC as an example, in Figure 3.

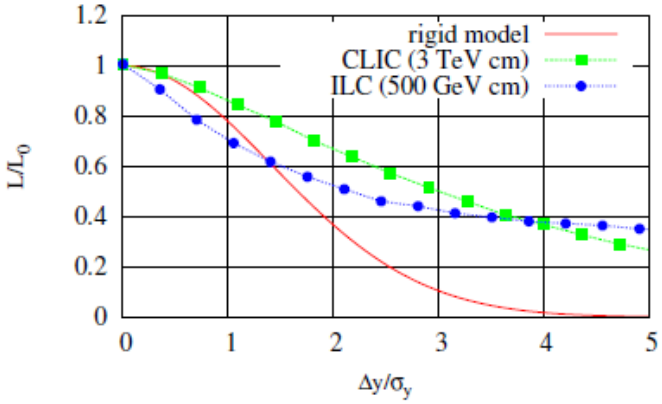

Figure 1: Luminosity relative to design vs. relative vertical beam-beam position offset at the IP.

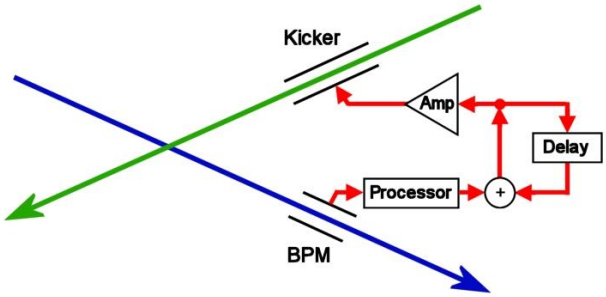

Figure 2: Schematic of IP intra-train feedback system for an IP with a non-zero beam crossing angle.

The bunchtrain time structure (Table 1) is a determining factor for the choice of IP feedback system technology as it sets the scale of the latency required for performing intra-train beam correction. The ILC design [1] calls for trains of approximately 3000 bunches, with an inter-bunch time separation of about 300ns. This allows for a digital feedback processor and the capability of bunch-by-bunch correction. The CLIC design [2] calls for trains of approximately 300 bunches, with an inter-bunch time separation of about 0.5ns. This requires an exceptionally fast, high-bandwidth, all-analogue feedback system in order to allow any correction at all within the 156ns bunchtrain duration.

3.All-analogue-based feedback systems (CLIC)

We have developed all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds. We achieved total latencies (signal propagation

delay + electronics latency) of 67ns (FONT1) [4], 54ns (FONT2) [5] and 23ns (FONT3) [6]. In the last case, the electronics latency was measured to be c. 13ns. Adding this to the signal propagation delay for feedback hardware distributed as in the CLIC design (Figure 3) yields a total expected latency of 37ns. The performance of such a CLIC IP feedback system has been simulated [3]. Figure 4 shows, for illustration, the simulated luminosity for one bunchtrain crossing. The initially low luminosity caused by the incoming beams' relative vertical offset caused by ground-motion effects is compensated by the action of the feedback in steering the beams into collision overlap within the duration of the bunchtrain. The CLIC system has been documented in the CLIC Conceptual Design Report [7].

4. Digital-based feedback systems (ILC)

We report the latest results on the design, development and beam testing of an ILC prototype system ('FONT5') that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) [8,9,10]. The use of a digital processor allows for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations.

A schematic of the FONT5 feedback system prototype and the experimental configuration in the upgraded Accelerator Test Facility (ATF) extraction beamline, ATF2, is shown in Figure 5. The ATF can be operated to provide an extracted train that comprises up to 3 bunches separated by an interval that is selectable in the range 140 - 300 ns. This provides a short ILC-like train which can be used for controlled feedback system tests. FONT5 has been designed as a bunch-by-bunch feedback with a latency goal of around 140ns, meeting the minimum ILC specification of c. 150ns bunch spacing. This allows measurement of the first bunch position and correction of both the second and third ATF bunches.

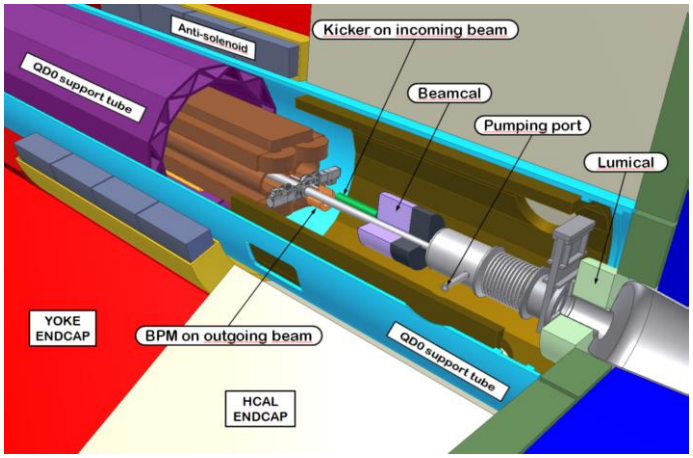

Figure 3: Layout of IP intra-train feedback system components in the CLIC interaction region [7].

Two stripline BPMs (P2, P3) are used to provide vertical beam position inputs to the feedback. Two stripline kickers (K1, K2) are used to provide fast vertical beam corrections. A third stripline BPM (P1) is used to witness the incoming beam conditions. Upstream dipole corrector magnets (not shown) can be used to steer the beam so as to introduce a controllable

vertical position offset in the BPMs. Each BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board. Analogue output correction signals are sent to a fast amplifier that drives each kicker.

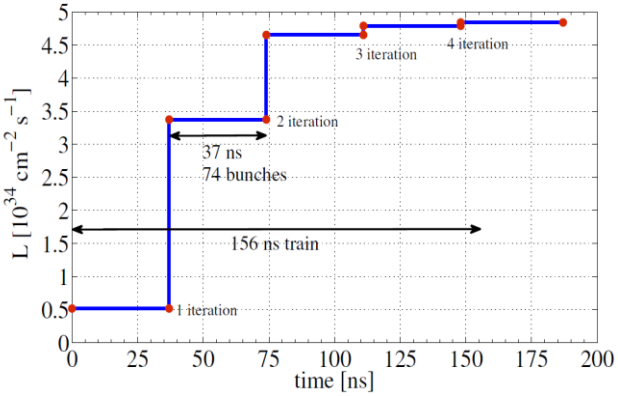

Figure 4: Luminosity vs. time for a simulated bunchtrain crossing at CLIC.

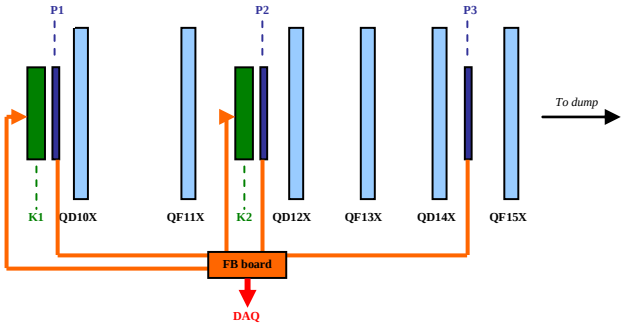

Figure 5: Schematic of FONT5 at the ATF2 extraction beamline showing the relative locations of the kickers, BPMs and the elements of the feedback system.

The design of the front-end BPM signal processor is described in [11]. The top and bottom (y) stripline BPM signals were added with a resistive coupler and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have very low latencies so as to yield a total processor latency of 10ns.

The custom digital feedback processor board is shown in Figure 6. There are 9 analogue signal input channels in which digitisation is performed using ADCs with a maximum conversion rate of 400 MS/s, and 2 analogue output channels formed using DACs, which can be clocked at up to 210 MHz. The digital signal processing is based on a Xilinx Virtex5 FPGA. The FPGA is clocked with a 357 MHz source derived from the ATF master oscillator and hence locked to the beam. The ADCs are clocked at 357 MHz. The analogue BPM processor output signals are sampled on peak to provide the input signals to the feedback. The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the sum signal for beam charge normalisation. The delay loop is implemented as an accumulator in the FPGA. The output is converted back to analogue and used as input to the driver amplifier. A

pre-beam trigger signal is used to enable the amplifier drive output from the digital board. The driver amplifier was manufactured by TMD Technologies and provides ±30A of drive current into the kicker. The risetime is 35ns from the time of the input signal to reach 90% of peak output. Beam test results are described in [8,9,10]. The feedback system meets the ILC requirements on latency, kick strength and dynamic range. It is documented in [12].

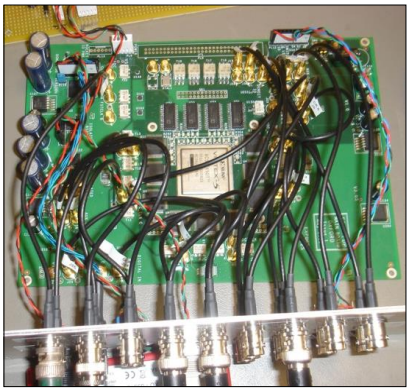

Figure 6: FONT5 digital feedback board.

5. Conclusions

Prototype fast intra-train beam-based feedback systems for luminosity optimisation at future lepton colliders have been designed, prototyped, and tested with beam. They meet the design requirements for IP collision feedbacks at both ILC and CLIC.

References

[1] ILC: http://www.linearcollider.org/
[2] CLIC: http://clic-study.org/
[3] J. Resta Lopez, P.N. Burrows, G.B. Christian, *Luminosity performance studies of the compact linear collider with intra-train feedback system at the interaction point*, JINST 5:P09007 (2010).
[4] P.N. Burrows et al, *Feedback On Nanosecond Timescales (FONT): results from first beam tests at the NLCTA at SLAC*, Proceedings PAC03, Portland, Oregon, May 2003, p. 687.
[5] P.N. Burrows et al, *Nanosecond-timescale intra-bunch-train feedback for the linear collider: results of the FONT2 run*, Proceedings EPAC04, Lucerne, July 2004, p. 785.
[6] P.N. Burrows et al, *Tests of the FONT3 linear collider intra-train beam feedback system at the ATF*, Proceedings PAC05, Knoxville, TN, May 2005, p. 1359.
[7] *A Multi-TeV Linear Collider based on CLIC Technology: CLIC CDR, CERN-2012-007, p. 552.*
[8] R. Apsimon et al, *Latest beam test results from ATF2 with the FONT ILC prototype intra-train beam feedback systems*, Proc. the International Particle Accelerator Conference, Kyoto, May 2010
[9] G.B. Christian et al, *Latest performance results from the FONT5 intra-train position and angle feedback system at ATF2*, Proc. International Particle Accelerator Conference, San Sebastian, 2011.
[10] D.R. Bett et al, *Latest performance results from the FONT5 intra-train beam position and angle feedback system at ATF'*, Proc. International Particle Accelerator Conference, New Orleans, 2012.
[11] P.N. Burrows et al, *A low-latency sub-micron resolution stripline beam position monitoring system for single-pass beamlines*, Proc. Int. Particle Accelerator Conference, New Orleans, 2012.
[12] *International Linear Collider Technical Design Report, Part 2: Baseline Design*, p. 186.

