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Radiation-hard active pixel detectors based on HV-CMOS technology for HL-LHC upgrades

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New active pixel detectors, based on the high-voltage CMOS technology, have been recently introduced into the HEP community. The design principle relies in the pixel electronics being integrated inside the silicon substrate itself. Applied to particle tracking detectors, major advantages of the HV-CMOS technology with respect to standard silicon detectors are very low material budget, fast charge collection time, high-radiation tolerance, operation at room temperature and low cost.

Within the R&D for the future ATLAS tracker upgrade for the High-Luminosity LHC program, the HV2FEI4 is a HV-CMOS prototype chip developed in 180 nm AMS technology H18. It has been designed to be compatible with both a pixel and a strip readout ASIC. In this paper, first experience in operating the HV2FEI4 chip is reviewed. Preliminary results after neutron irradiation up to $10^{16}\,n_{eq}/cm^2$ and after X-ray irradiation up to 100 Mrad are shown.

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1. Introduction

A major luminosity upgrade for the Large Hadron Collider (LHC) is planned for ~ 2024. During the so-called High-Luminosity LHC (HL-LHC), the instantenous luminosity will be raised up to $\sim 5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ with the aim of collecting a total integrated luminosity of $\sim 3000\,\mathrm{fb}^{-1}$ for the two general-purpose LHC experiments, ATLAS [1] and CMS [2], after ten years of operation. For ATLAS, an upgrade scenario will imply the complete replacement of its present internal tracker. At the luminosities expected in the HL-LHC, the number of proton-proton interactions per bunch-crossing will reach $\sim$140 (assuming a bunch-spacing configuration of 25 ns), and the tracking detectors will need to withstand a very high cumulated radiation damage, with fluences beyond $\sim 10^{16}\,\mathrm{n_{eq}}/\mathrm{cm}^2$ (1 MeV neutron equivalent per square centimetre) [3] for the smallest radii close to the beam-pipe. Key requirements for the new tracker are therefore radiation hardness, low detector occupancy and excellent tracking performance in a high pile-up environment. The current baseline layout is an all-silicon system, with pixel detectors in the innermost layers and silicon micro-strip detectors at intermediate and outer radii. For the pixel detector, a hybrid integration approach is assumed, in which a silicon pixel sensor is bump-bonded to a readout chip (DC-coupling). Pixel sizes of $25 \times 150\,\mu\mathrm{m}^2$ ($50 \times 250\,\mu\mathrm{m}^2$) are targeted for the innermost (outermost) layers, with a typical sensor thickness of $\sim 150\,\mu\mathrm{m}$ [3].

A new detector concept based on the high-voltage CMOS (HV-CMOS) technology has been recently proposed [4]. HV-CMOS is a well established commercial technology widely used in different industrial application systems (*e.g.* flat panel displays, motor drivers in automotive industry) that require higher voltages ($\geq 50\,\mathrm{V}$) than the standard supply voltages of current CMOS technologies (typically few volts). By integrating on a thin silicon substrate with moderate resistivity the pixel electronics (*e.g.* charge sensitive amplifier, comparator, etc.), a particle detector with almost complete fill-factor can be achieved. Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping.

2. Principle of a High-Voltage CMOS pixel detector

The operating principle of the HV-CMOS pixel detector is depicted in Fig. 1. A *p*-type silicon substrate contains a deep *n*-well that acts as the signal collecting electrode. The deep *n*-well contains the entire pixel electronics, both PMOS (implemented directly inside the *n*-well) and NMOS transistors (placed inside a *p*-well that itself is embedded inside the *n*-well). By applying a reverse bias voltage to the *n*-well with respect to the substrate, a depletion area is created. After the passage of a charged particle through the bulk, the charge carriers created by ionization in the depleted region drift along the electric field lines towards the electrode. As all transistors are physically isolated from the substrate (as implemented in the deep *n*-well), a relatively high bias voltage ($\sim 100\,\mathrm{V}$) can be applied to enlarge the depletion zone (typically $\sim 15\,\mu\mathrm{m}$-deep).

Several HV-CMOS prototype sensors have already been produced in 350 and 180 nm Austria Microsystems [5] (AMS) technology. Testbeam results on a monolithic pixel detector (with simplified electronics), with 21 µm implemented in 350 nm AMS technology, indicate a spatial resolution of almost 3 μm [6]. Another HV-CMOS prototype with $50 \times 50\,\mu\mathrm{m}^2$ pixel-size was irradiated with 23 MeV protons up to $10^{15}\,\mathrm{n_{eq}}/\mathrm{cm}^2$ (this is roughly the fluence expected for the first strip layer of

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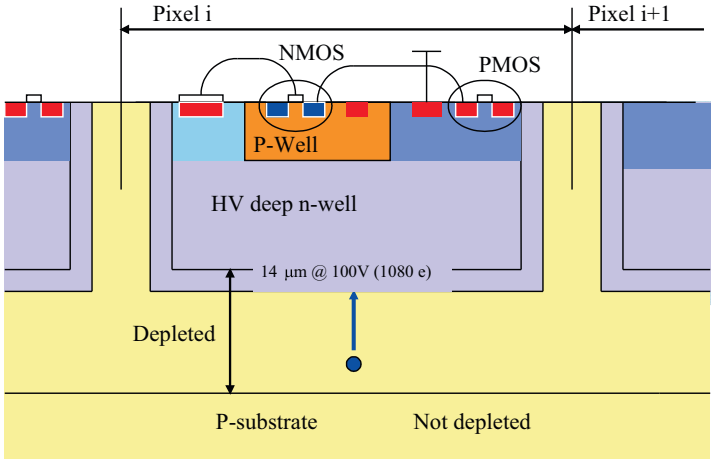


Figure 1: Principle of the high-voltage CMOS pixel detector.

the future ATLAS tracker), corresponding to a dose of ∼300 Mrad in SiO_2. The signal to noise ratio, as measured with a high-energy β-source, was found to be larger than 40 at 10 °C [7].

3. The HV2FEI4 prototype chip

The HV2FEI4 chip [6] is an active pixel detector prototype produced in 180 nm AMS H18 technology and developed for the R&D program of the future ATLAS tracker upgrade. The unit cell structure (see Fig. 2) contains six pixels arranged in three columns and two rows, each pixel being $125 \times 33\,\mu m^2$. The entire detector matrix consists of 20×12 unit cells, or 1440 individual pixels. Each pixel implements a CMOS charge-sensitive amplifier, a comparator (including local threshold adjustment) and an output stage.

The HV2FEI4 has been designed to be compatible with either a pixel or a strip readout chip. In the case of the hybrid-pixel readout, the six pixels in a unit cell are connected three by three in a triangular configuration. With the output buffers of the pixels being biased with different voltages, every pixel in a group will generate a unique signal amplitude. By interpreting the pulse-height, the spatial resolution is increased without changes to the pixel readout chip. In the case of the strip-like readout, the pixels are connected to form so-called "virtual" strips. An internal resistor network generates voltage drops along the strip-line, so that the resulting pulse-height contains information about the hit-position along the virtual strip-length. This would allow a large improvement of the spatial resolution in the Z-coordinate (along the beam-axis) in the strip-region.

3.1 Hybrid-pixel readout

The pixel readout has been tested with the ATLAS FEI4 chip [8], a $18.8 \times 20.2\,mm^2$ ASIC developed for the pixel modules of the ATLAS Insertable B-Layer [9] and future outer layer upgrades. As the pixel size of the FEI4 is $250 \times 50\,\mu m^2$, the HV2FEI4 unit-cell corresponds to two FEI4 pixels (see "so" and "st" pads in Fig. 2). In this case, instead of using the standard bump-bonding technique, the HV-CMOS sensor was glued to the readout ASIC (see Fig. 3a), so that the signal transmission is done capacitively (AC-coupling). Fig. 3b shows a photograph of the setup. The

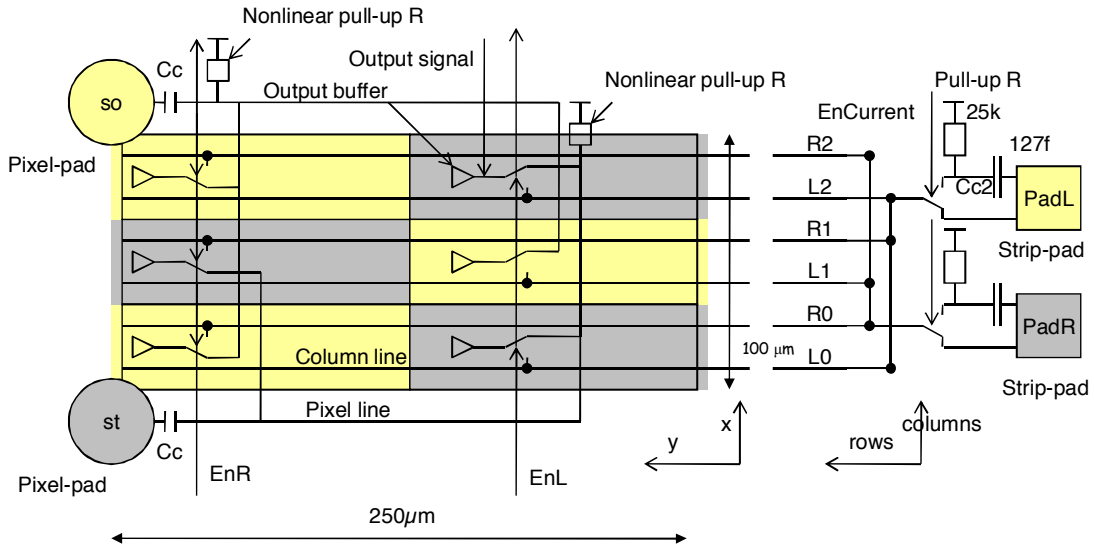


Figure 2: Unit cell structure of the HV2FEI4 pixel HV-CMOS pixel sensor prototype. The unit cell contains six pixels arranged in three columns and two rows. The size of each individual pixel is $125 \times 33\,\mu m^2$. The area of the unit cell is $250 \times 100\,\mu m^2$, corresponding to two pixels of the FE-I4 [8] front-end readout chip. The "so" and "st" pads are used with a pixel readout ASIC; the "padL" and "padR" pads are used with a strip readout ASIC.

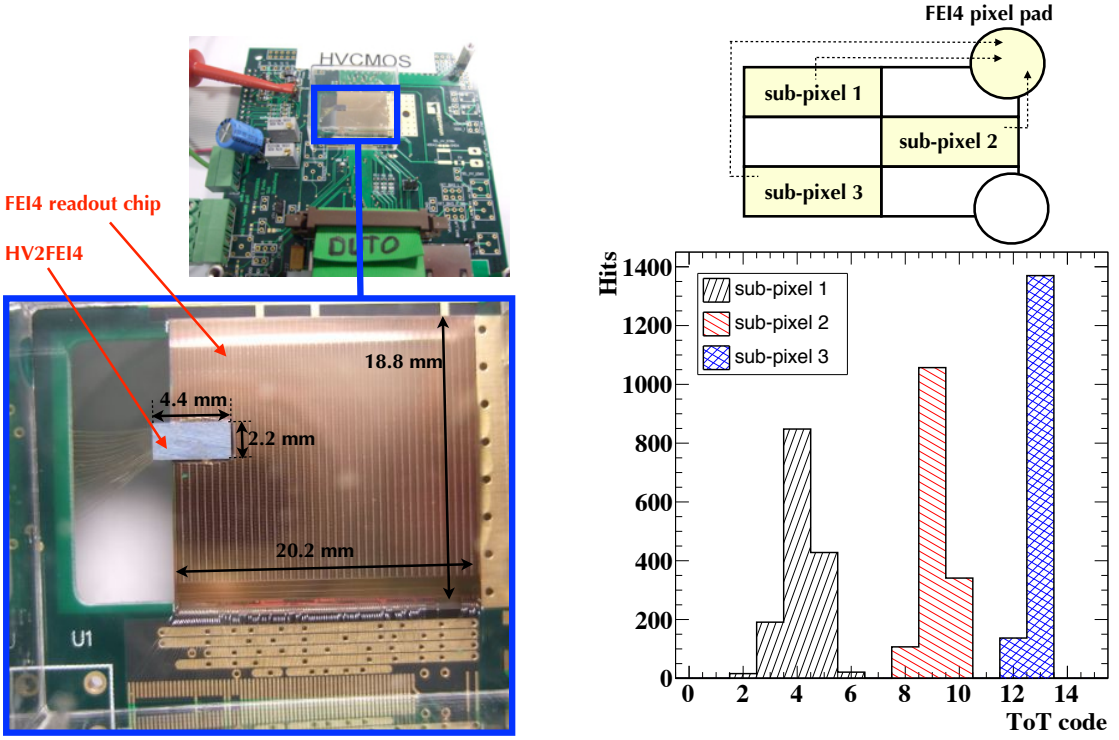
analog front-end of the FEI4 ASIC implements for each pixel an amplifier and a discrminator with adjustable threshold. The collected charge amplitude is then digitised into Time-Over-Threshold (ToT). The hit pixel address, a hit time stamp and the ToT information are then sent to output buffers. Fig. 3b shows the ToT distribution for a specific FEI4 pixel coupled to the HV2FEI4. The three different sub-pixels of the unit-cell connected to the same pixel pad can be clearly differentiated.

3.2 Strip-like readout

For the strip readout, work is currently ongoing with a setup using the analog Beetle chip (developed for the LHCb VELO tracking detector) as readout ASIC. Fig. 4 shows a first proof-of-principle of the pixel encoding along a virtual strip of the HV2FEI4 chip. Depending on the row number (*i.e* position along the strip), the pixel pulse amplitude varies according to the resistor network implemented in the strip bias-line.

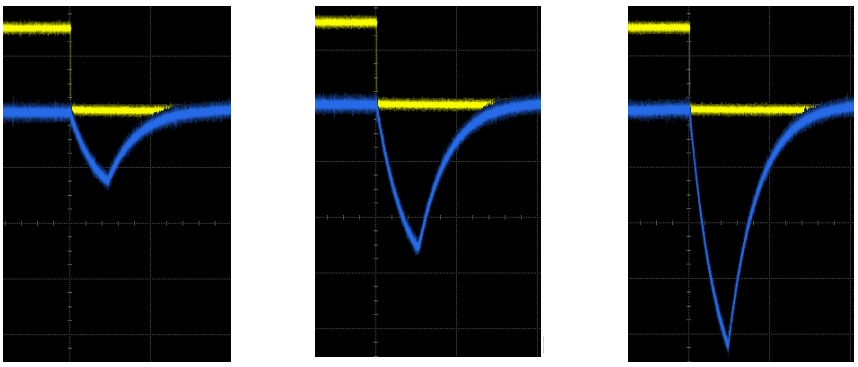
4. Irradiation

Several HV2FEI4 first-version prototypes (HV2FEI4v1) have been irradiated with different particles (protons, neutrons, X-rays) and fluences. Fig. 5 shows the IV characteristics as measured at room temperature after neutron irradiation at $10^{15}\,n_{eq}/cm^2$ and $10^{16}\,n_{eq}/cm^2$ fluences. Despite the fact HV2FEI4v1 is known to be not fully radition-hard (as due to the usage of standard cells in the pixel matrix) the results show good performance with respect to bulk damage, with a current increase factor of ~ 10 between the two fluences.



(a) (b)

Figure 3: (a) Hybrid-pixel readout of the HV-CMOS chip. The enlarged photograph shows the $2.2 \times 4.4\,\mathrm{mm}^2$ HV2FEI4 chip glued to a $18.8 \times 20.2\,\mathrm{mm}^2$ FEI4 readout ASIC. (b) Distribution of Time-Over-Threshold (ToT) for a single FEI4 pixel. The top-schema illustrates, within a single unit-cell of the HV2FEI4 chip, the connection of the three (colored) sub-pixels to the corresponding pixel pad.



(a) row 0 (b) row 12 (c) row 23

Figure 4: Pixel encoding along a virtual strip of the HV2FEI4 chip operated in a strip-like readout mode. The different oscilloscope screenshots show the analog (negative) pulse at the discriminator output of different pixels along a virtual strip (12 unit-cells or 24 pixel rows).

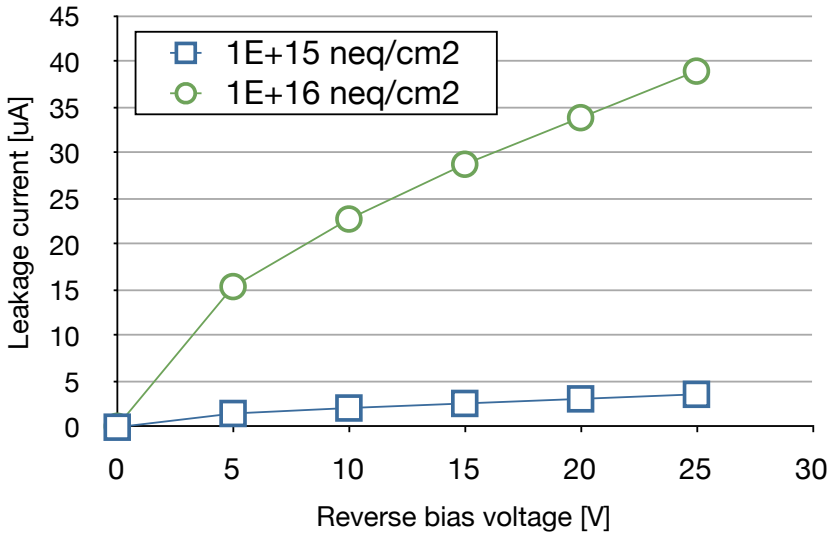


Figure 5: IV characteristics after neutron irradiation up to $10^{15}\,n_{eq}/cm^2$ and $10^{16}\,n_{eq}/cm^2$. Measurements are at room temperature.

A second version of the chip (HV2FEI4v2) was recently produced, with some design modifications for an improved radiation tolerance. The HV2FEI4v2 contains three different pixel types to study how effective a particular implementation is with respect to radiation damage (*e.g.*, among other features, the so-called "rad-hard" pixels implement circular transistors and guard rings). Fig. 6 shows the pulse amplitude at the preamplifier output for different pixel types as a function of dose for an X-ray irradiated HV2FEI4v2 chip[1]. Pulses of 1 V amplitude were externally injected into the pixel matrix. Results show no significant degradation of the chip response after 50 Mrad, with a decrease of the on-chip preamplifier output response after 100 Mrad. Indeed after a period of four-days annealing, the original chip performance is almost fully restored.

5. Summary

A new concept of particle detector based on the high-voltage CMOS (HV-CMOS) technology has been presented. The HV-CMOS chips offer several advantages with respect to standard silicon detectors: very low material budget, fast charge collection time, high-radiation tolerance, operation at room temperature and low cost. The HV2FEI4 is a prototype chip produced in 180 nm AMS technology for the R&D program of the future ATLAS tracker upgrade. The chip has been designed to be compatible with both a pixel and a strip readout ASIC. The signal transmission to an FEI4 readout ASIC through capacitive coupling has been shown to work well, achieving the identification of individual sub-pixels within a single unit-cell based in the ToT distribution of the FEI4. The proof-of-principle of pixel encoding in a virtual strip has been also validated. The HV2FEI4 chip is found to be operative at room temperature even after neutron irradiation up to a fluence of $10^{16}\,n_{eq}/cm^2$ and after X-ray irradiation up to a dose of 100 Mrad. Next steps in this

[1] results are shown up to 100 Mrad although the chip has been recently irradiated up to 860 Mrad.

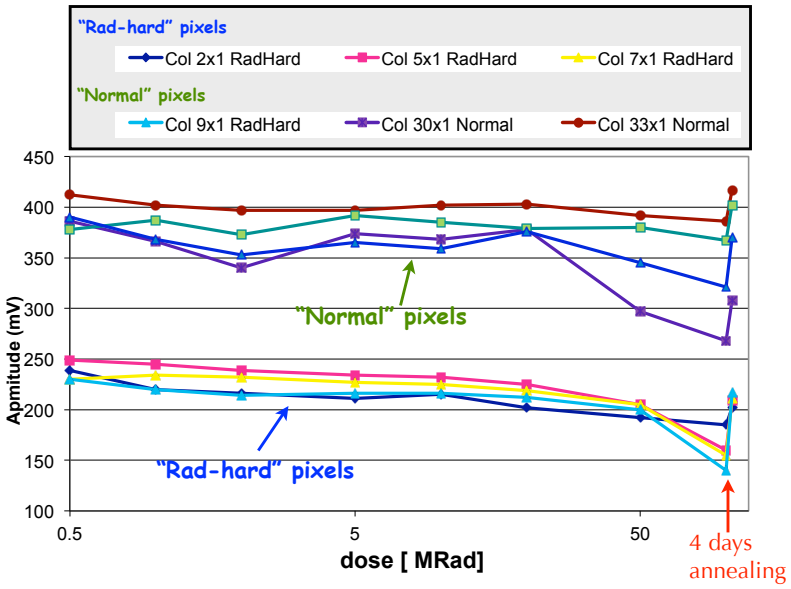


Figure 6: Pulse amplitude at the preamplifier output for 1 V injected-pulse after X-ray irradiation up to 100 Mrad of a HV2FEI4v2 prototype chip. Two different group of pixels (so-called "normal" and "rad-hard") are compared. The intrinsic lower amplitude of the "rad-hard" pixels is just due to the larger parasitic capacitance of their circular transistors if compared with the "normal" pixel transistors.

R&D program include further irradiation studies and the evaluation of the hit-detection efficiency in a testbeam environment.

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