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Upgrade of the CMS Tracker

Katja KLEIN[*†]
1. Physikalisches Institut B, RWTH Aachen University
E-mail: Katja.Klein@cern.ch

The performance of the Tracker of the CMS experiment, comprising of a pixel and a strip detector, has so far been excellent, as reflected in the wealth of beautiful physics results from CMS. However, the foreseen increases of both the instantaneous and the integrated luminosity by the LHC during the next ten years will necessitate a stepwise upgrade of the CMS tracking detector.
In the extended end-of-year shutdown 2016/17 the pixel detector will be exchanged. The new device is designed for an instantaneous luminosity of $2 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an integrated luminosity of $500\,\mathrm{fb}^{-1}$. The number of layers will be increased from three to four in the barrel part and from two to three in the end caps, thus providing four-hit coverage over the full pseudorapidity range. A smaller beampipe allows the reduction of the radius of the innermost layer, improving the tracking performance. Further improvements include a new readout chip, reduction of material, and the installation of more efficient cooling and powering systems.
Around 2022, in Long Shutdown 3, the whole tracker will need to be replaced, in order to be able to cope with an instantaneous luminosity of $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an integrated luminosity of $3000\,\mathrm{fb}^{-1}$, as expected for the High Luminosity LHC (HL-LHC). A new challenge is the requirement that tracker information should be usable in the Level 1 trigger decision. This has led to a dedicated module design with two closely spaced sensor layers whose hits are correlated in the module electronics. In this way an estimate on the transverse momentum can be made and high momentum tracks can be selected, significantly reducing the data volume to be processed.
This paper will motivate the design choices for the CMS pixel and outer tracker upgrades. The status and plans of these projects will be summarized and highlights of the R&D will be described.

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[*]Speaker.
[†]on behalf of the CMS Collaboration

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1. Introduction

The Large Hadron Collider (LHC) at CERN, Geneva, is the world's largest and most powerful proton and heavy ion collider. During Run 1, which ended in 2012, the LHC delivered about $30\,\text{fb}^{-1}$ of proton-proton collisions at center-of-mass energies of $\sqrt{s} = 7-8\,\text{TeV}$ and at a peak instantaneous luminosity of up to $7.7 \cdot 10^{33}\,\text{cm}^{-2}\text{s}^{-1}$.

Within the next ten years a series of upgrades to the LHC are planned, to improve further its performance. During the currently ongoing Long Shutdown 1 (LS1), work is taking place to allow the design center-of-mass energy of 14 TeV to be achieved. Data taking will resume in 2015 and last until Long Shutdown 2 (LS2) in 2018. For this Run II a peak luminosity of $1.7 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ is expected. A number of improvements, in particular to the injector chain, during LS2 will allow the peak luminosity to be increased to about $2.0 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$. Run III will last until Long Shutdown 3 (LS3), which is currently planned for 2022/2023. During LS3 the LHC itself will be turned into the High Luminosity LHC (HL-LHC), with a peak luminosity of $5 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$.

About $300\,\text{fb}^{-1}$ of data are expected to be delivered in total during Runs II & III, while about $3000\,\text{fb}^{-1}$ of data will be taken after LS3.

Various upgrades are also planned for the CMS experiment [1], and particularly for its tracking detectors. During LS1 consolidation of the tracker cooling and dry air systems is taking place, to enable operation of the tracker at nominal temperatures. During the extended winter technical stop 2016/2017 a new pixel detector will be installed [2]. This is referred to as the "Phase-1 Pixel Upgrade". No tracker upgrades are foreseen for LS2, but a replacement of the innermost layer of the pixel detector might be required after $250\,\text{fb}^{-1}$. In LS3, both a new pixel detector and outer tracker, including a track trigger, will be installed [3]. This is referred to as the "Phase-2 Upgrade" of the CMS tracker.

In this paper, the Phase-1 Pixel Upgrade and the Phase-2 Upgrade of the outer tracker will be covered.

2. The Phase-1 Pixel Upgrade

The present pixel detector comprises three cylindrical layers in the barrel part (BPIX) and two disks per side (FPIX) (Fig. 1, left). The barrel layers have radii of 4.4, 7.3, and 10.2 cm, while the disks are installed at distances of ± 34.5 and ± 46.5 cm from the nominal interaction point along the beam direction (z). The pixel cell size is 100 x 150 μm^2. The 66 million pixels add up to a silicon area of about $1\,\text{m}^2$. In 2012, the fraction of working channels was 97 %.

The present CMS pixel detector was designed for nominal LHC luminosity, $1.0 \cdot 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$, with a bunch spacing of 25 ns. For twice the luminosity, 50 (100) pile-up events are expected for a bunch spacing of 25 (50) ns, and hit rates could reach $600\,\text{MHz/cm}^2$. Under such conditions, severe data losses in the pixel front-end of, in the worst case, up to 50 % are expected. Therefore the pixel detector will be replaced already in the winter shutdown 2016/17, requiring careful minimization of the impact on data taking. The solution is an evolutionary upgrade, with main improvements as follows:

- Four-hit coverage up to a pseudorapidity $|\eta| = 2.5$, where $\eta = -\ln(\tan(\theta/2))$, with the polar angle θ, will increase the robustness in the tracking. The number of barrel layers is

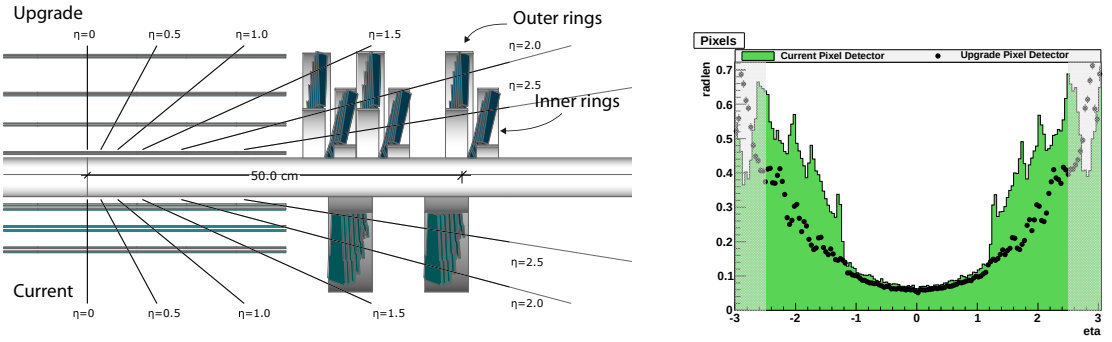

Figure 1: Left: Layout of the present (bottom) and upgraded (top) pixel detector, in $r-z$ view. Right: Material budget in fraction of radiation lengths as a function of pseudorapidity for the present (green histogram) and upgraded (dots) pixel detector. The grey areas are outside of the sensitive tracker volume.

increased to four and the number of disks is increased to three per side. This improves the tracking efficiency in a simulated $t\bar{t}$ sample with 50 pile-up events by 10-20 % depending on pseudorapidity, while the fake rate is decreased by almost 20 % at high η [2].

- The innermost barrel layer will be installed at a smaller radius of 2.9 cm. This will improve vertex resolution and b-tagging efficiency. For a light quark mistag rate of 1 % and a pile-up of 50, the b-tagging efficiency increases by about 15 % [2].
- A new, improved readout chip will recover the hit efficiency.
- The amount of passive material will be decreased by using ultra-light mechanical support structures, by relocating electrical patch panels to outside of the sensitive volume, and by switching to an evaporative CO_2 cooling system. These changes result in a significant decrease of material for $|\eta| > 1$, as is visible from Fig. 1, right. The mass of BPIX will be reduced from 16.8 kg to 6.7 kg.
- A novel powering scheme based on DC-DC conversion will allow a factor of 1.9 more channels to be powered.

The new layout can be seen in Fig. 1: the barrel layers are at radii of 2.9, 6.8, 10.2, and 16.0 cm, and the disks at positions of $\pm$29.1, $\pm$39.6, and $\pm$51.6 cm from the interaction point.

2.1 Pixel Modules and Readout Chip

The upgrade pixel detector comprises 1 846 pixel modules with a total of 124 million channels. In both FPIX and BPIX the modules are of rectangular shape, whilst previously several types of wedge shaped modules were used in FPIX. The restriction to one basic module type simplifies module production for FPIX considerably.

An exploded view of the barrel modules is shown in Fig. 2, left. As in the present pixel detector, n^+-in-n silicon sensors with a thickness of 285 μm are used. The active area amounts to 16.2 x 64.8 mm^2 and the pixel cell size is again 100 x 150 μm^2. Each sensor comprises 66 560

pixels. The sensor is bump-bonded to 2 x 8 readout chips (ROCs), which will be thinned down to 75 μm and 180 μm for layer 1 and layers 2-4, respectively. A low mass PCB, the High Density Interconnect or HDI, is glued on top of the sensor, and wirebonded to the ROCs. It distributes the voltages to the sensor and the ROCs, and signals to and from the ROCs. The HDI contains three 2 μm thin copper layers, and carries a data manager chip, the Token Bit Manager or TBM. The power and data cable consists of 20 copper-clad aluminium wires of 125 μm and 360 μm diameter for data transmission and power, respectively. Mechanical support for mounting is provided by two 250 μm thick base-strips made from silicon-nitride (Si_3N_4) for BPIX modules of layers 2-4, while the modules for the innermost layer, where no room for the base strips is available, have a carbon fiber clip attached at one short end only.

FPIX modules differ in the layout of the HDI, the module cable (which is a flexible Kapton cable), and the support, which is realized by a single module end holder made of PEEK.

The modules will be built by regional consortia. Currently qualification of the production centers is ongoing, including the commissioning of in-house bump-bonding. Module mass production will start in 2014.

The new "PSI46dig" ROC is again made in 250 nm CMOS technology and is heavily based on the present chip, the PSI46 ROC. Both chips feature a column drain architecture. To reduce data losses, the depths of data and time stamp buffers have been increased. Simulations indicate that data losses in the first layer will decrease from 16.0 % (50 %) to 2.4 % (4.8 %) for a bunch spacing of 25 ns (50 ns) at $2.0 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Reduction of internal cross-talk and a faster comparator result in a lower threshold. Test beams show that stable and low noise operation is possible with a threshold of 1300 electrons, a significant improvement with respect to the present value of 2800 electrons. The readout protocol was changed from analog-coded to digital and the ROC readout speed was increased from 40 MHz to 160 Mbit/s.

The second version PSI46digV2 is currently under test. One more iteration is foreseen to fix remaining minor issues.

A dedicated chip version, employing a Column Drain Cluster algorithm, with clusters of 4 x 4 pixels being transferred to the chip periphery in parallel, is foreseen for the innermost layer. This chip will be submitted end of 2013.

2.2 DC-DC Conversion Powering

The increase of readout channels by a factor of 1.9 implies an increase of power losses on the supply cables by a factor of almost 4. Since the present cables and power supplies are to be reused, a powering scheme based on the DC-DC conversion technique will be implemented [2], where the power is supplied at a higher voltage and lower current. DC-DC converters will be installed on the service structures, at $|\eta| \approx 4$ and of the order of 1 m away from the pixel modules. With an input voltage of 10 V and output voltages of either 3.0 V or 2.4 V, for the digital and analog part of the module electronics, respectively, losses are reduced by a factor of about ten. One DC-DC converter pair powers between one and four pixel modules. The buck topology has been chosen for the DC-DC converters. The board has a footprint of 16 x 28 mm^2 and carries an ASIC [4] which includes the power transistors, drivers and logic; a shielded air-core inductor; and filter networks (Fig. 2, top right). The efficiency is about 80 %. System tests with pixel modules have shown that the noise of the modules is not increased by using these DC-DC converters (Fig. 2, bottom right).

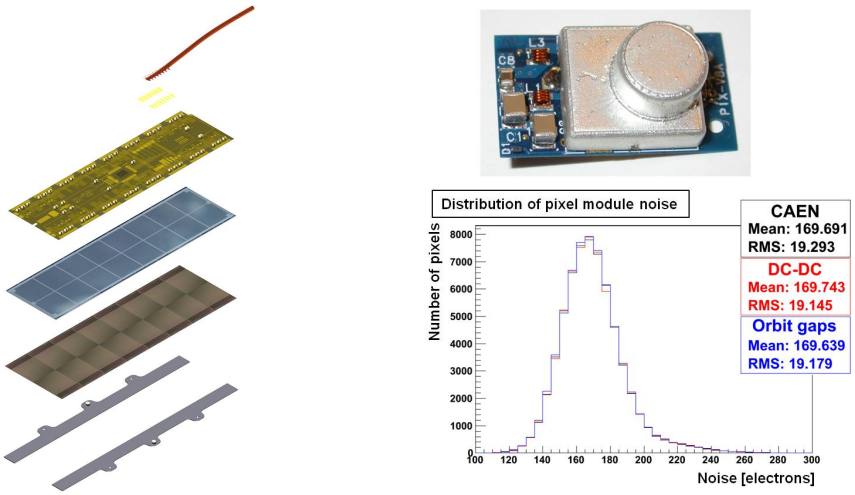

Figure 2: Left: exploded view of the BPIX module layout for layers 2-4. Right: DC-DC converter (top) and noise distributions of all pixels from one module (bottom) without (black) and with DC-DC converters, for different load conditions (red and blue).

3. The Phase-2 Tracker Upgrade

3.1 Concept and Layout

The requirements for the Phase-2 outer tracker are demanding. The new detector must be sufficiently radiation-tolerant to withstand the radiation levels expected for an integrated luminosity of 3000 fb^{-1}. The granularity must be high enough to keep the occupancy at the few per cent level, so that 100-200 simultaneous collisions per bunch crossing can be resolved. The amount of material should be decreased with respect to the present tracker, to improve tracking performance at low transverse momentum, p_T. Finally the tracker is required to provide input to the Level 1 (L1) trigger of CMS, which will enable a reduction of trigger rates with respect to a situation where only calorimeter and muon trigger objects are used, without losing physics performance.

The concept foresees that the tracker provides a reduced amount of data to the L1 trigger at 40 MHz, while the complete tracker information is shipped out only upon reception of a L1 trigger. To reduce the volume of the trigger data, low p_T tracks are locally rejected. So-called "p_T modules" will perform the discrimination between high and low p_T tracks. Level 1 tracks with p_T above a certain threshold (e.g. 2 GeV) are then formed at the back-end.

After careful studies a classical layout with a barrel and end caps was adopted as baseline. Compared with the alternative long-barrel geometry, it provides excellent performance at lower power, material and cost. Six barrel layers and five disks per side with in total 15 348 modules are currently foreseen (Fig. 3, left). The inner region with $r < 60$ cm will be instrumented with modules with one strip (S) and one pixel (P) sensor mounted back-to-back ("PS p_T modules"), while modules with two strip sensors mounted back-to-back will be installed further outside ("2S p_T modules").

The pixel detector will have four barrel layers plus forward disks. An extension of the pixel system to $|\eta| \approx 4$ is under consideration.

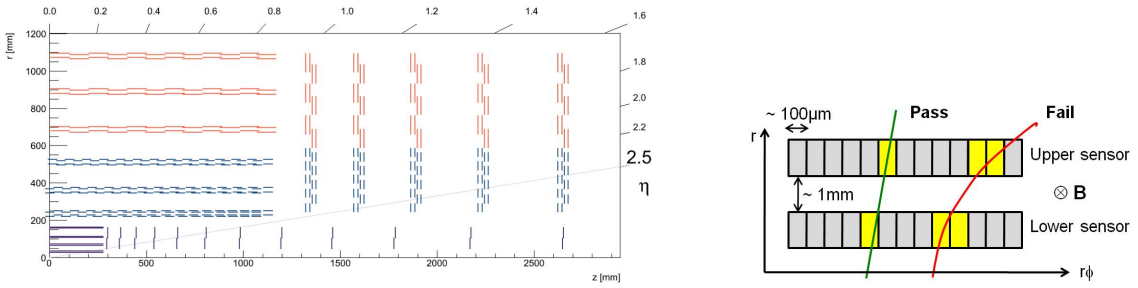

Figure 3: Left: $r-z$ view of one quarter of the CMS tracker layout for the Phase-2 Upgrade. In violet the pixel detector is shown, while blue and red lines indicate PS and 2S modules, respectively. Right: Sketch illustrating the correlation of hits in closely-spaced sensor layers.

3.2 Track Trigger and p_T Modules

Presently tracking information is used at the High Level Trigger (HLT) only. To reduce the trigger rates at HL-LHC, tracking data is to be used already at L1. To limit the associated data volume, low p_T tracks are identified by their bending in the strong magnetic field of CMS, and are rejected. To measure the bending, hit patterns in two closely spaced (1-4 mm) detector layers are compared and 2-cluster tracklets ("stubs") are formed (Fig. 3, right). Stubs with a p_T above a certain threshold are shipped out and used to form tracks at the back-end, e.g. by using associative memories for fast pattern recognition. These tracks are then combined with other trigger objects.

The two module types are shown in Fig. 4. The 2S module has an area of 10 cm x 10 cm and consists of two sensors with 5 cm long strips and a pitch of 90 μm. The sensors are wire-bonded from top and bottom to the readout hybrids, which each carry eight CMS Binary Chips (CBCs) plus a Data Concentrator chip. The PS module is half as large. The upper sensor carries short strips with dimensions of 2.5 cm x 100 μm, which are wire-bonded to hybrids with readout chips. The lower sensor is structured with large pixels of dimensions 1.5 mm x 100 μm, and is bump-bonded to dedicated readout chips. This module can therefore provide accurate z information. Both modules carry a DC-DC converter and a GBTX chip plus opto-electrical converters on service hybrids.

R&D on the CBC [5] is well advanced. The 2 x 127 channel chip is fabricated in 130 nm CMOS technology, and mounted with C4 bump bonds. It features unsparsified binary readout. The chip receives data from both sensors and also from a number of "neighbour" channels through wire bonds. After amplification and hit detection, clusters are formed. Following a cluster width discrimination step, clusters from the lower and upper sensor within a programmable window and with programmable channel offset are correlated. Stubs are formed and passed to the Data Concentrator. Tests with the second version of the chip (CBC2), using mini-modules with two CBC2s, a prototype hybrid and two test sensors, have shown that the chip works well. Stubs are correctly found both using test pulses and with cosmic muon data.

3.3 Sensors for the Outer Tracker

A test campaign was conducted to identify suitable silicon sensors for the Phase-2 outer tracker [6]. Wafers of different material (Floatzone (FZ), Magnetic Czochralski (MCz) and Epitaxial), polarities (n-type = p-in-n; and p-type = n-in-p, with p-stop and p-spray isolation), and

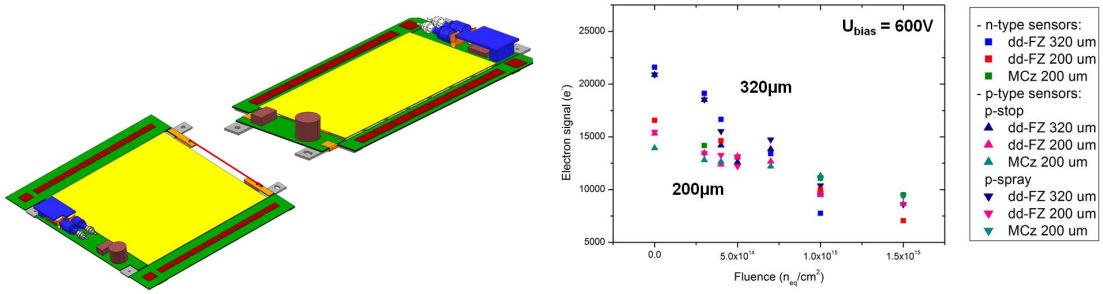

Figure 4: Drawings of the 2S module (left) and PS module (middle), not to scale. Right: charge versus fluence for sensors of various materials, polarities and thicknesses ("dd" stands for "deep diffused").

thicknesses (120, 200 (physically thinned or deep diffused), 320 μm) from the same supplier have been investigated. The wafers carry a variety of test structures and test sensors with different strip lengths, pitches and strip widths. The structures were irradiated in steps with both protons and neutrons. It could be shown that the advantage of thick sensors, namely generation of a larger signal, does not hold for very high fluences (Fig. 4, right). N-type sensors are disfavoured, as non-Gaussian noise was observed after large fluences in these sensors. The preferred option is therefore p-type sensors with a thickness of 200 μm.

4. Summary

The Phase-1 pixel detector, to be installed in a technical stop 2016/17, is under construction. Changes to the geometry, an improved readout chip and reduction of material will improve the performance of the CMS pixel detector.

The Phase-2 outer tracker upgrade is also taking shape. The baseline layout and module design, including the sensor polarity, have been chosen. The requirement to contribute information to the trigger represents an unprecedented challenge, and R&D is performed both on the front-end and back-end part of the readout and data handling. A technical proposal is planned for 2014.

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