

## DEPFET pixel detectors for future electron-positron experiments

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The DEPFET Collaboration develops highly granular, ultra-thin pixel detectors for outstanding vertex reconstruction at future collider experiments. A DEPFET sensor, by the integration of a field effect transistor on a fully depleted silicon bulk, provides simultaneously position sensitive detector capabilities and in-pixel amplification. The characterization of the latest DEPFET prototypes has proven that a comfortable signal to noise ratio and excellent single point resolution can be achieved for a sensor thickness of 50 micrometers. The close to final auxiliary ASICs have been produced and found to operate a DEPFET pixel detector of the latest generation with the required read-out speed. A complete detector concept is being developed for the Belle II experiment at the new Japanese super flavor factory. DEPFET is not only the technology of choice for the Belle II vertex detector, but also a solid candidate for the ILC. Therefore, in this paper, the status of DEPFET R&D project is reviewed in the light of the requirements of the vertex detector at a future electron-positron collider.

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## 1. Introduction

The discovery of a new boson at the LHC (CERN) [1] in Summer 2012 represents an inflexion point in understanding the final physics laws that govern our Universe. The new particle discovered looks, in terms of mass, production and decay, like the Higgs boson predicted by the Standard Model (SM) [2]. This new particle is unique, since it is the only fundamental scalar (spin 0) particle detected up to now and represents therefore a totally new form of matter. Still, the big question remains: is it finally the SM Higgs boson or something else? In order to give an unambiguous answer to this question, a deep exploration of its mass and couplings with high precision is necessary. In this sense, a linear  $e^+e^-$  collider seems the best suited machine to reach such an ultimate precision regime [3] [4] and, indeed, the preparations towards an International Linear Collider (ILC) are already very advanced [5].

At a multi-GeV electron-positron linear collider the well-defined initial state in the collisions would allow to probe, amongst many other physics processes [6], the model independent Higgs production [7]. In order to fully exploit the capabilities of such a precision machine excellent detectors, beyond the current state of the art defined by the LHC experiments, are needed. The detector concepts at the International Linear Collider (ILD [8] and SiD [9]) are general purpose detector systems with solenoidal magnets, hermetic coverage, excellent vertex detectors, precise trackers, highly segmented imaging calorimeters and efficient muon chambers.

An alternative approach to stress-test the Standard Model and eventually find evidence of New Physics is through ultra-high luminosity machines. Those factories, running at intermediate energies, could complement the direct discoveries of the energy frontier machines like ILC by the detailed study of the flavor structure of the SM and beyond.

The inner detector systems in both, energy and luminosity frontier machines, have to cope with very stringent requirements [10] [11]: high-resolution low-mass trackers and extremely ultra-transparent granular pixel vertex detectors.

DEPFET<sup>1</sup> due to its excellent spatial resolution, low material budget and low power consumption has been chosen as the baseline for the pixel detector of the Belle II experiment in the new Japanese super flavor factory and is one of the candidate technologies for the vertex detector of the linear collider concepts [12].

## 2. The DEPFET Pixel Detector

The DEPFET detectors developed for the Belle II pixel detector (PXD) are almost prototypes of the two innermost layers of the ILD vertex detector non only geometrically (sensitive length and width) but also in the key operational parameters as shown in table 1. The combination of excellent resolution, minimal material budget and low power dissipation is a substantial challenge for the vertex detector systems of the future detectors in high energy physics.

### 2.1 The DEPFET technology

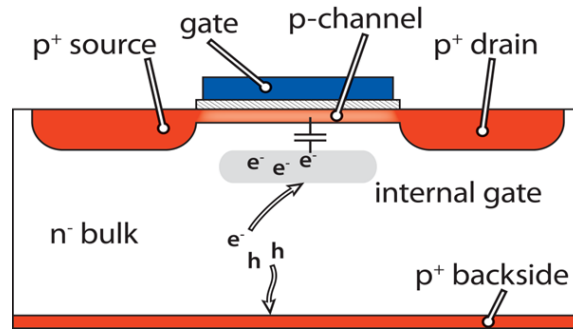
DEPFET is an active pixel solid state detector technology that exploits the concept of amplifying p-channel field effect transistors in a fully sidewards depleted n-type silicon bulk. A schematic

<sup>1</sup>DEpleted P-channel Field Effect Transistor

	Belle II pixel detector	ILC detector concepts
Occupancy [hits/ $\mu\text{m}^2/\text{s}$ ]	0.4	0.1
TID per year [Mrad]	2.0	0.1
NIEL per year [1 MeV $n_{eq}$ ]	$2.0 \times 10^{12}$	$1.0 \times 10^{11}$
Frame readout time [ $\mu\text{s}$ ]	20	20-100
Material budget per layer [ $X_0$ ]	0.2 %	0.1 %
Resolution [ $\mu\text{m}$ ]	10	3

**Table 1:** Comparison of the main requirements for the Belle II and ILC vertex detectors. The combination of all these factors is a substantial challenge for the detector system.

view of one DEPFET cell is shown in figure 1. An additional  $n^+$  implant (*internal gate*) underneath the transistor's channel forms a potential minimum for the electrons in the substrate. The charges drift towards the internal gate and, once there, modulate proportionally the current flowing between the source and drain. After the read-out, the charges can be removed from the internal gate by applying a periodic voltage pulse to a *clear* contact placed on the periphery of each pixel [13].



**Figure 1:** Schematic view of a DEPFET pixel. The internal gate represents the minimum of potential for the electrons created by impinging particles in the substrate, where they are collected.

A DEPFET sensor provides detection, fast charge collection and internal amplification at the same time. Due to the small capacitance of the collection node, the DEPFET has a low intrinsic noise while a large signal is achieved due to the fully depleted bulk, resulting in a device with a large signal-to-noise ratio (SNR) even with a very thin detector substrate [14]. The crucial parameter of the DEPFET technology is the internal amplification of the device ( $g_q$ ). The gain of this first stage is expected for the final Belle II PXD sensors of the order of  $500 \text{ pA}/e^-$ , although 50 % higher values were achieved with thicker sensors and dielectrics in previous DEPFET productions [15].

## 2.2 Mode of operation

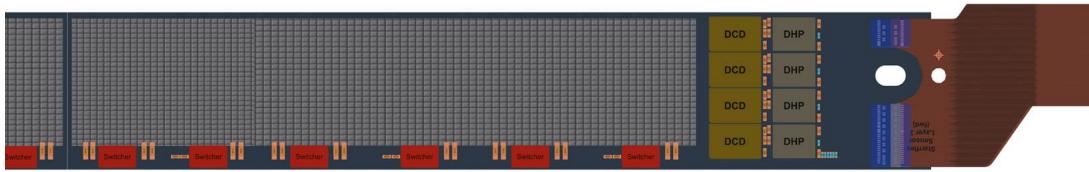
A DEPFET sensor is a combination of individual DEPFET pixels arranged in a matrix and operated together. The gate and clear lines of the pixels placed on the same matrix row are connected to a control chip (*Switcher – B*) [16], while the pixels on the same column have the drain contacts connected to a current receiver ASIC (*DCDB* or Drain Current Digitizer) [17]. The use of long drain readout lines allows to keep material (front end electronics and cooling) out of the accep-

tance volume. The auxiliary electronics needed to operate a DEPFET detector will be explained in the next section.

Such a pixel matrix is operated in *rolling – shutter* mode as follows. The drain current of all the pixels lying on the same row is sampled once per cycle before the clearing; once a row is read out and cleared, the next row is processed (row-wise readout<sup>2</sup>). The pedestal subtraction is done in the digital domain in a processor chip (*DHP* or Data Handling Processor) [18]. Although the long drain lines may compromise the settling of the drain current signal, it has been demonstrated [19] with DCD dynamic measurements that, with a  $\sim 6$  cm long DEPFET sensor, a read-clear cycle can be performed in 92 ns reaching the target speed of 100 ns for the Belle II PXD (50 KHz frame rate).

### 2.3 Auxiliary electronics

The basic unit on a DEPFET-based vertex detector (*half-ladder*) is depicted in figure 2. By the repetition, in a cylindrical arrangement of this all-silicon ladder (two half ladders glued together) around the beam pipe, the geometry of the vertex detector is therefore implemented.



**Figure 2:** Schematic view of an all-silicon DEPFET (half) ladder. The front-end ASICs (on the right hand side) are bump bonded directly on the thick silicon integrated support structure that keeps the stiffness of the assembly. The control chips are placed in the lateral balcony next to the sensor, that fills the central part of the ladder.

In order to meet the low material budget requirement, the sensitive area placed in the central part of a DEPFET ladder is ground to the thickness required by the specific application. The thinning technology uses anisotropic etching on bonded wafers to create a thin, self supporting sensor, where no additional support structures are needed. The use of a single type of material for sensor and support structure avoids mechanical stress due to absence of CTE<sup>3</sup> mismatch. The stiffness is provided by a thick<sup>4</sup> (400  $\mu\text{m}$ ) silicon rim around the sensor, where the auxiliary ASICs are directly bonded to. The row control is provided by the steering chips placed in the narrow balcony that runs along the length of the ladder next to the sensitive area, while the analog front-end and the electronics for first data compression are at both ends of the ladder.

The Switcher-B, that allows the selection and the clearing of segments of pixels row-wise, has 32 channels and is implemented in AMS high voltage 0.35  $\mu\text{m}$  technology. This chip contains a driver that can provide the high clear pulse needed to remove the collected charges from the internal gate. Using thin gate oxides and a special design of enclosed transistors and guard rings, a radiation tolerance up 360 kGy is demonstrated [20]. The drain current of each pixel is processed

<sup>2</sup>In practice, multiple rows can be read out in parallel at the same time, reducing the frame time proportionally

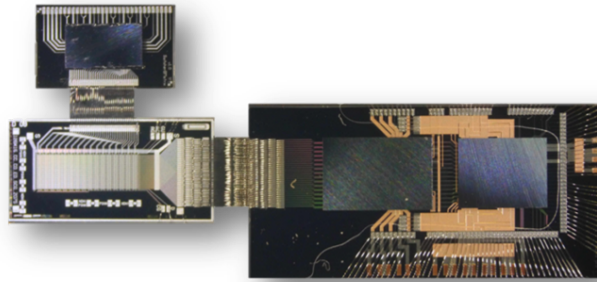
<sup>3</sup>Coefficient of Thermal Expansion

<sup>4</sup>Additional grooves are etched for further material reduction

by the DCDB chip that, fabricated in UMC 180 nm technology, has 256 analog inputs. The current receiver is based on transimpedance amplifiers and the analog signal is further digitized by an 8 bits algorithmic ADC, with a sample rate of 10 MSamples/s. The chip is found to be fully functional after an integrated dose of 200 kGy. The digitized data in the DCDB is then sent to the DHP where the first data reduction is performed. This ASIC, fabricated in IBM 90 nm technology<sup>5</sup> can store raw data and pedestals, perform the common mode correction, pedestal subtraction and zero suppression and can control and configure the rest of the other ASIC types in the ladder. The most radiation sensitive parts (PLL<sup>6</sup> and CML<sup>7</sup> driver) have been tested to work properly after 1000 kGy. All the full-size close to final versions of the Belle II ASICs mentioned here are designed, produced and found to work together at nominal speed (320 MHz frequency equivalent to 100 ns sampling period and leading to 20  $\mu$ s frame integration time).

### 3. Latest sensor prototype production

A DEPFET production is a process that includes more than 90 fabrication steps; amongst others, nine implantations, more than twenty lithographies, double poly silicon layers, three metal layers and the back side processing.



**Figure 3:** Picture of the Belle II concept demonstrator. A minimal system composed by one DEPFET sensor of the latest prototype run has been operated with the close to final version of the ASICs.

Although previous prototype runs explored the performance of (450  $\mu$ m thick) sensors with small pixel pitch (20 $\times$ 20  $\mu$ m<sup>2</sup>) [21] [22], the first thin DEPFET matrices are produced in the latest Belle II prototype production, called *PXD6*. The *PXD6* generation includes 8 wafers with small (50  $\mu$ m) thin matrices with large pixel pitch (50 $\times$ 50  $\mu$ m<sup>2</sup> and 50 $\times$ 75  $\mu$ m<sup>2</sup>) tailored to the Belle II requirements and different technology variations (clear and drift structures) in addition to full size sensors for prototyping.

This new prototype run includes devices with a factor two thinner dielectrics than previous productions, ensuring radiation hardness up to the full expected doses in Belle II [23].

One of the small DEPFET sensors produced in the latest generation has been assembled (figure 3) in a test board and equipped with the minimum necessary amount of components to be

<sup>5</sup>The final production is being produced in TSMC 65 nm CMOS technology instead

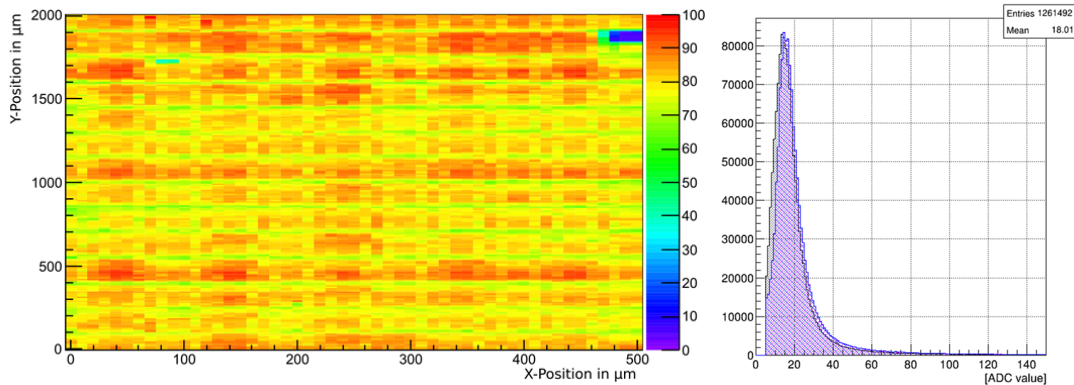
<sup>6</sup>Phase-Locked Loop

<sup>7</sup>Current-Mode Logic

operated (a SwitcherB, a DCDB and a DHP) and a full characterization of its performance has been carried out.

#### 4. Prototype tests

The performance of thin DEPFET sensors from the latest prototype production has been extensively studied with lasers and radioactive sources in the laboratory as well as in beam tests at CERN and DESY [24]. The first step before investigating the different properties of a DEPFET detector includes the optimization of the different bias voltages from the sensor and also the FEE<sup>8</sup>. The charge collection uniformity of the signal over a large area of the sensor has been evaluated using a laser scan (figure 4 (Left)). In this particular design, less than 6 % of signal spread was found in the signal collection over an area of  $16 \times 26$  pixels. A systematic charge collection difference was found between odd and even rows of the device which origin is still under investigation. This effect is not observed to create any degradation in the performance of the detector since the efficiency stayed above 99.5 % independently of the position of the impinging particle.



**Figure 4:** (Left) A  $16 \times 26$  pixels area of the DEPFET sensor was scanned with a laser to study the signal collection uniformity over large regions. (Right) Cluster signal for perpendicular incident 6 GeV electrons.

For optimal operating parameters the cluster  $5 \times 5$  signal created by perpendicular impinging MIPs<sup>9</sup> is shown in figure 4 (Right). The observed distribution has a Landau shape and the gain of the first in-pixel amplification stage can be obtained<sup>10</sup> from the peak position to be  $g_q \sim 450$  pA/e<sup>-</sup>, compatible with the designed value.

In addition, the intrinsic resolution of the detector matches the detector requirements for perpendicular tracks, obtaining  $\sim 10$  μm with a pixel pitch of  $50 \times 50$  μm<sup>2</sup> and approaching 1 μm with  $20 \times 20$  μm<sup>2</sup> and 450 μm thick ILC-like sensor type [25].

#### 5. Summary

The DEPFET Collaboration is developing ultra-transparent active pixel sensors with integrated amplification. The performance of a DEPFET detector system in terms of radiation hardness,

<sup>8</sup>Front End Electronics

<sup>9</sup>Minimum Ionizing Particle

<sup>10</sup>1 ADC unit corresponds to a current of 86 nA

signal-to-noise ratio, material budget, spatial resolution and readout speed can fulfill the challenging requirements imposed on the vertex detectors of the future  $e^+e^-$  colliders.

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