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The DEPFET pixel detector for the Belle II experiment at SuperKEKB

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A pixel detector built with the DEPFET technology will be used for the two innermost layers of the Belle II experiment at the e^+e^- SuperKEKB collider at KEK. The physics goals of the experiment impose challenging requirements to the design of the pixel detector in terms of performance, material budget and power consumption. The DEPFET technology has proven to be a suitable solution for the Belle II requirements and has been chosen as the baseline for the detector. This paper reviews the DEPFET pixel detector for Belle II and the various system aspects that have driven its final design.

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1. The Belle II experiment and its pixel detector

The SuperKEKB [1] collider, an upgrade of the former KEKB, is under construction at KEK. It is an asymmetric (4 GeV, 7 GeV) e^+e^- collider working at the center of mass energy of the $\Upsilon(4S)$ resonance. The design peak luminosity is $8 \times 10^{35}\,\mathrm{cm}^2\,\mathrm{s}^{-1}$, about 40 times larger than KEKB, aiming at an integrated luminosity of $50\,\mathrm{ab}^{-1}$. This increase of the luminosity will be achieved by reducing both the horizontal and vertical size of the beam (*Nano Beam*) by an order of magnitude and by doubling the beam currents [2].

To fully exploit the higher luminosity the former Belle detector is being upgraded [2]. This new spectrometer must cope with the higher backgrounds and event rates and the corresponding larger radiation damage, occupancy and fake hit production. In addition, to cope with beam background at the interaction point, the boost is smaller at SuperKEKB reducing the average separation between the B and $\bar{B}$ vertices by a factor 2, down to about 100 µm. As a consequence, improved vertexing and tracking capabilities are needed in the Belle II detector. This converts the vertex detector in one of the key elements that drive the physics performance. It consists of four layers of double-sided silicon strip detectors, SVD [2], in the outer radii and two layers of highly granular pixel sensors in the innermost part, known as PXD [2].

The PXD is intended to improve vertex resolution and will be placed with the first layer at 1.4 cm from the beam line and the second layer at 2.2 cm. As a consequence of the low momentum of the particles in the final state (< 1 GeV/c), the hit position determination is intrinsically limited due to the multiple Coulomb scattering. This sets a lower limit of 10 µm for the spatial resolution in the PXD that can be achieved with a moderate pixel size of 50×50 µm^2. This pixel size is also enough to cope with the expected occupancy of $0.4\,\mathrm{hits/\mu m^2/s}$. For the same reason the material budget must be kept low, up to a maximum of $\sim$0.2% $\mathrm{X}_\circ$ per layer, implying a thickness of 75 µm of the sensitive part of the sensor. The acceptance of the detector must cover the range 17°-155° in azimuth angle. The detector will be read continuously with a frame time of 20 µs keeping the occupancy below 3%. This continuous readout means that ASICs are *ON* all the time, which together with the restrictions on the material budget sets the requirements for cooling. Finally, according to the simulations, the radiation dose expected in the inner region of the detector is around 2 Mrad/year.

2. The DEPFET detector

2.1 The DEPFET sensor

Each DEPFET [3] pixel consists of a field effect transistor (FET) integrated on a high resistivity n–type sidewards depleted silicon bulk (Fig. 1). A deep n–doping implantation, the internal gate, creates a minimum of potential for electrons at around 1 µm underneath the transistor's gate. The electrons created by a traversing particle, will drift towards the surface of the device and will accumulate in the internal gate. This charge modulates the current through the pMOS transistor channel, which is used as the readout signal. The figure of merit is the internal amplification of the device, g_q, which defines the internal gain in terms of pA per collected electron. The values expected for the final sensors are in the order of $400\,\mathrm{pA}/e^-$ [4]. After a successful reading, the electrons have to be completely removed very fast from the internal gate. Incomplete removal of

the charge would interfere with the next measurement. This is done via a *clear* contact (n^+ type implant) that is placed on the periphery of each pixel. The potential barrier between the clear contact and the internal gate is modulated with an additional implant called *cleargate*.

Thanks to its specific architecture, the DEPFET sensors provide detection with fast charge collection and internal amplification at the same time. The low capacitance of the internal gate and the small intrinsic noise, in the order of $\sim$50 nA, allow to build thin detectors with an excellent signal over noise ratio [5].

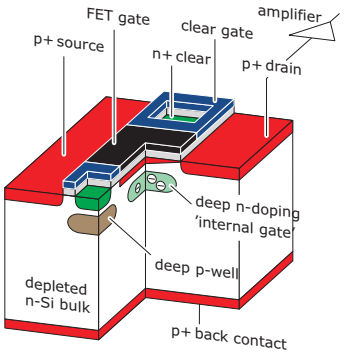

Figure 1: Sketch of a DEPFET pixel where one can appreciate the internal gate where electrons produced by particles are accumulated.

2.1.1 Radiation tolerance

Two main radiation damage mechanisms will affect the performance of the DEPFET sensors. The first one, due to surface damage as a result of the expected $\sim$2 Mrad/year, will affect the threshold voltage of the pMOS and clear gates and, also, in the case of the pMOS gate, reduce the internal amplification of the device due to the reduced mobility of the charge carriers in the pMOS conducting channel. The second has to do with, mainly, the increase of leakage current and noise produced by the expected $1.2 \times 10^{13}\,\mathrm{cm}^{-2}$ 1 MeV neutron equivalent fluence per year. The former problem is solved by a combination of oxide thinning in the pMOS gate and the addition of a very thin layer of Si_3N_4 on top of the usual SiO_2, which has some nice features like the fact that it can also trap electrons leading to a compensation of radiation effects. The loss of internal gain due to oxide thinning can be compensated by reducing the gate length. The latter problem is solved by reducing the operating temperature of the sensors.

2.2 The DEPFET pixel matrix

A DEPFET pixel detector is made of an array of small DEPFET pixels arranged in a rectangular matrix. In order to operate the matrix a steering chip, SwitcherB [6], is needed to drive the pMOS gate and clear voltages and a second chip, the DCDB [7], to digitise the pMOS drain current. A third chip, the DHP [8], is also used in the Belle II PXD for data reduction (pedestal, common mode and zero suppression) as well as for handling of timing and control signals. Details of the ASICs can be found in the references given above.

The matrix is operated in *rolling shutter* mode, i.e. one row is activated and read at a time and then cleared. In the case of the PXD DEPFET module 4 rows are read at a time to reduce the time required to read a full frame. All the pixels in a stripe of 4 rows are connected to the same SwitcherB clear and gate channels. Only the activated rows consume power, while the others, even if not active, are still sensitive to charge. This is key to keep the power consumption very low in the sensitive region of the module. All the channels in the same column share the same DCDB channel. Long drain readout lines are used to keep most of the material (DCD and DHP chips) and generated heat out of the acceptance region. Fig. 2 shows a 3D model of a PXD module with the steering chips along the side and the digitiser and data handling chips at the end of the module.

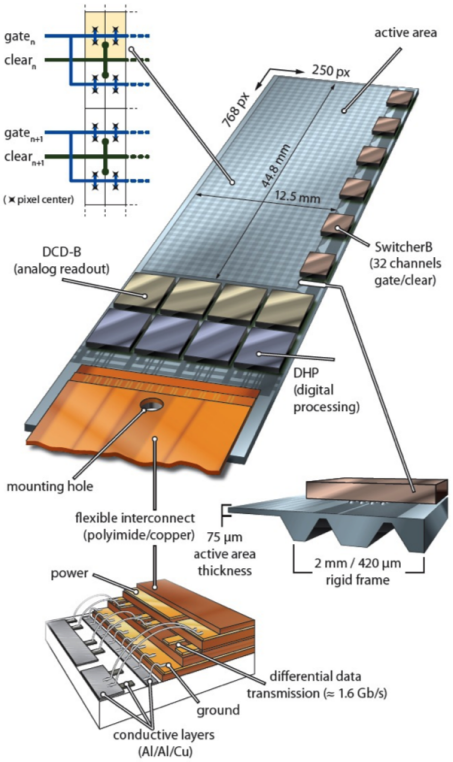

Figure 2: Sketch of a pixel matrix showing the path of the steering signals produced by the ASICs to activate and deactivating the transistors and the data lines connected to the readout ASICS at the bottom.

Each DEPFET matrix has 768×250 pixels as shown in Table 1. To cope with the 192 stripes of 4 rows each, 6 SwitcherB chips are located along the module on a 2 mm wide and 420 µm thick balcony (see Fig. 2). For each of the columns in a stripe, 4 data lines are needed, one for each of the rows. These 1000 data lines are handled by 4 DCDB chips with 250 channels each.

Careful laboratory measurements have proven that the read–clear cycle can be done in 92 ns (10.83 MHz row rate) [9]. Using a 100 ns cycle, 19.2 µs would be needed to read out sequentially all the 192 stripes in a full frame, which fulfils the Belle II requirement of 20 µs (50 kHz frame rate) for a PXD matrix.

2.3 Sensor Thinning

DEPFET sensors for Belle II are thinned down to 75 µm in the sensitive area. Conventional techniques like backside grinding or chemical mechanical polishing (CMP) cannot be used since the backside is electrically active. A special technology [10] has been developed that first processes the back side of the *sensor* wafer which is afterwards bonded onto a *handling* wafer. The sensor wafer is then thinned from the top with conventional methods, down to the desired thickness, and processed. Anisotropic edging is used to open the window under the sensitive area leaving, in the case of the Belle II PXD, a 75 µm thick silicon *membrane* containing the DEPFET active pixels. The handling wafer stays as a 420 µm thick frame that provides mechanical stiffness and support for the thin active pixel (Fig. 3) with the added value of a uniform coefficient of thermal expansion since it is an all silicon structure.

2.4 The DEPFET ladder

A DEPFET ladder consists of two self-supporting modules or half-ladders glued together with a ceramic reinforcement beam as shown in Fig. 3. The ceramic beams provide enough stiffness to the long ladders. Two different modules, symmetric with respect to the short edge with the groves for the ceramic beams, will be used for each of the two pixel layers in the Belle II PXD. Each of the modules will have, see Table 1, 768×250 pixels. Given that the tracks will impinge with larger angles in the region closer to the end of module the intrinsic spatial resolution does not need to be as good as in the central region, and therefore the modules have been divided in two regions with different pixel sizes as indicated in Table 1.

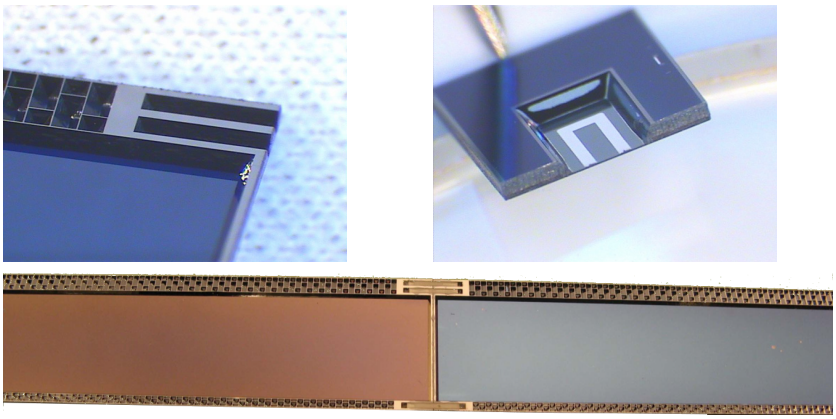

Figure 3: Top Left: Thinned module, showing the structured frame around the very thin sensitive region. Top Right: Picture of a test structure showing the thickness difference between the frame and the thinned layer. Bottom: picture showing how two modules are glued together, by means of ceramic beams glued in specific groves in the module to form a long ladder

	Inner Layer (L1)	Outer Layer (L2)
no. of modules	8	12
Thickness (µm)	75	75
no. of pixels/module	768×250	768×250
Pixel size (µm^2) /CENTER	55×50	70×50
/FORWARD	60×50	85×50
Sensitive area (mm^2)	44.8×12.5	61.44×12.5

Table 1: Parameters of the half-modules in each of the 2 layers of the PXD.

Three different types of ASICs are bump bonded on the module, namely, the DCDB, the SwitcherB and the DHP (see section 2.2). A solderable landing pad on the sensor substrate is needed for a correct bump bonding. A third metal layer made of copper has been introducedto solve this, since copper is solder wettable, and to reduce the resistivity between critical blocks in the periphery of the pixels. Passive components such as decoupling capacitors and termination resistors of sizes 01005 and 0201 are also soldered directly on the module. Signal and power lines are routed on three metal layers, two of aluminium and the top one of copper.

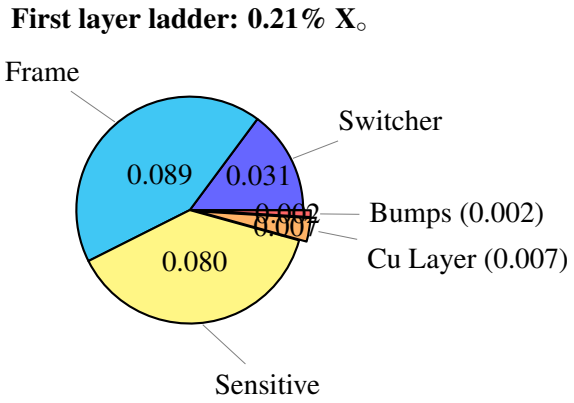

Figure 4: Distribution of material in the module.

A breakdown of the detector material over the acceptance with the most important contribu-

tions is presented in Fig. 4. The ladder material corresponds to 0.21% $X_\circ$/layer over the active area. There is no contribution from the DCDB and the DHP to the material since they are placed out of the acceptance.

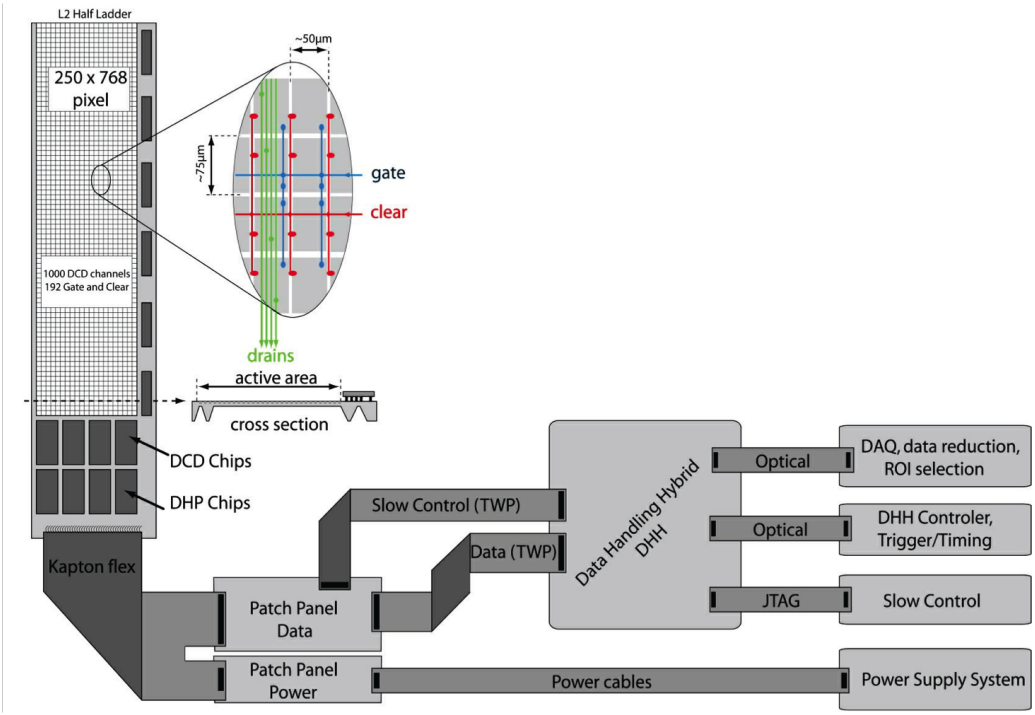

Figure 5: Off detector electronics (only one module is shown)

3. The full readout chain and backend electronics

A 50cm Kapton flexprint connects the DEPFET module with the off-detector electronics and power supplies. As shown in Fig. 2 the cable is attached at the end of the module behind the DHP devices and wire–bonded to dedicated pads on the module. Fig. 5 depicts the full-scheme from the DEPFET module to the power supply and computing infrastructure, with two passive patch panels and the DHH (Data Handling Hybrid).

The data patch panel redistributes the fast and slow signals to the DHH. The goal of the DHH is twofold. On the one hand, the DHH receives the timing and trigger signals and the slow control commands from the Belle II environment and sends them to the DHP devices. On the other hand, it receives and multiplexes the data from the four DHP devices and transmits it, via an optical link, to the back-end ATCA architecture computing nodes, where further data buffering and signal processing is performed. The power patch-panel is used to redistribute the power lines and for filtering and decoupling. The power supply system to operate the DEPFET modules is a complex one in terms of number of different supply channels (∼20 voltage levels), noise performance sensitivity and voltage regulation, as described in [11].

4. Performance

Many beam tests were performed with different types of thick (450 µm) DEPFET sensors in the past (see [5] and references therein). This paper, however, will briefly report on the results obtained with thinned sensor prototypes operated with close to final readout electronics running at full speed during the May 2013 beam test performed at DESY (Hamburg).

The device under test was a 50 µm thin PXD like sensor with 32×64 pixels assembled together with a DCDB and a SwitcherB, see Fig. 6. The pixel pitch was $50\times75\,\mu m^2$ and two different pixel gate lengths were evaluated. Both the SwitcherB and DCDB were operated at full speed, i.e. 100 ns read–clear cycle. The results show that these sensors exhibit a charge collection efficiency above 99%. The signal over noise ratio for MIPs was measured to be between 20–40 depending on the gate length of the pixel matrix. Fig. 7.a shows the charge distribution of the prototype with the baseline design gate length of 4 µm. It features a most probable value of 23.9±0.3, and a signal over noise ratio of 41.5±0.4. From that a value of $g_q\approx450$ pA/e$^-$ is obtained. Fig. 7.b shows that a resolution of 10 µm was achieved with thinned sensors.

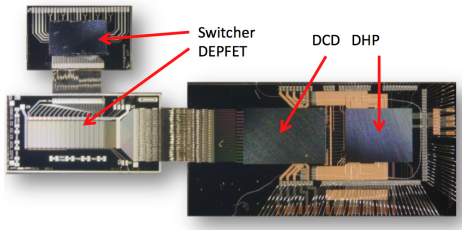

Figure 6: Prototype module tested during the 2013 DESY beam test using the full readout chain.

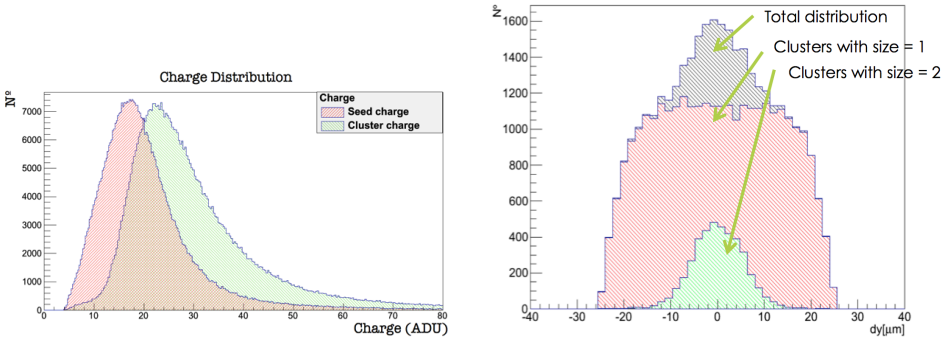

Figure 7: (Left) Charge collection distribution with a most probable value of 23.9 (Right) Residual distribution showing a resolution of 10 µm when charge is shared among pixels.

5. The Electric MultiChip Module (E–MCM)

The E–MCM is an electrically active prototype of a half-module. It contains all the elements but the DEPFET pixels. The E–MCM should allow to study and characterise the routing of the final modules and the electronic components. The metal process of the E–MCM is as close as possible to the final modules so it can provide valuable feedback on the electrical properties and metalization process and prove the technological feasibility of the 3 metal layers. In addition, it

can be used as starting point to practice the final modules commissioning and to establish a well defined quality assurance policy.

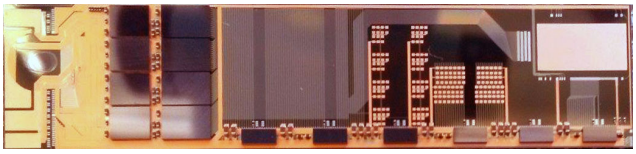

Figure 8: Fully populated E–MCM module.

Fig 8 shows a fully populated E–MCM module which is currently under characterisation. The most relevant steps to assemble the modules are: electrical test of all interconnections to test for opens and shorts, flip-chip the three types of ASICs onto their corresponding copper pads, solder the close to 70 passive components of 01005 and 0201 sizes and attachment of the Kapton cable to the module end.

6. PXD System Engineering

6.1 Support

An overview of the mechanical design of the PXD is shown in Fig. 9. The ladders are mounted on stainless steel blocks which also serve to dissipate the heat produced by the readout electronics. This blocks have integrated cooling channels to circulate cold, dry air and capillaries for the 2-phase CO_2 cooling. The blocks are mounted on the beam pipe structure so that the PXD will follow any movement of the beam pipe.

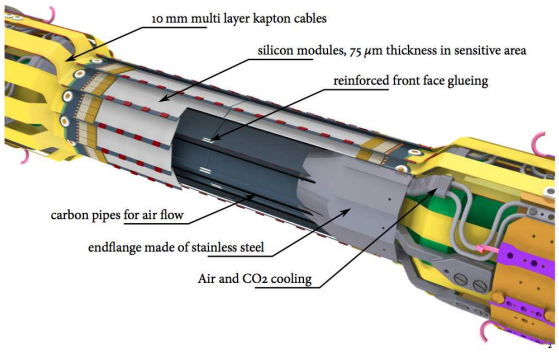

Figure 9: Schematic view of the PXD mounted on the beam pipe including silicon modules, the kapton flex, the support and cooling blocks as well as the cooling pipes.

6.2 Thermal studies

The power dissipation of the PXD must be removed with minimal material in the acceptance region. Finite element simulations (FEA) and laboratory measurements [12] have proven that the

2-phase CO_2 circulating through the cooling blocks is enough to remove the heat produced by the readout electronics. The center of the ladders has to rely on forced convection with cold, dry air. The total power consumption is around 9 W per module (0.5 W the Switchers, 6 W the DCDs, 2 W the DHPs and 0.5 W distributed homogeneously in the active area) adding up to 360 W for the whole PXD. The temperature of the sensors (to keep the leakage current at modest levels) and chips (to prevent electro-migration) should not exceed 30 °C and 60 °C respectively.

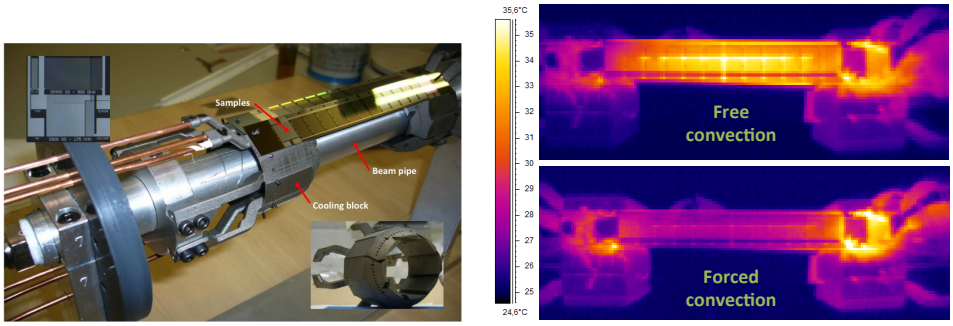

Figure 10: (left) Setup for the thermal measurements using sensor mechanical samples, with integrated resistors, and cooling blocks. (right) Images acquired with an infra–red camera with and without forced convection.

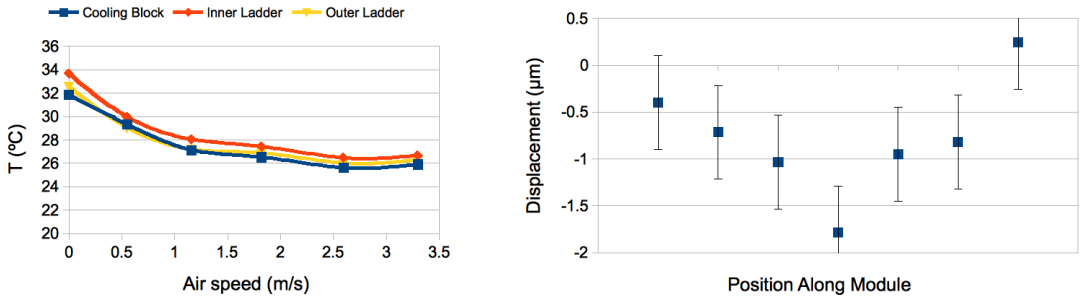

Figure 11: (Left) Temperature as a function of air speed showing that a gentle flow of 2 m/s is enough to reach the plateau of forced convection. (Right) Measured deformation due to the air flow along the module. The maximum deformation happens at the center and is about 2 μm.

Measurements made on a thermal mockup (see Fig. 10) validated the FEA models. The mockup was built using close to final cooling blocks, silicon modules with real thickness and with integrated resistors that were populated with temperature sensors in strategic places. An open CO_2 system operated at -30 °C and dry air cooled with liquid nitrogen were circulated through the cooling blocks. The ambient temperature was 25 °C. Fig.10 shows that this combination keeps the temperature within the required limits with a gradient along the module below 5 °C. Fig. 11 shows that an air flow of 2 m/s is enough to get to the forced convection plateau and the deformation along the module due to this air flow is of the order of 2 µm as measured with capacitive displacement sensors located along the module.

7. Conclusions

A pixel detector (PXD) based on DEPFET technology is being developed for the new Flavour Factory (SuperKEKB) under construction in KEK (Japan). This machine will deliver a luminosity never achieved before and the requirements for the PXD are stringent in terms of resolution, power consumption and material budget. Measurements have already proven that thin sensors can be produced and operated at the nominal speed needed in Belle II. The temperature of the detector can be controlled using the cooling concept adopted by the Collaboration. The full readout chain with most of the final system electronics has been tested in beam-tests at DESY. The construction of E–MCM is an important step forward in understanding how to develop the final size monolithic modules thanks to the feedback it will provide on the metalization process and electrical properties as well as on the commissioning procedures.

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