

The Micro-Vertex Detector of the PANDA Experiment

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The future PANDA apparatus at the international FAIR accelerator facility in Darmstadt is foreseen to study the strong interaction in antiproton-proton annihilations. The experimental setup is composed of a Target Spectrometer surrounding the stationary target and a Forward Spectrometer to accommodate the forward-boosted event topologies. In order to evaluate channels involving charm content, the central tracking system is preceded by the Micro-Vertex Detector (MVD) which allows ultra precise track and secondary vertex resolutions and thus the discrimination of short-lived charmonium states from the background. The MVD will consist of four barrels of silicon detectors, two layers consisting of silicon pixel sensors, and two layers of double-sided silicon strip sensors as well as a set of forward disks comprising both technologies. The presentation will focus on the technological aspects of design and construction of the detector, particularly the challenging constraints, such as the absence of a central hardware trigger, the required track resolution, the limited power consumption and the radiation hardness of its components. The efforts undertaken so far in prototyping and testing are reviewed and first results are discussed.[†] PoS(Vertex 2013)008

22nd International Workshop on Vertex Detectors September 15th-20th, 2013 Lake Starnberg, Germany

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[†]This work was supported by BMBF (grant no. 05P12RGFP6) and HIC for FAIR

1. Introduction

The existing GSI facility in Darmstadt, Germany will be extended to FAIR (Facility for Antiproton and Ion Research) [1]. This future international accelerator facility, currently under construction, will deliver high intensity beams of protons, antiprotons and ions to several experiments. A focus will be on experiments with antiprotons. The PANDA (antiProton ANnihilation at DArmstadt) experiment will study annihilation reactions between a stored antiproton beam and a stationary gas target [2]. The High-Energy-Storage Ring (HESR) will provide up to $1 \cdot 10^{11}$ antiprotons in a momentum range from 1.5 GeV/c to 15.0 GeV/c. The HESR presents two operation modes: a high luminosity mode with stochastic beam cooling to reach a peak luminosity of $2 \cdot 10^{32} \text{ cm}^{-2} \text{s}^{-1}$ and a high resolution mode employing additional electron cooling to reach a momentum resolution in the order of $\sigma_p/p \leq 4 \cdot 10^{-5}$ [3].

The physics program of $\overline{P}ANDA$ is determined by the performance of the stored beam and the characteristics of antiproton-proton annihilations. In that way, many open questions in the non-perturbative regime of QCD can be approached. The rich and diverse hadron physics program comprises charmonium spectroscopy as well as the search for new objects, predicted in QCD, like glueballs, hybrids and other exotic states. Furthermore, in-medium modifications of hadrons, baryon spectroscopy and CP-violation in the charm sector are possible fields of study.



Figure 1: The left frame shows the $\overline{P}ANDA$ detector that comprises several detector layers divided into a Target Spectrometer and a Forward Spectrometer. The Micro-Vertex Detector is the innermost detector surrounding the interaction zone defined by the crossing of beam pipe and target pipe (right).

As a fixed target experiment, the PANDA detector is composed of a Target Spectrometer and a Forward Spectrometer, to cover almost the full solid angle. The Target Spectrometer is instrumented with a 2 T superconducting solenoid magnet surrounding the internal target along with different detector layers for tracking, particle identification and calorimetry. The Forward Spectrometer with its 2 Tm resistive dipole magnet detects particles under small angles with respect to the beam pipe. The Micro-Vertex Detector (MVD) as part of the tracking system of the Target Spectrometer is designed to detect secondary vertices of charmed and strange hadrons close to the interaction point and to deliver precise tracking information together with other tracking detectors. The required vertex resolution is in the order of 100 µm and was validated from simulations. The MVD is equipped with 2 barrel layers made from hybrid silicon pixel detectors and 2 barrel layers of double-sided silicon strip detectors, respectively. The forward part is covered by 6 disk layers with the inner 4 layers comprised entirely of pixel detectors and the outer 2 layers of strip detectors and, closer to the beam pipe pixel detectors, respectively. This arrangement ensures the requirement for 4 MVD hit points per track, an optimal detector coverage and a material budget below 10% X₀. All components have to be radiation tolerant to non-ionizing radiation loads of up to $10^{14} n_{1Mev_{eq}} cm^{-2}$ and ionizing radiation loads of up to 10 Mrad.

 \overline{P} ANDA's unique data acquisition concept demands that every sub-detector is able to detect hits without requiring an external trigger. Therefore, the deployed front-end electronics has to be able to distinguish physical events from noise and send digital hit information along with a precise time stamp to the event builder. Moreover, the detector must be capable to sustain and handle high interaction rates of up to 20 million antiproton-proton annihilations per second. A maximum of 3 million hits per second will be reached for the most occupied front-end chip in the pixel part. The Technical Design Report for the \overline{P} ANDA MVD has been referred and published [4].

2. The Pixel Subdetector

Figure 2: The picture on the left shows a pixel sensor wafer for the $\overline{P}ANDA$ MVD. On the right a prototype assembly comprising a ToPix v3 bump-bonded to a pixel sensor is depicted.

In order to achieve an excellent spatial resolution and to cope with the high particle flux near the interaction point, the inner layers of the $\overline{P}ANDA$ MVD will employ silicon hybrid pixel detectors. To achieve the requested spatial resolution, a pixel cell size of 100 µm x 100 µm was chosen according to simulations. As sensor material, an n-epitaxial layer grown on a Czochralski substrate was chosen [5]. From tests with different layers, an epi-layer thickness of 100 µm was determined. The production will be carried out using 4 inch wafers of n⁺ conductivity type, Sb doped with

525 µm thickness and a resistivity of $0.01 - 0.02 \Omega \cdot \text{cm}$. The n-type epitaxial layer will have a resistivity of $1000 - 2000 \Omega \cdot \text{cm}$. Sensors in full-size PANDA geometry were produced and tested. Properties such as thinning and planarity were tested as well. Figure 2 shows a photograph of the sensor wafer.

The sensor readout will be done by a custom ASIC bump-bonded to the sensor. The **To**rino **Pixel** readout chip (ToPix), produced in 0.13 µm IBM CMOS technology, is a self-triggering front-end chip [6]. Amplitude measurement is done by means of the Time over Threshold (ToT) technique. Hits are time stamped synchronous to the global $\overline{P}ANDA$ timing clock. The recently submitted prototype version ToPix v4 features two 2 x 128-cells and two 2 x 32-cells double columns with complete pixel cells, end of column control logic and buffers. In order to determine the best single-event upset protection scheme for the pixel logic, Hamming encoding and triple modular redundancy (TMR) was implemented, while the end of column logic employs Hamming encoding. The serial data output is compatible to the SLVS standard of the GBT interface [7]. Previous versions of this triggerless chip were tested for total ionizing dose effects (CERN) and single-event upset (SIRAD-LNL) as well as in test-beams in a beam telescope together with silicon strip detectors [8].

3. The Strip Subdetector

To reduce the number of readout channels, the detector layers further away from the interaction point are equipped with double-sided silicon strip detectors. The strip part of the MVD employs three different sensor geometries: square $(35 \times 35 \text{ mm}^2 \text{ with } 512 \times 512 \text{ strips})$ and rectangular (60 x 35 mm² with 896 x 512 strips) shaped sensors for the barrel part and trapezoidal (58 mm high, 37 mm long side and 22 mm short side with 768 x 768 strips) sensors for the disk part. Figure 3 displays prototype wafers of these sensors. Prototype sensors in the full-size PANDA geometry for the strip detectors of the barrel part as well as for the disk part were produced by CiS, Erfurt [9]. The 285 µm thick sensors with punch-through biasing and 8 guard rings feature p-spray isola-



Figure 3: Strip sensor wafers for the $\overline{P}ANDA$ MVD. Left: Sensors for the barrel part. Right: Sensors for the disk part.

tion on the n-side. The sensors can be read out via AC-coupling or DC-coupling. The square and rectangular sensors have a strip pitch of 65 μ m and a stereo angle between p-side and n-side of 90°. The trapezoidal sensors have a strip pitch of 45 μ m and a stereo angle of 15°. They will be read out using a floating-strip scheme by bonding every second strip to the front-end electronics.

The sensors and test structures were tested extensively and characterized electrically by different means of test equipment, like probe-stations, probe-cards or special designed test fixtures. The sensor parameters were investigated at different radiation levels. Several irradiation tests were performed at the isochronous cyclotron facility in Bonn using a 14 MeV proton beam [10]. Prototype modules were assembled and tested with radioactive sources as well as test-beams at COSY, DESY and at the CERN PS and SPS. The photo on the left in figure 4 shows such a prototype module.



Figure 4: The prototype module depicted on the left, employing a square shaped double-sided silicon strip detector for the $\overline{P}ANDA$ MVD with floating-strip readout and a pitch adapter between sensor and front-end made from flex-PCB, was used in a test-beam measurement at the CERN SPS. The corresponding hit map from a measurement with a 15 GeV electron beam can be seen on the right.

To read out the approximately 200,000 channels in the strip part of the MVD, a highly integrated front-end ASIC is needed. Since PANDA will not have a central trigger, each detector needs to be self-triggering. Front-ends for silicon strip detectors used in contemporary experiments do not fulfill those requirements. Thus, the development for a new front-end chip, called PASTA, based on the requirements of $\overline{P}ANDA$ was initiated. The ASIC design is carried out at the INFN Torino in collaboration with JLU Gießen and FZ Jülich. The basic functionality was deduced from the TOFPET [11]. The TOFPET is an ASIC for the readout of silicon photomultipliers of the ENDO TOFPET US collaboration. It features a self-triggering architecture with fully digital back-end. The digitization is implemented using ToT from TDCs with analog interpolators. In this way, the time stamping of the hit can be more precise than just derived from the global PANDA timing clock, resulting in the order of 100 ps. The ToT approach was also chosen to reach the power consumption goal of 256 mW per 64 channel chip, in order to simplify the cooling system and ensure a stable sensor operation. In order to reduce the pile-up probability, multiple ToT-stages are implemented for each channel. A complete redesign of the analog input stage for the dynamic range and capacitance of silicon strip detectors was required. The submission of a first prototype in UMC 110 nm technology is foreseen for the first half of 2014.

4. Hybridization

The MVD, as the innermost detector, should exhibit small to no influence on the performance of the outer detectors. Therefore, the introduced amount of material measured in terms of radiation lengths needs to be kept small. Hence, the materials applied for the construction of detector modules need to fulfill requirements like high radiation length, high thermal conductivity and mechanical stability under high radiation levels. Accordingly, it was decided to build support structures as a sandwich structure made from carbon fibers (M55J) and a carbon foam core. For instance, the barrel staves for the strip part will be made from the same sandwich structure of an ultralight carbon fiber foam molded in carbon fiber form sheet reinforcements with a specific feature being a high thermally conducting carbon foam (POCO HTC) and an integrated cooling pipe beneath the front-end chips. The stave exhibits cutouts at the sensor positions to reduce the amount of material further without affecting the stiffness. In figure 5 a prototype and the structural design of a strip barrel stave can be seen.



Figure 5: A prototype of the support structure for the strip barrel stave. The concept of the stave can be seen in the schematic cross section on the right.

The suitable material to be employed for the hybrid carrier board is polyimide film. In this way, radiation hard, flexible printed circuit boards with low material budget can be produced. Recently, pitch-adapters based on flex-PCB were produced¹ [12]. The 2-layer design with a dielectric thickness of 25 μ m features a trace width of 35 μ m, laser drilling of 50 μ m and gold plating for bonding. By distributing the traces on two layers, it is possible to route the traces for the dense input-pitch of the front-end as small as 44 μ m. Pitch-adapters of this kind were used on the latest sensor module employed in test-beam measurements, as depicted in figure 4. By using this technology, the integration of the pitch-adapter into the hybrid carrier board can be achieved.

5. Data Acquisition

The high event rate of up to $2 \cdot 10^7$ antiproton-proton annihilations per second and the triggerless PANDA readout scheme requires a fast and effective data acquisition system (DAQ). For the strip part, a Module Data Concentrator ASIC (MDC) next to the front-end chips at the stave level is planned. The ASIC design is currently carried out at the Fachhochschule Südwestfalen. This chip will multiplex the data coming from all front-end chips of one sensor. It will decode and buffer the

¹Manufacturer: GS Swiss PCB AG

data and perform time-ordering, mapping and clustering. By employing a 2-dimensional clustering algorithm, the amount of data to be sent off the detector can be reduced. The controller will also include slow control functions for its internal parameters and for the connected front-ends. It will be connected through the E-link protocol using high speed serial links to the next stage in the DAQ chain. High speed serial links help to reduce the amount of copper lines inside the sensitive detector volume. To reduce the length of electrical data transmission lines, the utilization of fast optical data links like the GBT link (CERN) is intended. The GBT boards will sit inside the $\overline{P}ANDA$ detector near the MVD and send off the data coming from several module data concentrators via optical fibers to the counting room electronics. The MVD Multiplexer Board (MMB) [13] is the off-detector electronic based on Advanced Mezzanine Cards (AMC) for ATCA to receive the optical data from the detector. It will feature three GBT links with a net data rate of up to 3.2 Gbps and an uplink of 10 Gbps. Its FPGA can be used to perform algorithms for track finding. It will implement the $\overline{P}ANDA$ time distribution system (SODANET), which is currently under development, and uplink the data to the FPGA-based Compute Nodes of the $\overline{P}ANDA$ DAQ system. Figure 6 shows the DAQ scheme for the MVD strip detector.



Figure 6: Readout chain for the MVD strip detector part: The front-end chips connected to one sensor will be aggregated by one Module Data Concentrator chip. Up to eight MDCs are connected to a GBT board. The MVD Multiplexer Board can handle up to three optical GBT links and connects to Compute Nodes of the event selection system.

6. Detector Services

Special attention has to be given to the powering and cooling of the detector. Since a focus is on the design for low power consumption of the front-end ASICs, an active cooling of the detector is still required. Water at 16 °C will be used as cooling liquid. The cooling circuit inside the detector will operate in underpressure mode to prevent leaking in case of failure. Pipes of a nickel-cobalt

alloy with an outer diameter of 2 mm and a wall thickness of 80 µm embedded in carbon foam of the detector staves cool the front-end electronics. Tests of detector mockups with thermal loads were carried out to validate the results derived from FEM simulations.

In order to reduce the voltage drop along the supply cables for the front-ends and MDCs, a powering scheme with switching DC-DC converters close to the detector was chosen. Therefore, DC-DC converters able to operate inside the 2 T solenoid are required. Because of that, radiation hard air-coil converters developed at CERN for the upgrade of LHC exeriments will be employed [14]. Figure 7 shows the arrangement of services for the MVD along the beam-pipe inside the $\overline{P}ANDA$ detector.



Figure 7: CAD drawing of services for the MVD arranged along the beam pipe. The GBT boards are located next to the detector to reduce the length of electrical data transmission cables. The DC-DC converters are situated inside the \overline{P} ANDA detector in order to reduce the power drop along the supply lines.

7. Summary

The design and implementation of the $\overline{P}ANDA$ MVD is well advanced. The developments and tests for the pixel and strip sensors were completed and in the course of this, methods for largescale sensor qualification were developed. Sensors, front-ends and structural components were tested for radiation hardness at multiple irradiation facilities. Several successful beam tests were performed using triggerless pixel front-end prototypes together with prototype sensors along with $\overline{P}ANDA$ -sized strip detectors in a time-stamp synchronized DAQ scheme to link between the two individual systems. In the near future, the individually tested components will be brought together for a full-size detector module test to reach production readiness for the construction of the full detector.

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