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The Phase-2 Upgrade of the Silicon Strip Tracker of the ATLAS experiment

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The Large Hadron Collider (LHC) performs extremely well in operation. About 26 fb $^{-1}$ of data have been collected at a center-of-mass energy of 7 TeV in 2011 and at 8 TeV in 2012. Meanwhile, a phased upgrade of the LHC is planned and in about ten years from now the High-Luminosity LHC (HL-LHC) is foreseen. By luminosity levelling and a ten times higher LHC design luminosity the delivery of about 3000 fb $^{-1}$ is envisaged. To cope with the severe radiation dose and high particle rates, an upgrade of several detector components of the ATLAS experiment is required. The inner detector and transition radiation tracker will be replaced by an all silicon tracking detector. The report focuses on the Phase-2 upgrade of the ATLAS silicon strip detector. It gives an overview of the concept and highlight technology choices for the upgrade strip tracker. The developments towards low mass and modular double-sided structures for the barrel and forward region are discussed. The current status of prototyping, assembly procedures and mechanical and electrical results of the prototypes, so-called stavelets and petalets is presented.

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1. Introduction

In about ten years a major upgrade of the LHC to the so-called High-Luminosity-LHC (HL-LHC) is planned [1]. It is foreseen to be operated at a center-of-mass energy of 14 TeV and run with an increased instantaneous luminosity of $5\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In total an integrated luminosity of about 3000 fb $^{-1}$ is planned to be collected. This would allow to extend the mass reach for new physics and to measure Higgs boson properties.

These operating conditions result in challenges for the experiments. For the ATLAS experiment several detector components are planned to be upgraded. A major upgrade is the replacement of the inner tracker. An all silicon detector is intended to replace the current silicon pixel and strip detectors and the transition radiation tracker. Moreover, the use of a track trigger at level-1 is planned [2]. In the following requirements, expected performance and both design and prototype details are laid out for the upgrade of the silicon strip detector.

1.1 Requirements and challenges for the upgrade of the silicon strip tracking detector

The running conditions at the HL-LHC lead to several requirements and challenges for the silicon strip tracking detector. The high instantaneous luminosity of up to $5\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ requires a high triggering rate and results in large event sizes. In addition, up to 200 multiple interactions per bunch crossing are expected. The resulting high occupancy requires a huge granularity of the detector. Due to the high particle fluences, detectors in the strip tracker region have to be radiation hard to up to 2×10^{15} 1 MeV neq cm^{-2}. This leads also to a non-negligible activation of the material. To maintain a high performance of the detector, low material budget is needed and the tracking detector will have to be implemented in the existing ATLAS detector with a partial reuse of services [3]. The motivation for a new all silicon tracker is to improve, or at least maintain, the performance of the present inner detector of the ATLAS experiment at the HL-LHC.

2. The upgrade of the ATLAS silicon strip tracker

Details of the design and main components of the ATLAS silicon strip tracker will be described in the following section.

2.1 The layout

The current baseline layout is the so-called "Letter of Intent"-Layout [2]. It is shown in figure 1, which displays one quarter of the inner tracker in r-z. In the barrel region four pixel layers and three short strip layers are planned with strip lengths of about 24 mm and two strip layers with longer strips being about 48 mm long. In addition, a stub cylinder is laid out to improve the performance in the transition region between the barrel and forward tracker regions. In the forward region, the end-caps are intended to have seven strip layers with varying strip length of 8-48 mm. The outer dimensions are given by the current ATLAS detector. In the design a full coverage is achieved up to pseudorapidity $|\eta| < 2.5$ and minimal gaps occur only in the last end-cap strip layer at z=3 m. Each strip layer corresponds to several detector modules with two silicon sensors with 40 mrad stereo angle. The layout foresees hermeticity for 1 GeV/c tracks. In total the pixel detector will consist of 8.2 m^2 silicon and about 638 M channels and the strip detector of 191 m^2 with about

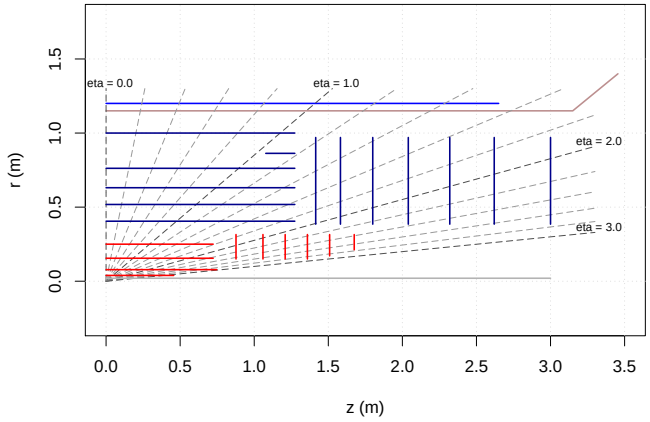


Figure 1: The baseline layout of the replacement tracker showing the active areas of silicon detectors arranged on cylinders and disks.

74 M channels. For comparison, the current silicon strip layers in the ATLAS experiment correspond to 30% in area. Because of the large amount of required silicon modules, a reduction in cost is targeted where possible.

Moreover, there are no specific trigger layers planned. However, an upgrade of the trigger scheme will be pursued. The total level-0 trigger rate will be limited to 500 kHz with a latency of 6 μs and level-1 rates have to be below 200 kHz with 20 μs latency. For maintaining low trigger rates for low p_T-lepton triggers, a so-called region-of-interest is built from muon and calorimeter information by the level-0 trigger and fed into front-end chips of the tracking detector. This allows to extract tracking information for specific regions within the level-1 latency.

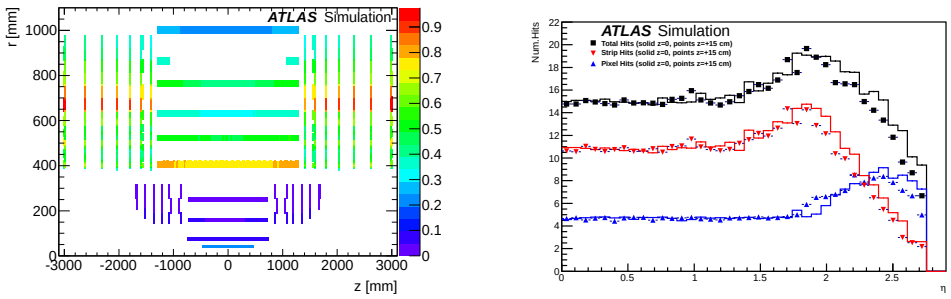
2.2 The expected performance

The expected performance of the "Letter of intent"-design was evaluated using simulation [2]. In figure 2(a) the hit occupancies with 200 pile-up events are displayed as a function of r-z, in percent. Due to the high granularity and large amount of channels hit occupancies below 1% are obtained for the strip region. An example for the tracking performance is given in figure 2(b). It shows the number of hits on muon tracks with $p_T > 5$ GeV as a function of η. More than 14 hits are expected including inefficiencies. It is also obvious that the stub cylinders contribute to a good performance in the transition region, since no reduction in number of hits is observed.

The estimated material in radiation length X_0 is planned to be below 0.7% in the central region. The reduction of material, especially routing service material outside the tracking volume, aims for less tracking inefficiencies. For comparison, the current inner detector has partially values above 1% [4].

3. Design of the barrel and end-cap region strip detectors

For the design of the barrel and end-cap region strip detectors, modularity is exploited. This will be explained in detail below and individual components, namely sensor modules and service



(a) (b)

Figure 2: In (a) channel occupancies (in percent) with 200 pile-up events. In (b) number of hits on muon tracks with $p_T > 5$ GeV as a function of pseudorapidity, η. The line shows the result for tracks originating at the centre of the detector, and the symbols for the tracks originating from z=150 mm.

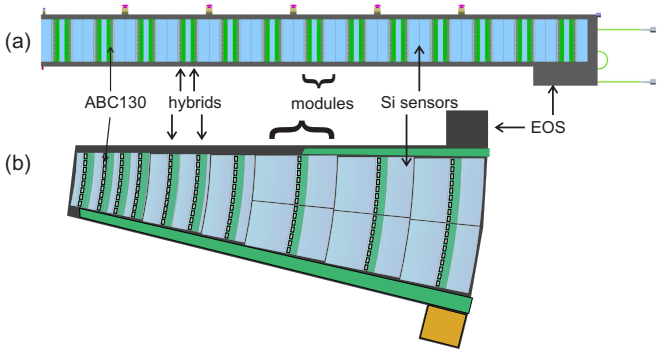


Figure 3: a) Barrel stave components, b) Petal components.

modules will be described. The aim is an easier final assembly and multiple site production and testing possibilities. Early system tests are intended as well.

3.1 Silicon detector module layout

The barrel region strip detector is planned to be built out of staves. These are structures of about 1.3 m length and double-sided assembled with silicon strip sensor modules. A schematic drawing is given in the part a) of figure 3. In the part b) of this figure, a drawing of a petal is shown, the corresponding detector unit for the end-cap region. It has a wedge-shape and a length of about 0.6 m. A stave has 13 modules per side and petals have nine modules per side of different types in six rings. As can be seen in figure 4 [5], the silicon sensor modules are glued on top of a copper bus tape, which is co-cured on carbon fibre facings, building the cores. In the middle of the rigid core run titanium coolant tubes embedded in carbon honeycomb. The staves and petals are planned to be cooled with CO_2. For communication each unit has an end of substructure card (EOS card). A photo of one stave silicon sensor module is depicted in figure 5. It shows a silicon sensor of about $10\times10\,\mathrm{cm}^2$ with two kapton flex hybrids glued on top, which reduces the amount of support material. The displayed module uses ASICs produced in 250 nm CMOS process, the

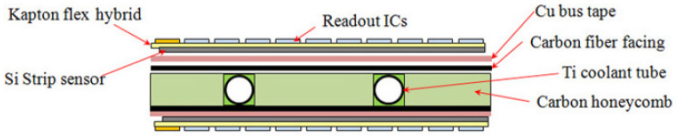


Figure 4: Cross section of a stave.

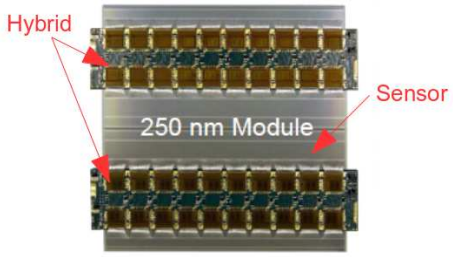


Figure 5: Silicon sensor module for the stave region with asics in 250 nm CMOS process.

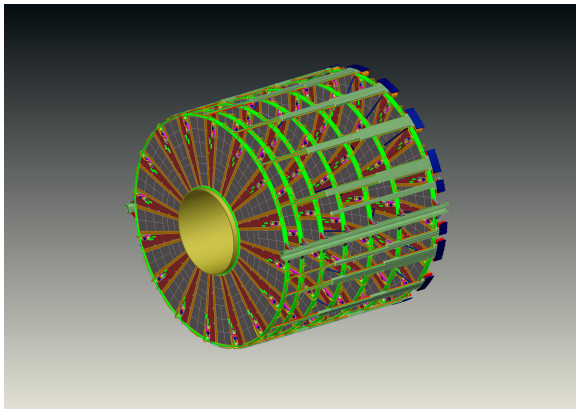


Figure 6: Drawing of one end-cap showing the carbon support structure (light green), seven disks with 32 petals (grey) each and service modules (dark green).

ABC250 [6]. It is a binary readout chip with 128 channels, which is based on the chip of the current semiconductor tracker in the ATLAS experiment. For future new ASICs are in production with 130 nm process. They are designed with 256 channels for smaller hybrids, less ASICs, respectively and lower power consumption. The sensors will be described in more detail in section 3.2.

The staves and petals will be assembled in pre-built support structures made out of carbon. They are foreseen to be end insertable including services. Exemplary one drawing of one end-cap is shown in figure 6. It layouts the seven disks with each having 32 petals, in total 446 petals per end-cap, respectively. Additionally, service modules (dark green along the carbon structure) are visible. The (in total 472) staves are tilted by ten degrees to build barrel layers in their support structure. It is planned that the staves slid into support cylinders and are locked using single edge mounting. Afterwards services can be connected. First assembly tests with mock-ups have been

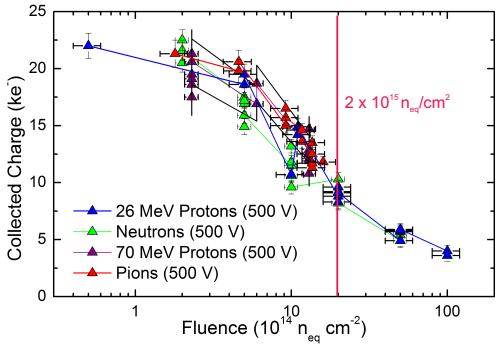


Figure 7: Collected signal charge at 500 V bias voltage for minimum ionising particles as a function of 1 MeV neq cm^{-2} fluence for various types of particles.

successfully performed [7]. In total about 13000 barrel modules and 8000 end-cap modules will be needed for the construction.

In order to reduce the time for installation, services between the EOS card and the patch panel are placed in modules. Cabling and connections for coolant and grounding are combined in these modules. First designs and mock-ups are available and under test.

3.2 Silicon sensors and electrical design

3.2.1 Silicon sensors

The baseline are AC-coupled n-in-p float-zone silicon strip sensors of about 300 μm thickness with p-stop isolation. They are advantageous with respect to their radiation hardness due to the collection of electrons and no type inversion. Studies have been conducted to test the radiation hardness of such sensors produced by Hamamatsu [8]. The result after annealing (80 min at 60 °C) is shown in figure 7. It displays the collected charge as a function of the fluence after irradiation with different particles. Highlighted by a vertical line is the dose of 2×10^{15} 1 MeV neq cm^{-2}, which corresponds to the expected fluence in the strip region after an integrated luminosity of 3000 fb^{-1}. About 10000 electrons can still be collected at the bias voltage of 500 V. Estimations of the signal-to-noise ratios lead to values above 17-26 [2]. Due to geometry, full-size sensors in the barrel region are planned with the size of 97×97 mm^2, having four rows of 1280 strips each with a pitch of 74.5 μm. The end-cap sensors are wedge-shaped with radial strips to get the r-ϕ-coordinates. Additionally, they have a range of different strip lengths. Currently, a further test and irradiation program is ongoing to investigate sensors with different p-stop isolations, ganging, different pitches, reduced size of edges and skewed geometry.

3.2.2 Electrical overview

On each hybrid is a hybrid controller chip to interface ASICs and EOS card. Low voltage and high voltage support for the modules is also obtained on each hybrid via the EOS card using a power bus. The powering is still under investigation and studies are conducted both on DC-DC and serial powering. The high voltage is foreseen to be multiplexed with powering on single line per stave with switches.

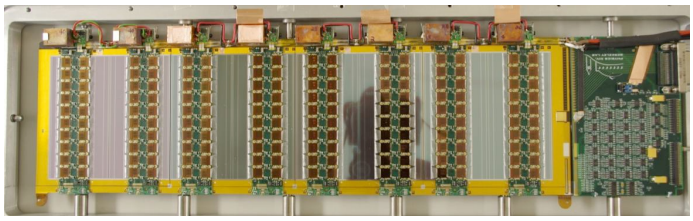


Figure 8: DC-DC powered stavelet with ABC250s.

4. Prototyping of modules and hybrids

In the following section the status and plans of the prototyping of modules and hybrids will be given both for the barrel region and for the end-cap region.

4.1 Barrel region prototyping

One prototype barrel module has already been shown in figure 5. The assembly of it is designed to allow for mass production and dedicated tooling was developed. For example, the assembly and test of hybrids is performed in panels. Modules are tested both DC-DC and serially powered. They show a similar noise behaviour and low values of around 600 electrons are measured. After irradiation an as expected increase of the noise was measured [2]. Nine production sites are currently gaining experience and in total about 70 modules have been successfully assembled. This shows that the production is well understood and the properties are controlled. The development of hybrids for the 130 nm ASIC has started and first thermo-mechanical hybrids have been produced.

The ongoing step in prototyping is the so-called stavelet program [9]. Instead of directly building full staves, smaller versions with four modules per side have been assembled. This allowed to test the construction, shielding, grounding, powering and readout on a smaller scale. A photo of one DC-DC powered stavelet is given in figure 8. Assembly tools were successfully developed and electrical tests show that the noise on a serially powered stavelet is only around 20 electrons higher compared to the noise of single modules. Additionally, thermal and noise performance in ongoing tests of a two-sided shieldless stavelet are promising. It has one side DC-DC powered and the other serially. Also the construction of both a DC-DC and a serially powered full stave is ongoing.

4.2 End-cap region prototyping

The end-cap region makes full use of the experience of the barrel region and is prototyping a petal in reduced size, the so-called petalet. It is intended to test the assembly and hybrid design and production on the innermost radius, where the smallest strip pitch occurs and the region where the petal splits into two sensor columns. A sketch of a petal is laid out in figure 9 [10]. It highlights the petalet modules in red boxes. The petalet is two-sided and will be DC-DC powered. It has a size of about $20\times17\,\mathrm{cm}^2$ and is made out of similar materials as petals. Each side is assembled with three sensors and 24 ASICs (two or three hybrids). The sensors have been successfully produced as 4 inch silicon n-in-p sensors with p-stop isolation by CNM, Barcelona [11]. Two different layouts are investigated for readout. One with two upper hybrids, one on each sensor and with data and

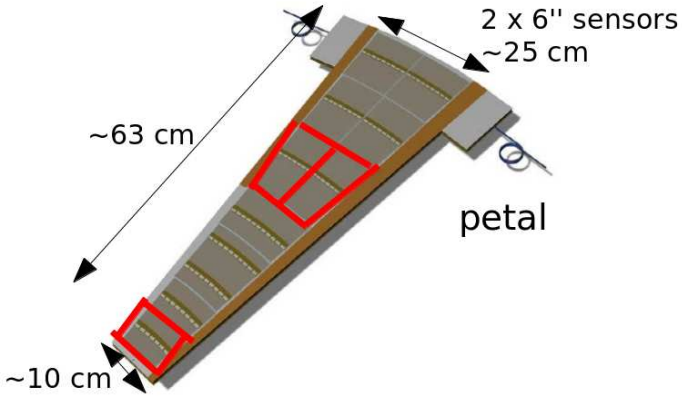
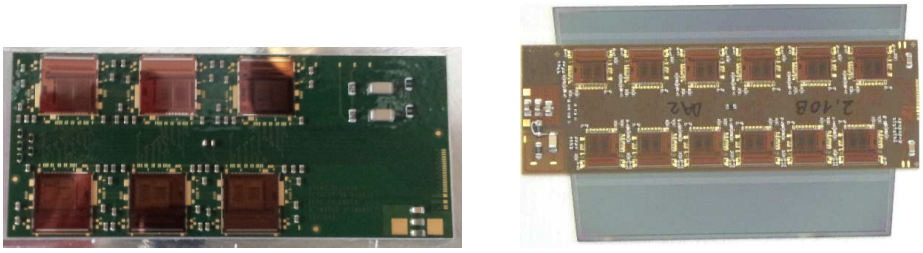


Figure 9: Schematic drawing of a petal and highlighted in red boxes the modules prototyped in the petalet.



(a) (b)

Figure 10: In (a) photo of an upper right L&F hybrid, in (b) photo of a lower Bear module.

power routing on one side (the so-called L&F), the second with a single upper hybrid bridging over both sensors and with data and power on different sides (the so-called Bear). Both layouts are studied in detail on to select one for petals. In the L&F layout both one lower and two upper hybrids have been designed. Upper left and right hybrids have also been produced. The ASIC assembly is done with a flip-chip bonder and electrical tests are being conducted. A photo of an upper right hybrid with six ABC250s is given in figure 10(a). In the Bear layout both lower and upper hybrids with each 12 ABC250s have been assembled. Specific tooling allows for constant gluing heights, when gluing chips on hybrids. The hybrids show a good performance with low mean noise of 375 electrons and long-term noise stability over more than 80 hours. In addition, lower modules have been built and a photo of a hybrid glued on a silicon sensor can be seen in figure 10(b). Successful wire-bonding and height measurements show constant glue heights of $100\pm15\,\mu$m. A thermal picture shows a linear heat distribution. The performance was also electrically tested. Figure 11 shows the successful test result of a noise measurement at 80 MHz readout. A mean noise value of about 560 electrons was obtained, when running the sensor fully depleted. A noise measurement versus bias voltage depicts the expected behaviour of reduction in noise and after full depletion a flat noise is measured. In addition, the leakage current of the sensor shows similar behaviour before and after gluing the hybrid on top. Further steps are the assembly of more modules both lower and upper and the conduction of long-term module tests. In

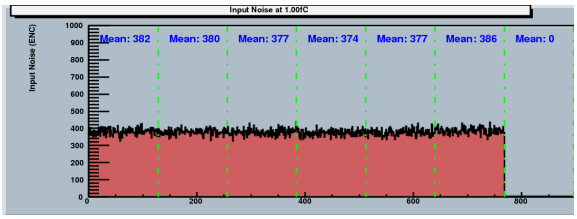


Figure 11: Noise of a lower Bear module at input charge of 1 fC in Equivalent Noise Charge (electrons) as a function of channels. The mean noise is given for each ASIC.

(a) (b)

Figure 12: In (a) photo of one petalet core, in (b) photo of a petalet bus tape.

future, module tests are planned with a beta source and in a test beam. The petalet core has been designed and first ones have been produced. It includes a bended titanium pipe, which has stainless steel fittings brazed to and is successfully tested up to 200 bar. One photo of a core is shown in figure 12(a). The bus tape, which is foreseen to be glued onto the petalet core for routing, has been laid out as a several layer flex tape. First ones have been produced. A photo is given in figure 12(b). Currently, more cores and a module assembly tool is in preparation. These will allow to build and test full petalets soon.

5. Summary

The note describes the layout, expected performance and prototyping status of a new silicon strip tracker for the ATLAS experiment at the HL-LHC. The layout is defined and five barrel and seven end-cap layers plus one stub cylinder are planned. It has a large increase of channels and area compared to the current inner tracker of the ATLAS experiment. Modularity is exploited for both staves and petals. Compared to the present silicon strip tracker a reduced mass and improved performance is expected. Currently many components are in prototyping and under test. First successful results were obtained, demonstrating that the stave module production is well controlled. Moreover, double-sided stavelets show good performance and staves are under construction. First end-cap modules were built with good performance and the first petalet is planned to be assembled soon. The design of support structure, services modules and a new ASIC are approaching maturity,

resulting in a readiness for larger scale prototypes.

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