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The Silicon Upstream Tracker for the LHCb Upgrade

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The detector for the LHCb upgrade is designed for 40 MHz readout (the maximum beam-crossing rate), allowing the experiment to collect 5 fb^{-1} per year. The upgrade of the Upstream Tracker, upstream of the magnet, is crucial for charged track reconstruction and fast trigger decisions based on a tracking algorithm involving also vertex detector information. The detector consists of 4 planes made of single sided silicon strip sensors: the two external planes are sensitive to the horizontal coordinate while the others are tilted by $\pm 5^{\circ}$. The radiation dose integrated in 10 years is estimated to be 35 MRad for the inner region; the sensor operating temperature will be -°5 to prevent sensor thermal runaway. The material budget has to be minimized, imposing severe challenges to the design of the support structure, cooling system and electronics in the active area. We will present here the conceptual design of the detector and the status of the R&D for the project.

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1. Introduction

Heavy flavor physics has a great discovery potential that in principle can extend the search for new particles beyond the energy scale of the LHC. This is possible through indirect searches for new physics, as opposite to direct searches, where new particles can be discovered by reconstructing their invariant masses. In indirect searches, the sensitivity to new physics arises from loop diagrams where new particles contribute with sizable effects to physics observables. Experimental results have to be compared with theoretically "clean" predictions, and high precision measurements are crucial for the success of this scientific program. In this respect, there are many "theory clean" measurements currently limited by the statistical uncertainty that will benefit of a much larger data sample [1].

The LHCb detector [2] is a single-arm forward spectrometer covering the pseudorapidity range $2 < \eta < 5$, designed for the study of particles containing b or c quarks. The results from LHCb, based on data collected during the LHC Run 1, have definitively proved that precision measurements in the heavy-flavour sector can be made in the extreme environment of high-energy pp collisions. The readout and trigger scheme of the current LHCb detector, however, limit the amount of luminosity that can be recorded, and therefore the precision that can be achieved. In order to overcome these limitations, it is necessary to upgrade the current detector to 40 MHz readout with a highly flexible trigger. The trigger scheme for the upgrade consists of a Low-Level Trigger (LLT), based on the information of the electromagnetic calorimeter and of the muon detector, and a High-Level Trigger (HLT), a software-based trigger running on a CPU farm that profits from the fast tracking capability of the upgraded LHCb detector. The LLT will serve as a throttle, providing the trigger bandwidth (1-40 MHz) to be adapted to the available CPU power. The output data rate of the HLT for the offline event reconstruction will be 20 kHz. The LHCb experiment, after its upgrade foreseen in 2020, will be able to integrate 50 fb^{-1} in 10 years of data taking with instantaneous luminosity of $2 \times 10^{33}\,\text{cm}^{-2}\,\text{s}^{-1}$ at regime. The data rate will be increased substantially, as well as the trigger efficiency, leading to improvements in annual signal yields, compared to those obtained in 2011, by a factor of around ten for muonic B decays and twenty or more for heavy-flavour decays to hadronic final states.

2. Overview of UT detector

The LHCb tracking system consists of the Vertex Locator (VELO), the Tracker Turicensis (TT), located in front of a 4 Tm dipole magnet, and and a combination of silicon strip detectors (Inner Tracker, IT) and straw drift chambers (Outer Tracker, OT) placed behind. The VELO is a silicon strip device positioned close to the interaction region that measures the locations of the pp interaction primary vertices and the locations of the decay vertices of long-lived particles. The TT, the OT and IT are responsible for the tracking of charged particles, and for the measurement of their momenta. For the LHCb upgrade, all the tracking detectors will be replaced: the VELO will be based on pixel sensor technology, the Upstream Tracker (UT) will replace the TT and the Scintillating Fiber Tracker (SciFi), based on scintillating plastic fibers, will replace the OT and IT detectors. The tracking system for the LHCb upgrade is sketched in Fig. 1. The UT detector upgrade main goals are: (i) enable 40 MHz readout, (ii) enable full coverage of tracks within the geometric ac-

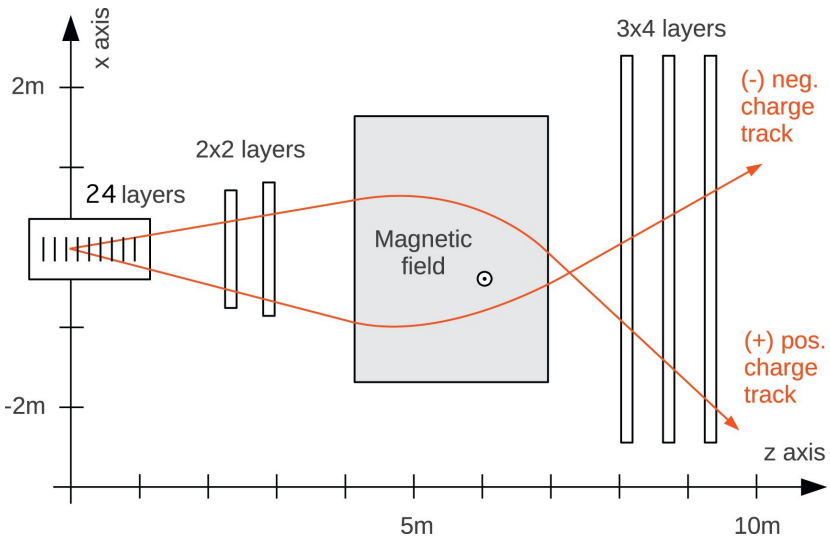

Figure 1: Schematic representation of the tracking system for the LHCb upgrade. The interaction region is inside the VELO at $z \simeq 0$, the UT is positioned before the magnet, and the SciFi is behind it. The main component of the field of the dipole magnet is parallel to the y-axis. The curved lines represent trajectories of a positively and negatively charged particle.

ceptance, (iii) increase the small angle acceptance, (iv) improve the sensor segmentation, and (v) minimize the detector material in terms of radiation length. The UT detector consists of 4 planes of single sided silicon strip sensors, positioned upstream of the magnet at about $2.27-2.70\,\mathrm{m}$ from the interaction region. The silicon layers are arranged in a $(x-u-v-x)$ configuration, where the x planes measure the x coordinate and the silicon strips runs along the y direction, while the u and the v planes are tilted of $+5^\circ$ and -5° with respect to the y direction. The spectrometer acceptance outer limit is $\pm 300\,\mathrm{mrad}$ in the bending plane (xz) and $\pm 250\,\mathrm{mrad}$ in the plane perpendicular to that (yz), while the inner limit is about $10\,\mathrm{mrad}$ determined by the beam pipe radius. The detector typical acceptance corresponds to a pseudorapidity range of $2 < \eta < 5$, which is covered with a nominal fiducial area of $1,538 \times 1,346\,\mathrm{mm}^2$ ($1,731 \times 1,346\,\mathrm{mm}^2$) for the most upstream (downstream) planes.

The silicon strip sensors are organized in a vertical column structure, the "stave", which provides the mechanical support and the cooling for the front-end electronics and the sensors, which will be operated at a temperature of -5°. The two planes closest to the interaction region consist of 16 staves and the remaining two planes are made of 18 staves. These are mounted adjacent to one another, and overlaps between the sensors ensure full coverage. The layers are mounted on a C-shaped aluminium frame outside of the spectrometer acceptance and inside a detector box, with thin windows at the front and back faces, to ensure thermal and electrical insulation. The SALT chips are bonded directly to the sensors and are positioned in the active tracking volume. A CO_2 bi-phase cooling system will provide efficient cooling with reduced impact on the material budget. Data are transferred to the periphery via thin flex cables, and separate flex cables bring the power to the sensors and the electronics.

3. UT objectives and expected performance

The LHCb detector proved to be able to cope with a larger number of visible interactions per bunch-crossing, μ, than originally planned ($\mu = 0.4$). In early 2010, due to a low number of bunches in the LHC, it was reached $\mu = 2.5$, similar to the value expected for the LHCb upgrade. However, an upgraded LHCb detector will experience larger bunch-to-bunch spillover, due to the 25 ns bunch spacing, and higher track multiplicities, given the expected increase of the LHC beam energies. Extensive studies based on Monte Carlo simulations were performed trying to reproduce the upgrade conditions, *e.g.* upgraded detector, number of primary vertices, and track multiplicity. Maximal tracking efficiency with minimal rate of fake tracks represents the challenge of the UT detector design at high luminosity and which determined its specifications.

The UT is a crucial element in track reconstruction whose main objectives are: (i) reduce ghost tracks [1], (ii) reconstruction of long-live particles decaying after the VELO, *e.g.* $K^0_S \to \pi^+\pi^-$ and $\Lambda \to p\pi^-$, (iii) provide p_T estimate for charged tracks and reject low momentum tracks for faster track reconstruction for trigger decisions (HLT). In Fig. 2, the ghost track probability is shown as a function of the transverse momentum, p_T, for charged tracks transversing all the tracking system ("long" tracks) originated from inclusive b events. The ghost track probability is significantly reduced once UT hits are required for the track reconstruction. Ghost track reduction is crucial for speeding up trigger timings and for background suppression in physics analyses. At LHCb, most of the K^0_S decay after VELO, and the UT information is especially important for their reconstruction. According to Monte Carlo simulation studies, 73% of $\bar{B}^0 \to J/\psi K^0_S$ events are reconstructed from K^0_S decays downstream of the VELO, using UT and SciFi hits only. In Table 3, the HLT timing results are shown using an emulation of the trigger system for the LHCb upgrade. The results have to be compared with the allowed timing budget for the upgraded trigger farm of about 16 ms per event, on average [2]. Using VELO and UT information only, it is possible to reconstruct track segments (VELO-UT tracks) and estimate their momenta. The average momentum resolution for VELO-UT tracks is about $\sigma(p_T)/p_T \sim 15\%$, in the p_T range [0.1-10] GeV/c. The bending power in the UT volume is limited to about 0.11 Tm. However, the momentum resolution is dominated by multiple scattering over almost the full range of particle momenta, hence the material budget has to be minimized. In order to reconstruct long tracks, a lower p_T cutoff of 400 MeV/c is applied to VELO-UT tracks, before matching them with track segments reconstructed in the SciFi. The p_T cutoff and the use of the VELO-UT momentum estimate in the track matching algorithm, reduce significantly the combinatorics and the ghost track rate. The timing and the ghost track rate increase almost by a factor 3 when the p_T cutoff and the momentum estimate is not used in the forward tracking algorithm.

4. Silicon sensors

The sensor design has to satisfy the specifications imposed by the physics requirements and to

[1] A ghost track is a fake track. For example it can be formed by matching a real track segment in the VELO (VELO seed) with a real track segment in the downstream tracker (SciFi seed).

[2] It should be noted that the execution time is machine dependent. The timing results presented here are obtained with a machine that is about 3 times faster than a 2.8 GHz Xeon.

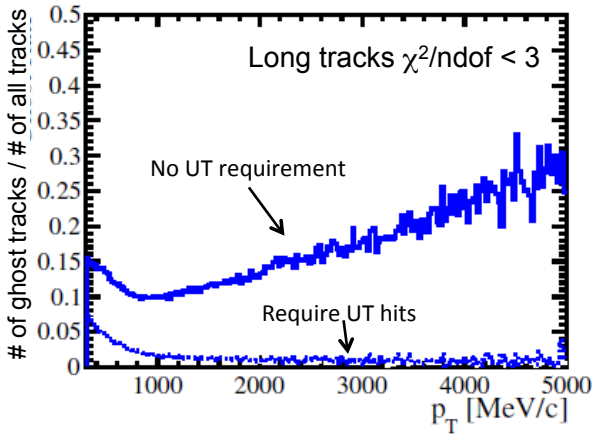

Figure 2: Probability for ghost tracks as a function of p_{T} for tracks inside the UT fiducial volume and with $\chi^2/\mathrm{ndof} > 3$. For long tracks there is ghost contribution from matching with SciFi segments, which is significantly reduced by requiring UT hits.

Tracking algorithm	Time (ms)
VELO tracking	1.9
VELO-UT tracking	1.8
Forward tracking	4.4
Total HLT2 tracking	8.1

Table 1: Timing of the HLT2 tracking sequence with instantaneous luminosity of $2 \times 10^{33}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Tracks with p_{T} above 400 MeV/c are searched for by the forward tracking algorithm.

cope with the radiation dose of about 35 MRad, expected in the innermost part of the detector with an integrated luminosity of 50 fb^{-1}. The hit density in the UT, Φ, depends strongly on the radial distance r from the interaction region, $\Phi(r) \sim 3.832 \cdot r^{-1.684}$ hits/event$\cdot\mathrm{cm}^{-2}$, and the radiation decreases by a factor of 10 at a radius greater than 15 cm. Simulation studies have demonstrated that a single-hit resolution of about 50 µm is adequate for UT. The momentum resolution of the spectrometer is then dominated by multiple scattering over almost the full range of particle momenta. Readout strip pitches of about 190 µm would meet this requirement, however a pitch of about 95 µm was chosen for the inner region to keep the maximum strip occupancy at the level of a few percent while minimizing the number of readout channels. For the same reason readout strip lengths of 97 mm, in the outer region, and of 48 mm, in the inner region, were chosen. In addition, Monte Carlo simulations have proved that having a poorer granularity in the central sensors would increase significantly the ghost rate of VELO-UT tracks . In the inner region, sensors with circular cut-out allow the beam pipe to pass through the UT while extending the detector acceptance at $\eta \sim 5$. A schematic of the sensor segmentation is shown in Fig. 3, where 4 types of sensor geometries are considered. The physics hole in the inner sensors has a radius of 33.4 mm; it includes also the space for the thermal insulation (5.0 mm) and the clearance (2.5 mm) determined by the beam pipe specifications. The thermal insulation compresses to 3.5 mm when put in place and it is

considered in the calculation. An additional radial space of 0.8 mm on the sensors is dedicated to the guard ring, hence the inner radius of the UT active area is at 34.2 mm. The sensors are 250 μm thick and are based on *n*-in-*p* technology for the inner sensors with 95 μm pitch; *p*-in-*n* technology is currently the baseline solution for the outer sensors with 190 μm pitch. The different technology choice for the outer sensors will be validated with radiation damage tests, system design and cost considerations. R&D on technology choices and prototypes for the inner sensors have been initiated with 2 different vendors, *i.e.* Hamamatsu [3] and Micron [4].

The most probable charge released in the sensors will be about 20 ke corresponding to a charge of 3.2 fC. A signal over noise ratio of about 20 is expected assuming an equivalent noise charge (ENC) of about 1000 e in the SALT chip and 10 pF input capacitance to the charge sensitive preamplifier. The bulk generated current in radiation damaged sensors is the main source of the reverse bias current, I_R, which increases power consumption and introduces noise; it strongly dependent on temperature T,

$$I_R(T) \propto T^2 e^{-E/2k_BT} \tag{4.1}$$

where $E \sim E_g = 1.2\,\text{eV}$ and k_B is the Boltzmann constant. In order to prevent thermal runaway of the silicon sensors in presence of radiation damage, they will be operated at a temperature of -°5.

5. Front-end electronics

The SALT chip [3, 4] provides zero-suppressed digital signal with 6 bit ADC resolution and operates for both signal polarities. It is a 128 channel ASICS based on CMOS IBM 130 nm technology, which ensures good radiation hardness up to about 50 MRad. It features a charge-sensitive preamplifier, a shaper, a 6-bit ADC, a DSP block for zero suppression and data compression, and a data serializer. The chip is positioned in the tracking volume, close to the sensor and bonded directly to it, in order to minimize the input capacitance to the charge-sensitive preamplifier while improving the S/N. The shaper peaking time is about 25 ns, with a fast baseline restore to limit the spillover signals, in the next beam-crossing 25 ns later, to a maximum of 5% of the signal. Particular attention in the design is devoted to the minimization of the power consumption, to be below 6 mW/channel, *i.e.* 0.77 W/chip. The first SALT chip prototype with 8 channels, featuring preamplifier and shaper and 2 channels of Single-to-Differential converter, has been designed and tested. Preliminary results are encouraging and within the specifications in terms of power consumption, fast baseline restore and noise. The prototype ASICS have been tested with negative and positive pulses and the gain of the preamplifier has been measured to be about 30 mV/fC in both cases using an input capacitance of 10 pF. When varying the input capacitance, the shaper peaking time changes from 23.5 ns at 0 pF to 29 ns at 50 pF, while the preamplifier gain changes from 36 mV/fC at 0 pF to 18 mV/fC at 50 pF. The measurement of the ENC is about 1000 e at 10 pF and the ENC slope in the range 10-40 pF is about 57 e/pF. The next ASIC submission is scheduled in February 2014, where several issues coming from measurements of present prototypes will be addressed. A prototype ASICS with 8 channels of 6-bit successive approximation register (SAR) ADC, a multiplexing and serialization circuitry, a phase-locked loop (PLL) block [5] and a scalable

[3] Hamamatsu Photonics K.K., Japan.
[4] Micron Semiconductor Ltd, UK.

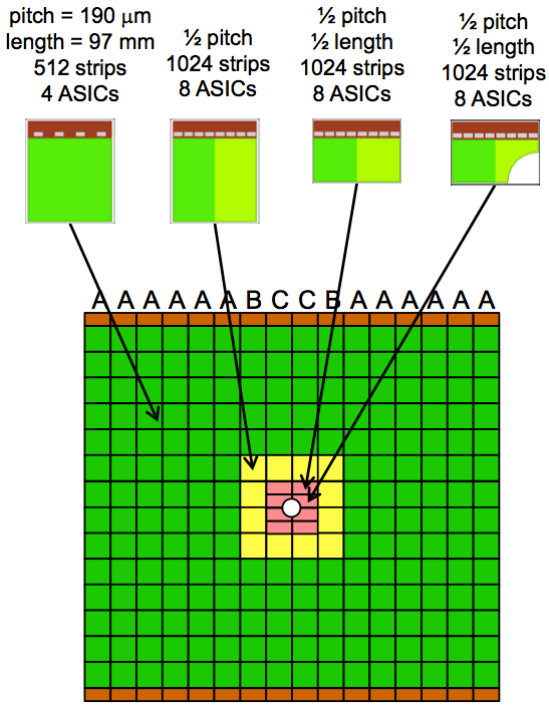

Figure 3: A schematic of the UT sensor segmentation. A strip pitch of about 190 μm and strip length of about 97 mm are used in the outer region, a strip pitch of about 95 μm and strip length of about 97 mm for the intermediate region, and sensors with a strip pitch of about 95 μm and strip length of about 48 mm are used in the inner region.

low-voltage signalling (SLVS) input/output circuitry was fabricated and tested. First measurements are encouraging and showed that the ADC is working very well: good linearity at 50 MHz sampling frequency (working fine also at 80 MHz), low power consumption, and effective number of bits between 5.7 and 5.9. The first results on the PLL and the SLVS blocks verified their functionality to be consistent with the specifications.

Hybrid flex circuits host the SALT chip and provide good thermal bridge for cooling and interconnections to low mass flex cables, based on kapton, with copper lines for data and power signals. Data lines will be connected to the GBT [6] boards providing transition from electrical to optical signals.

6. Mechanics and cooling

The mechanical requirements and design goals of UT [7] are summarized below. The UT conceptual design consists of 4 planes ($x-u-v-x$) of single sided silicon strip detectors, tiled around the beam pipe and covering the acceptance, corresponding to the pseudorapidity range $2 < \eta < 5$ in the bending plane (xz). The silicon sensors are arranged in vertical staves that are mounted adjacent to one another. Sensors overlap in x is obtained by staggering the z position of adjacent staves.

The stave has a modular structure whose elementary unit is the "hybrid", represented in Fig. 4 (left plot). It consists of the sensor, the support structure, the ASICS, the hybrid flex circuits and the low mass flex cables for data and power signals. The sensors are tiled on both sides of the stave, as shown in Fig. 4 (right plot), allowing for the overlap in y. The design is inspired by the ATLAS IBL stave [8], with carbon fiber reinforced plastic (CFRP) facings, providing structural support, which are glued with epoxy to a carbon foam interior. The stave is a closed structure which

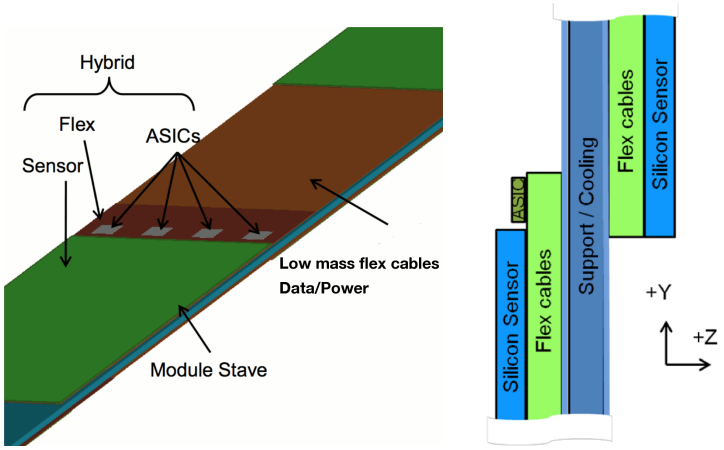

Figure 4: Left plot: sketch of the UT hybrid elementary module composed by the sensor, the support structure, the ASICS, the hybrid flex, and the low mass flex cables for data and power signals. Right plot: side view of the UT stave. The sensor and the front-end electronics alternates on both sides of the stave providing sensor overlap in the y direction.

provides stiffness and the facings are separated using lightweight foam. The metal cooling tubes are embedded in the interior of the structure, as shown in Fig. 5, and the carbon foam provides good heat transfer. The tubes are thin, 2.2 mm outer diameter and 0.1 mm wall thickness, and are made of Titanium alloy. The cooling system has to maintain the temperature of the sensors at -5°C by removing the heat generated in the ASICS, conservatively assumed to be 0.77 W/chip, and in the silicon sensors due to self-heating. The power consumption of UT has been estimated to be about 800 W/plane for a total of 3.2 kW. A dedicated simulation study, based on finite element analysis, has proved that evaporative CO_2 cooling is the optimal choice in terms of cooling efficiency and material budget. A "snake pipe" design with bent tubes passing underneath the ASICS, see Fig. 5, is currently considered as the baseline solution providing maximal heat transfer. However, several issues have still to be assessed, *e.g.* the tube bending radius, the thermal contractions and the mechanical deformations of the stave. A solution with two parallel tubes combined with heat spreaders and thermal vias is considered as a valid alternative and is also under study. The material budget of each plane is about 1.02 % X_0 according to the current stave design, where the sensor contributes for about 0.27 % X_0. The distribution of the radiation length, as a function of the pseudorapidity η, is reported in Fig. 6.

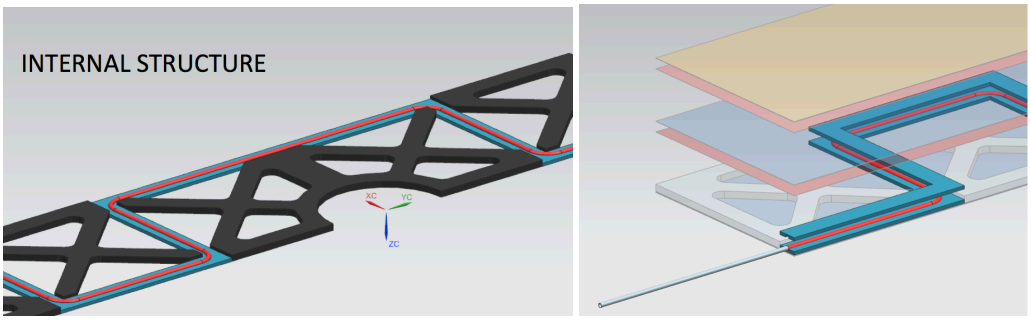

Figure 5: Left plot: the internal structure of the UT stave consists of the lightweight foam used for separating the CFRP facings and the carbon foam with the cooling tubes inside. Right plot: the titanium cooling pipes are embedded in the carbon foam and pass underneath the SALT chips for maximal heat transfer. The chips are positioned horizontally at the end of each hybrid module and a bent pipe ("snake pipe") provides maximal overlap.

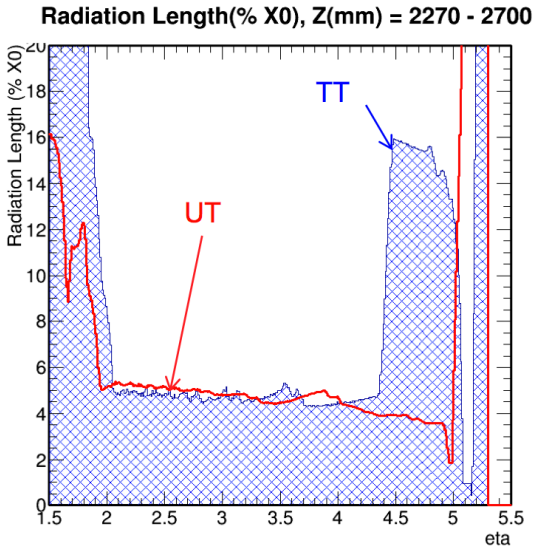

Figure 6: Radiation length (% X_0) as a function of the pseudorapidity η, between $z = 2270 - 2700$ mm, for the UT design and the current TT detector. The calculation includes 0.14% X_0 of air and 0.34% X_0 for the detector box. Each plane contributes with 1.02% X_0 to the total material budget. The reduction of material at $\eta = 4.3 - 5.0$ is due to a new design of the beam pipe jacket based on aereogel and kapton.

7. Conclusions

We have discussed the conceptual design for the UT detector and its main objectives. UT is crucial detector for charged particle tracking and trigger decisions in the LHCb upgrade. It will be able to significantly reduce ghost tracks and provide useful information for the momentum measurement with about 15% precision in the p_T range [0.1-10] GeV/c. In addition, an important speed up of trigger timings using VELO-UT momentum estimate (almost a factor 3) will be achievable.

We are developing a complex and novel front end electronics device (SALT ASIC), and low mass high signal density cables to bring the electronics signal to the detector edge. The UT design features a 40 MHz readout, an optimized segmentation of the sensors, a reduced material budget in the inner region of the detector due to a new beam pipe jacket design, and increased acceptance using circular cut-out sensors close to the beam pipe. The mechanics and the cooling are a challenge: the current design is inspired by the ATLAS IBL stave, with embedded CO_2 evaporative cooling. The R&D will continue until the Spring 2015 and we aim to be ready for installation in 2019.

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