PROCEEDINGS OF SCIENCE

Progress on Silicon-on-Insulator Monolithic Pixel Process

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A Silicon-On-Insulator (SOI) pixel process for monolithic radiation detectors is developed based on a 200 nm SOI FD-CMOS technology. The SOI detector includes both thick sensing region and CMOS circuits in a single die. Difficulties to combine both high-voltage sensors and low-voltage readout circuits in a very short distance are solved by introducing new techniques of buried-well and nested-well structure. In addition, newly introduced double-SOI wafer has shown promising results especially in the characteristics of radiation hardness.
To achieve thick sensing region, high-resistivity FZ-SOI wafer is introduced and successfully processed. Furthermore, to fulfill many requirements in actual experiments, new techniques such as stitching exposure, backside thinning, 3D vertical integration are being developed.
To perform these tasks, we have been operating Multi Project Wafer (MPW) runs periodically. Many users are submitting to the MPW run, and many kinds of detector developments are being done.
Present status of the process development is described and a few examples of the SOI detectors are shown.

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1. Introduction

In making a high-performance radiation image detector, it is a natural requirement to combine both sensors and readout circuits in a single die. A Silicon-On-Insulator (SOI) technology has been one of the promising technologies to realize such a requirement since it contains two active Si layers in a wafer. There were several pioneering works to develop SOI pixel detectors [1, 2], but their process technologies were not enough to solve all the difficulties inherent in the SOI pixel detectors. We have started SOI pixel R&D (called SOIPIX) in collaboration with Lapis Semiconductor Co. Ltd [3] which is a first supplier of the mass-produced SOI LSI in the world. The SOIPIX development was started as a generic R&D in the KEK detector development project [4] and targeting for not only high-energy physics experiments, but also X-ray, medical, and many other applications.

Figure 1 shows the schematic view of the SOIPIX detector. The SOI wafer is composed of a thick, high-resistive substrate (sensor part) and a thin low-resistive Si layer (CMOS circuitry) sandwiching a buried oxide (BOX) layer of 200 nm. Dopants of p and n type is implanted to the substrate and contacts/vias between the sensing nodes and top circuits are formed through the BOX. Recently we have also developed a double-SOI wafer process where additional middle Si layer is added (described in section 4) to extend the validity of the SOIPIX.

The main advantages of the SOIPIX are;

- There is no mechanical bump bonding, so obstacles, which will cause multiple scattering, are eliminated and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10fF), so large conversion gain and low noise operation are possible.
- Full CMOS circuitry can be implemented in the pixel.
- Cross section of single event effects caused by radiation is very small. A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.

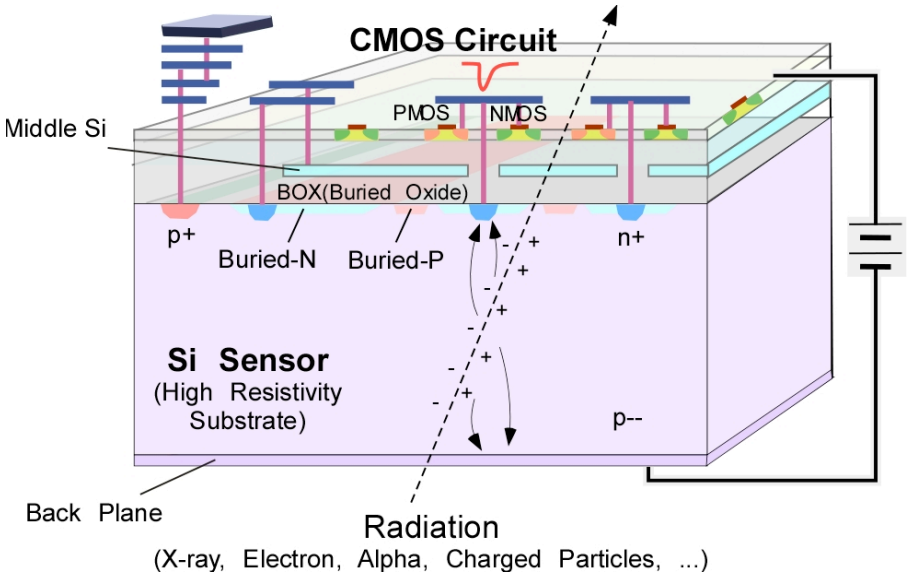

Figure 1. Schematic view of the SOI Pixel Detector using a double SOI wafer. In single SOI wafer case, there is no middle Si layer.

- Unlike conventional CMOS process, there is no leakage path to bulk. Thus SOI transistors are known to work over a very large temperature range from 4K to 600K. Especially, we have demonstrated SOI transistor operation at lower than 1K [5].
- The technology is based on industry process, so we can get high quality products. The SOI technology is one of the most promising technologies for future LSIs. Thus further progress and lower cost are foreseeable.
- Emerging vertical (3D) integration techniques are a natural extension of the SOI technology, so a much higher integration density is possible.

It is important to have many chances to submit test chips and Test Element Group (TEG) for the success of this kind of R&D. Therefore, we have started to operate Multi Project Wafer (MPW) runs of this process periodically (~twice/year) and opened the process to many other researchers.

To achieve thick sensing region, high-resistivity FZ-SOI wafer is introduced and successfully processed. Furthermore, to fulfill many requirements in actual experiments, new techniques such as stitching exposure, backside thinning, and 3D vertical integration [6] are being developed.

2. SOI Pixel Process

2.1 Wafer Process

The process is developed based on a 0.2μm Fully-Depleted SOI CMOS process. Main specifications of the process are summarized in

Table 1. We have been trying to use several kinds of high-resistive wafers (CZ and FZ) of both n- and p-type in sensor part (see section 2.3).

Table 1. SOI pixel process specifications.

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS, 1 Poly, 5 Metal layers, MIM capacitor (1.5 fF/μm2), DMOS option. Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si: Cz, ~18 Ωcm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: 720 μm thick. Cz(n) ~ 700 Ωcm, FZ(n) ~ 7kΩcm, FZ(p) ~ 25 kΩcm, etc.
Backside	Thinned to 50 ~ 500 μm by mechanical grind, and chemical etching. Then adequate impurity is implanted, laser annealed, and Al is plated (~200 nm).
Transistors	Normal and low threshold transistors for Core and I/O circuits. Three types of structures (body-floating, source-tie and body-tie)
Optional process	Stitching. Vertical integration with μ-bumps.

2.2 Sensor Structure & Back Gate Effect

One of the main difficulties to build the radiation sensor using the SOI wafer is a back-gate effect. Since the sensor and the transistors are located very near (~200 nm), transistors become ON when high voltage is applied to the sensor (Figure 3-(a)). To shield the electric field

coming from the sensing region to the transistor location, we developed Buried Well (BW) process. We implant p (n)-type dopant without removing the top Si layer to create a buried p (n)-well region (BPW (BNW)) under the BOX (Figure 2). Thus the transistor characteristics are not affected from the sensor voltage by introducing the BW layer.

Other Shielding method we have developed is a nested well structure in which BNW layer is formed within deeper BPW structure. The BNW layer is connected to a fixed voltage to shield transistors from the bottom. The nested well structure also reduces cross talk between the sensors and circuits.

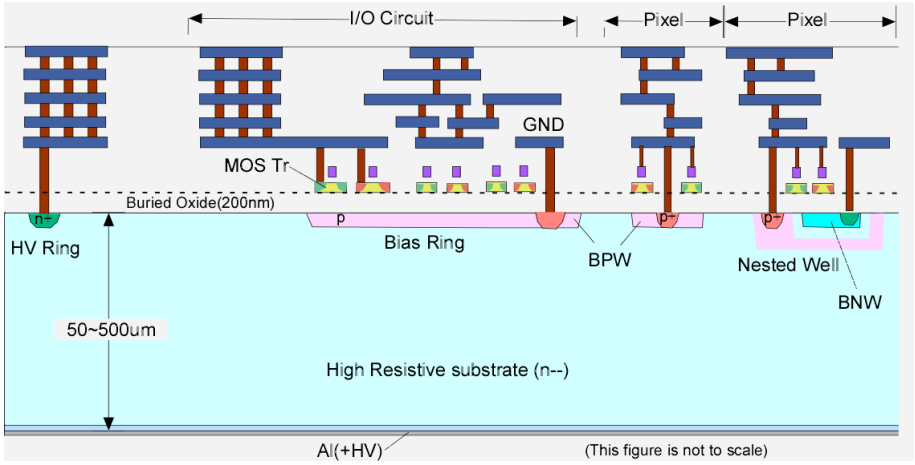

Figure 2. Cross sectional view of a typical SOI pixel detector (n-substrate case). Simple p+ sensing node with the BPW and nested well structure are depicted.

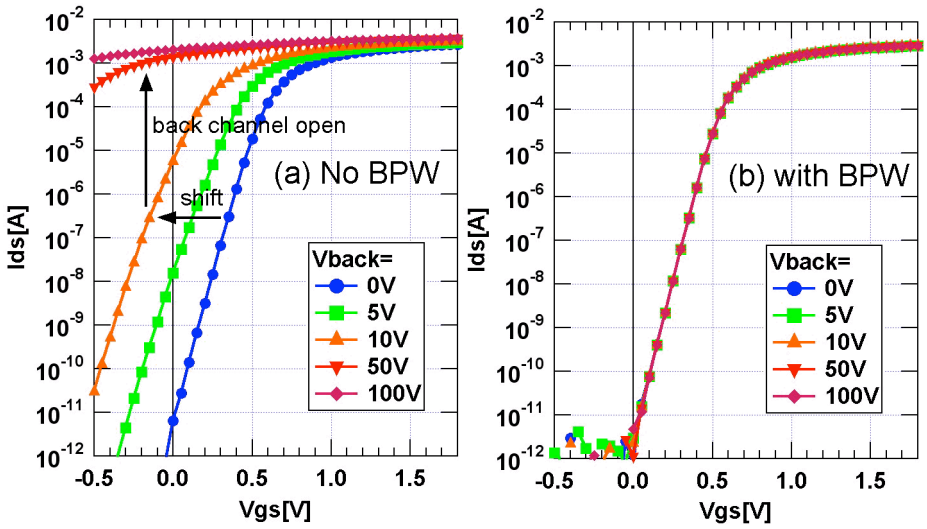

Figure 3. NMOS transistor Ids-Vds curve and back-side voltage dependence. (a) Without BPW layer. Transistor off current will increase by applying the detector voltage (Vback). (b) With BPW layer connected to ground. By introducing the BPW layer, the back-gate effect is fully suppressed.

As for the backside of the wafer, following processes are done normally; i) Mechanical grind to desired thickness, ii) Wet etching by 40μm, iii) Implant of n (p) dopant to n (p)-

substrate (depth ~ 0.5μm), iv) Aluminum plating (~200 nm). Applications which require thin dead layer such as low-energy X-ray applications will use different back-side processing.

2.3 High Resistive Wafer

We have been mainly using high-resistive SOI wafer from standard products of SOITEC Co. The handle wafer is made in Czochralski (Cz) method (called HR1 wafer), which is n-type and has about 700 Ωcm resistivity. However, it is desirable to get much higher resistivity to create thicker depletion depth with lower voltage, so we have made special SOI wafers by using high-resistive Floating Zone (FZ) wafers.

To do CMOS processing on a FZ-SOI wafer was not easy task since it includes high temperature processes and these will cause slips in the wafer. After careful tuning of the high temperature process, we succeeded to process FZ-SOI wafer without major slips.

Figure 4 shows sensor capacitance vs. detector voltage for FZ and CZ wafers. A thick FZ wafer (500 μm) becomes full depleted at 150 V, while thin CZ wafer (200 μm) needs 200V for full depletion.

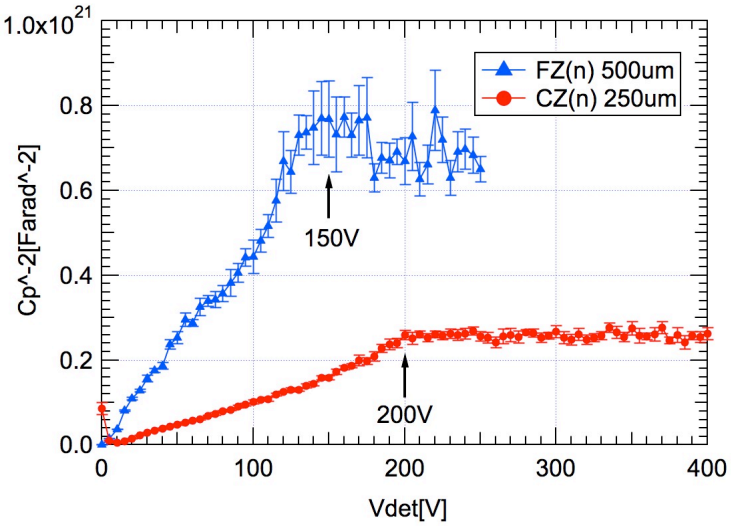

Figure 4. $1/C^2$ plot of SOI detectors capacitance versus detector voltage (Vdet). Calculated resistivity from the corner voltage is 6.0 kΩcm and 1.1 kΩcm for FZ(n) and Cz(n) wafers respectively.

2.4 Leakage current

Low leak current of the sensor is important especially for long integration time applications such as astronomical X-ray observation and measurements that require good energy resolution.

Figure 5-left shows the leakage current measurement of a SOI detector (XRPIX2b) [7] which use the HR1 wafer. Arrhenius Plot of the leakage current (Figure 5-right) implies main source of the leakage current is coming from generation current. It should be noted that the leakage current and the resistivity will change depending on wafer manufactures, lots, and cutting location in the Si ingot.

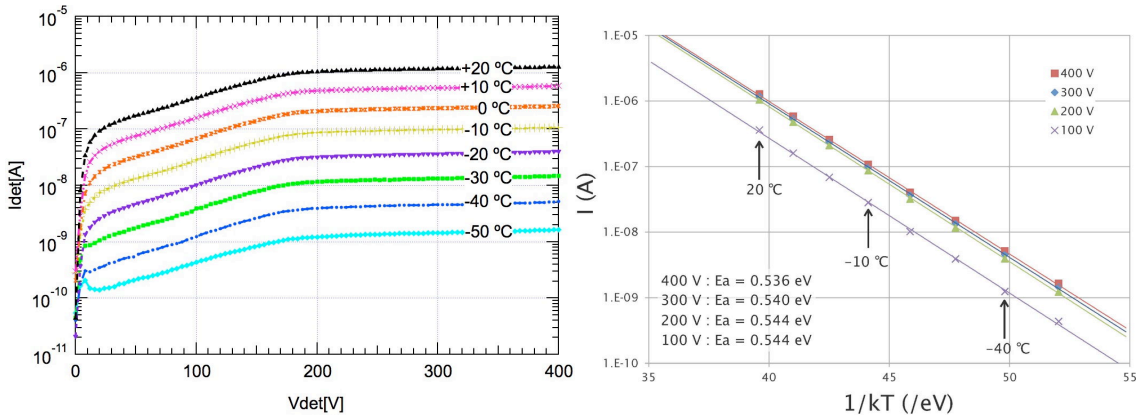

Figure 5. Leakage current of the XRPIX2b detector (left) and Arrhenius plot (right).

2.5 Stitching

Large area detectors are often required in many experiments, while the mask size is limited to 24.6mm x 30.8mm in size. Therefore, we have developed stitching technique to make a larger format detector by using a reticle set. Figure 6 shows the photographs of the stitched wafer. Each reticle contains both edge and central portions of the layout. Edge portion is masked during the central portion is exposed, and the central portion is masked when the edge portion is used. The central portion exposition is repeated multiple times.

This development is mainly driven by the RIKEN group for the SOPHIAS detector [8]. The SOPHIAS detector is being developed for the experiments in SACRA XFEL beam line. Accuracy of the two shot was better than 0.025μm. Although we are taking a buffer region of 10 μm now, we can shrink this if necessary.

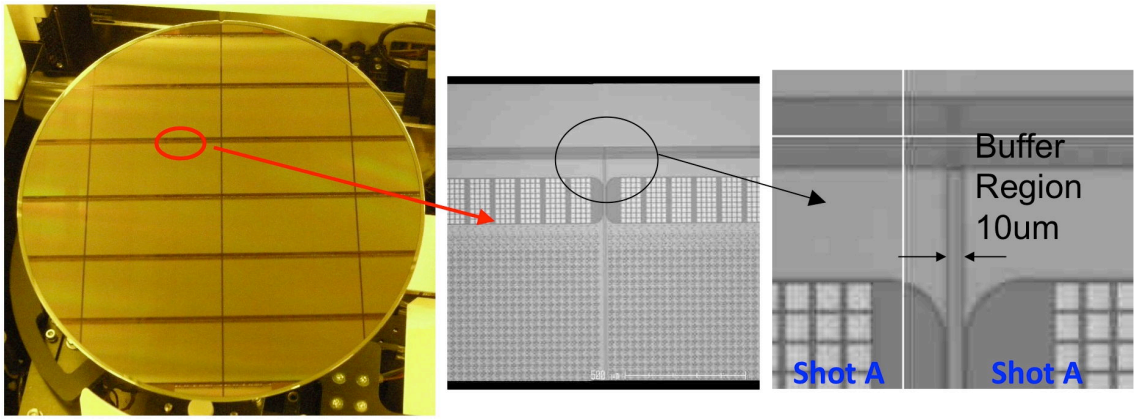

Figure 6. Stitching exposure for the SOPHIAS detector. Both edge structure and pixel structure were drawn in a reticle. Part of the mask is blocked during exposure. In this detector (SOPHIAS), pixel layout was repeated 3 times and edge structures are exposed at both ends.

3. Detector Developments

There are many activities in detector developments using the SOI pixel process. In this section, some of the detector developments are shortly introduced.

3.1 Integration Type Pixel Detector (INTPIX)

Main SOI detectors developed so far are integration-type pixel detectors (Table 2) [9]. The circuit is similar to that of the CMOS optical imager. Smallest size of the pixel we have developed is 8 μm square. Many of the integration-type pixels have correlated double sampling (CDS) circuit in each pixel or in column location. Largest chip (INTPIX5) so far has 896 x 1408 (~1.3 M) pixels. A photograph of the INTPIX4 detector and an example of X-ray image taken by the detector is shown in Figure 7.

Table 2. Specification of major integration-type pixel detectors.

	DIPIX1/2	FPIX1	INTPIX4	INTPIX5
Pixel Size [μm]	14 x 14	8 x 8	17 x 17	12 x 12
Chip Size [mm]	5 x 5	6 x 6	10.2 x 15.4	12.2 x 18.4
BPW width [μm]	10	6	12	9
CDS	Pixel CDS	-	Pixel CDS	Column CDS
Store Switch	O	-	O	O
Wafer	n or p	n and p	n	n and p (INT5) n or p (INT6N or P)
Gain	Fix (9.3 μV/e-)	Fix (~28 μV/e-)	Fix (12.6 μV/e-)	2 gain (~16 or 2.5 μV/e-)
Max. Charge	~110 ke-	~40 ke-	80 ke-	~70 or 460 ke-
No. of Pixels	256 x 128 x 2 (~65 kpix)	512 x 512 (~260 kpix)	512 x 832 (~430 kpix)	896 x 1408 (~1,260 kpix)
No. of Output	1	1 or 9	1 or 13	1 or 11
Rolling Shutter	-	O	-	O

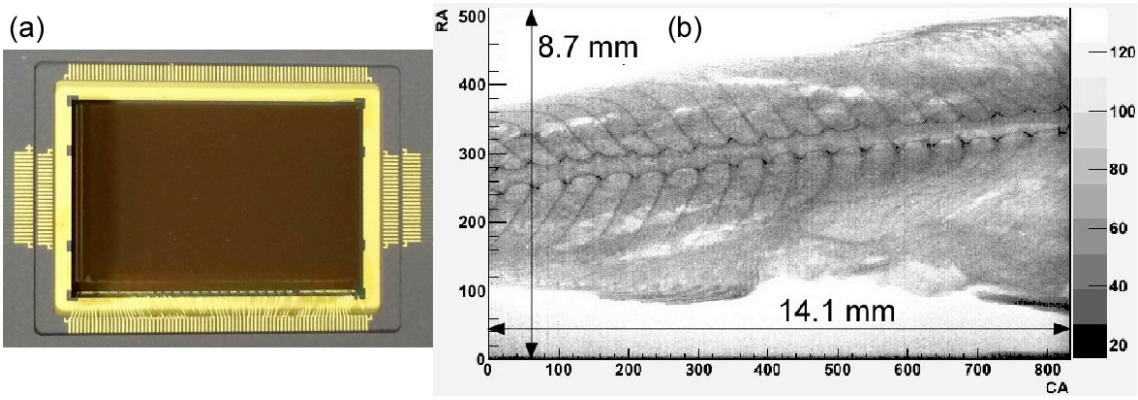

Figure 7. Photograph of the INTPIX4 detector and an example of X-ray image (small fish) taken by the detector.

3.2 X-ray Detector for Astrophysics (XRPIX)

The XRPIX detector [10] has been developed to used in X-ray astronomical satellite by Kyoto Univ. and KEK group. The basic structure of the detector is same as that of the integration type detector, but it also has a trigger generation function (Figure 8-left) within the pixel. By using the trigger function and taking anti-coincidence with surrounding active shield system, background event caused by charged particles can be removed.

In addition to source-follower type pixel same as the INTPIX, Charge Sensitive Amplifier (CSA) type pixel detector is developed recently. Figure 8-right shows energy spectrum of ^{55}Fe X-rays taken by the XRPIX-CSA sensor. CSA type pixel shows higher gain and much better

resolution compared to source follower type, and achieved noise level of 33 e- while source follower type has 76 e- noise level at -50 °C.

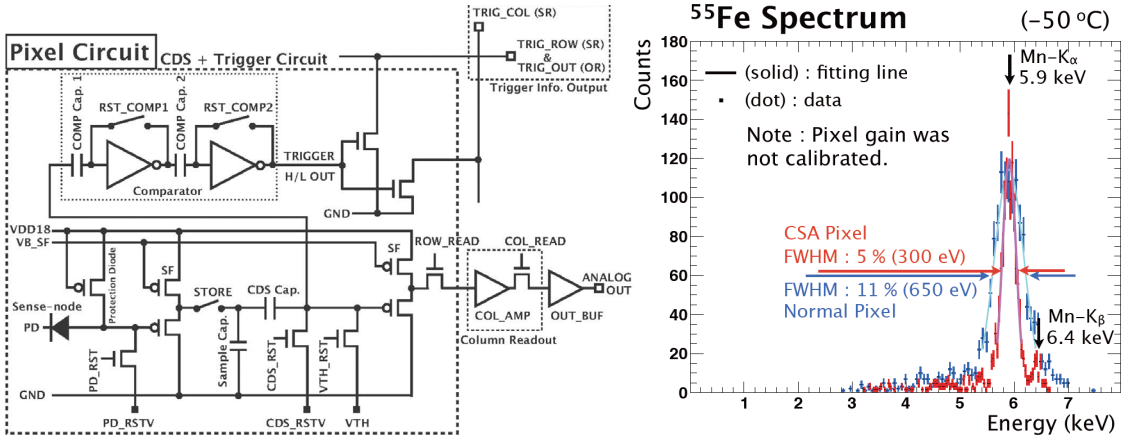

Figure 8. (left) Block diagram of the XRPIX detector. (right) Energy spectrum of 55Fe taken with the XRPIX detectors. CSA type pixel showed better resolution than normal pixel (source follower type).

3.3 Vertex Detector (PIXOR)

As an R&D for future vertex detectors such as Belle II experiment, a new detector called PIXOR (PIXel OR) is being developed by Tohoku Univ. and KEK group [11]. An analog signal from each pixel sensor is divided into two-dimensional directions, and the signals are ORed in a small N-by-N pixel matrix (now we are using 16 as N). Then the ORed signals are processed by a readout circuit in each small matrix and wait for a trigger (Figure 9).

This PIXOR scheme reduces the number of readout channels from N^2 to 2N. This scheme avoids a deterioration of intrinsic position resolution due to large circuit area and reduce number of readout channels. Thus the PIXOR detector is most appropriate between pixel detectors and strip detectors location.

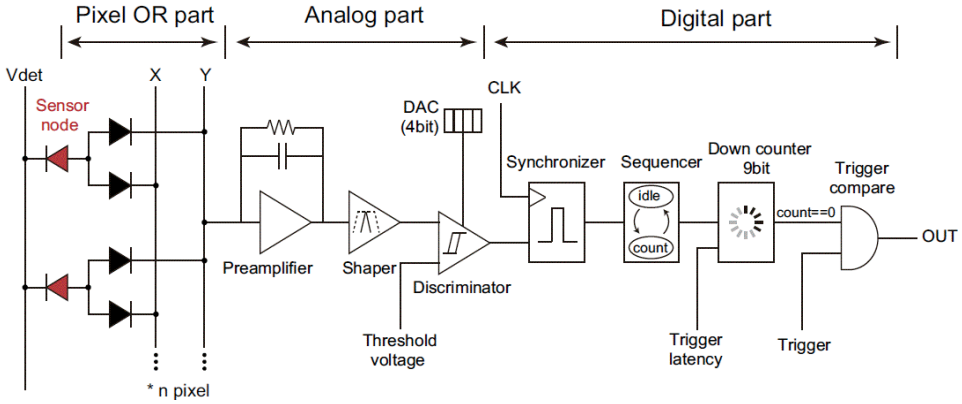

Figure 9. A block diagram of the single channel PIXOR circuit.

4. Double SOI wafer

While we solved the back-gate effect by introducing a BPW layer, there still remain two issues to make the SOIPIX usable in wide application; (a) Crosstalk between sensor node and circuit, (b) Radiation tolerance of the detector.

The crosstalk issue is severe in the case of intelligent pixel which contains many digital circuits. Radiation tolerance of the detector will limit the application field. While the SOI is immune to Single Event Effect (SEE), it is not so rad-hard to Total Ionization Dose (TID) due to the BOX and the surrounding oxide. The tolerable radiation level of the present SOIPIX devices is around 2 kGy.

To solve these issues, we added another Si layer between sensor and circuit layer in the SOI wafer (called DSOI: Double SOI). A cross section of the processed double SOI wafer is shown in Figure 10. In addition to above issues, the newly introduced middle Si layer (SOI2) shields back-gate effect too, so that we can optimize the size of the BPW without considering the back-gate effect.

The first DSOI wafers were produced by SOITEC Co. with n-substrate, and second DSOI wafers were produced by Shin-Etsu Chemical Co. Ltd, Japan, with p-type substrate.

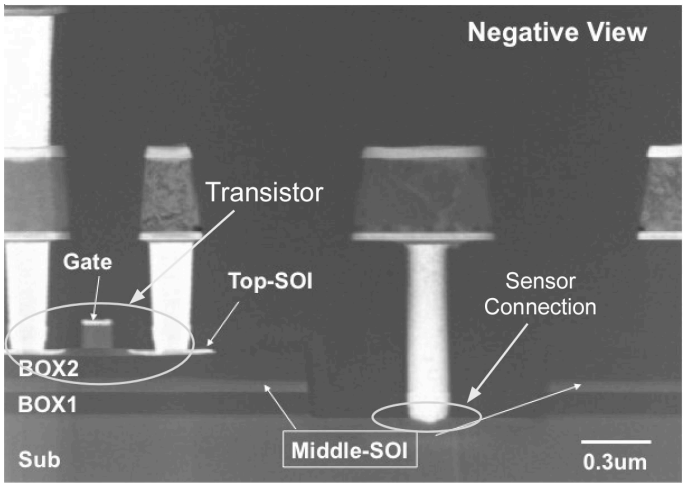

Figure 10. Cross sectional view of the double SOI wafer. In addition to top SOI and substrate, middle SOI layer is introduced. The thickness of the middle SOI is about 80 nm.

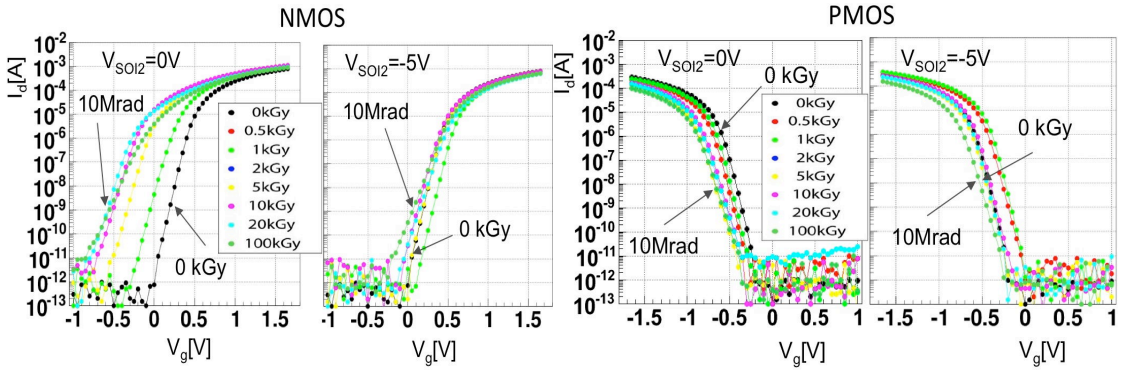

Figure 11. Id-Vgs curve variation with γ-ray irradiation and middle Si voltage (VSOI2). (Top) NMOS, (Bottom) PMOS.

When we irradiate SOI with γ-rays, transistor threshold voltage will shift to negative direction (Figure 11) due to hole trapping in the oxide. However, by applying negative voltage to the middle Si layer, electric field generated by the hole is compensated and the threshold voltage will return to almost original value [12].

5. Summary

We have developed a SOI pixel process based on a 200 nm FD-SOI CMOS process. Many issues in realizing the SOI pixel detectors are solved by introducing new techniques such as buried-well, nested-well structure and the double-SOI wafer. Especially the double SOI wafer is promising to realize radiation tolerant high performance pixel detector.

To achieve thick sensing region, high-resistive FZ-SOI wafer is introduced and successfully processed. Furthermore, to fulfill many requirements in actual experiments, new techniques such as stitching exposure, backside thinning, 3D vertical integration are being developed.

We have been operating Multi Project Wafer (MPW) runs periodically, and the process is open to researchers.

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