PROCEEDINGS OF SCIENCE

Progress in the development of the vertex detector with fine pixel CCD at the ILC

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We are developing a vertex detector with a 5 x 5 μm^2 fine pixel CCD (FPCCD) for the international linear collider (ILC). The ILC physics programme imposes several design requirements, such as high granularity and low occupancy. The FPCCD also imposes several requirements in the readout ASIC, mainly, fast readout speed, low noise and low power consumption.

We present the status of the R&D to achieve those design requirements.

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1. Introduction

The detailed understanding of the Electroweak Symmetry breaking is one of the most important goals within the ILC physics programme. This mechanism is reflected in the Higgs boson couplings.

The measurement of these couplings requires accurate particle identification; in particular, excellent separation between b-quarks and c-quarks, and between light quarks and gluon are crucial. In order to realize ILC's highly efficient flavor tagging, we need a vertex detector with an impact parameter resolution of $5\,\mu m \oplus 10\,\mu m/(p\beta sin^{3/2}(\theta))$ and a low level of pixel occupancy for accurate track reconstruction. Currently three sensor technology options are being actively developed for the ILD [1] vertex detector. Those technological options are CMOS Pixel Sensors (CPS), Depleted Field Effect Transistor (DEPFET) sensors and FPCCD sensors.

Here we cover the FPCCD sensors. Section 2 introduces the FPCCD detector. Section 3 presents the status of the R&D. Section 4 summarizes the conclusions.

2. FPCCD Detector

Baseline Design Vertex Detector

In order to reach the desired performance level, the ILD vertex detector should comply with the following specifications:

- A spatial resolution near the IP better than 3 μm.
- A material budget below 0.15% X_0 /layer.
- A first layer located at a radius of $\approx$ 1.6 cm.
- A pixel occupancy not exceeding a few percent.

The power consumption should be low enough to minimize the material budget of the cooling system inside the detector sensitive volume.

Simulations show that such a resolution is feasible with the proposed technologies (Fig. 1).

The baseline design of the ILD vertex detector consists of three, nearly cylindrical, concentric layers of double-sided ladders. Each ladder is equipped with pixel sensors on both sides, $\approx$ 2 mm apart, resulting in six measured impact positions for each charged particle crossing the detector (Fig. 2). The radii covered by the detector range from 16 mm to 60 mm. The material budget of each ladder amounts to $\approx$ 0.3 % X_0, equivalent to 0.15% X_0/layer.

This geometry is independent of the actual pixel technology being finally adopted.

[1] The International Large Detector (ILD) [7] is a concept for a detector at the ILC.

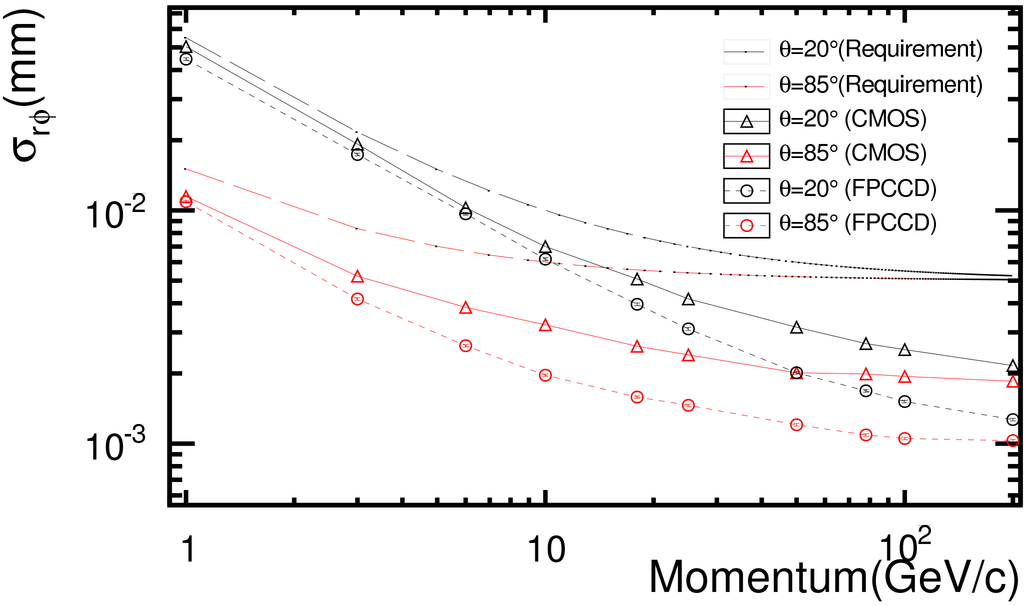

Figure 1: Impact parameter resolution of the ILD vertex detector for two different particle production angles (20° and 85°), assuming the baseline point resolution for the CMOS option (solid line), and the FPCCD option (dotted line). The curves with long dashes show the performance goal.

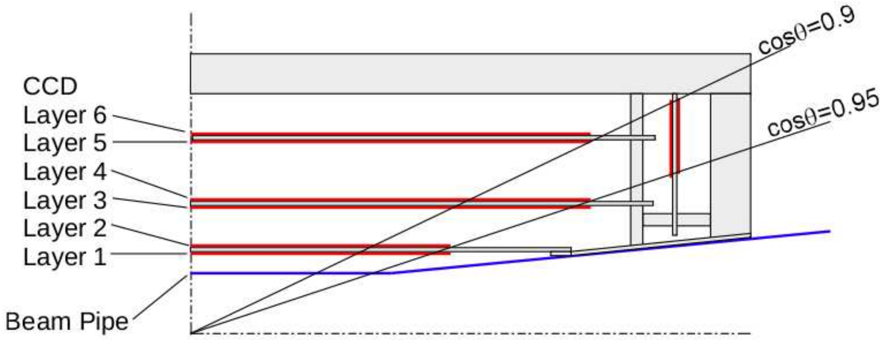

Figure 2: Schematic view of the ILD vertex detector. Every layer consists of three concentric layers of double-sided ladders. The inner layer length in the beam direction is half of the outer layers.

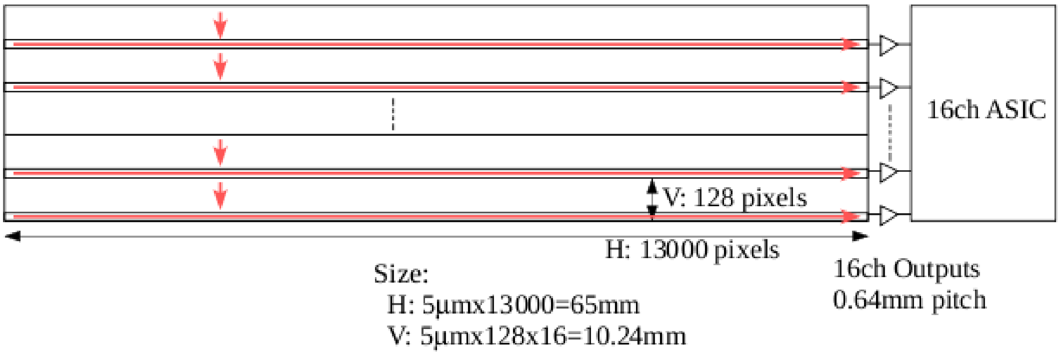

Figure 3: Schematic view of the innermost ladder of the FPCCD sensor. Each CCD wafer has 16 outputs covering 16 regions, and each region has 128 (V) x 13000 (H) pixels. Each region has a horizontal register to transfer the signal charge to the output node.

FPCCD

The FPCCD concept is based on the following:

1. Very small pixel size ($\approx 5\ \mu$m).
2. Fully depleted sensitive volume with 15 μm epitaxial layer thickness.
3. Readout between consecutive bunch trains crossing the interaction point.

The first item provides the FPCCD detector with excellent impact parameter resolution, below 1.4 μm, at high momentum limit for tracks with polar angle of 90 degrees.

The second item implies the charge spread between pixels is very small.

Readout in the inter-train has the additional advantage that the FPCCD is intrinsically free of beam-induced RF noise.

Another advantage of using FPCCD, and an unique feature of this sensor technology, is its use of cluster shapes to reduce the beam-induced backgrounds [3].

The dominant background stems from e^+e^- pairs from beamstrahlung, which are produced in the highly charged environment of the beam-beam interaction.

The schematic design of the FPCCD sensor is shown in Figure 3. The pixel size is 5 x 5 μm^2 and the thickness of the sensitive layer is 15 μm. For the outer layers, the pixel size is

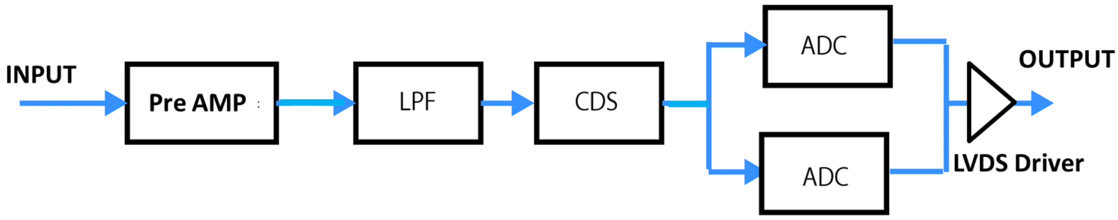

Figure 4: Readout ASIC overall architecture. ASIC has functions of amplifier, low-pass filter (LPF), correlated double sampler (CDS) and analog-to-digital converter (ADC). Two ADC are used to achieve the required readout speed.

envisioned to be somewhat larger. Each CCD wafer has 16 outputs covering 16 regions, and each region has 128 (V) x 13000 (H) pixels. The reason why the number of vertical (V) transfers is much less than the number of horizontal (H) transfers is that this configuration is more advantageous for the radiation tolerance. Each region has a horizontal register to transfer the signal charge to the output node. Pixels in the horizontal registers are also sensitive to the charged particles.

The required frequency to read out the whole pixel in the inter-train is $\approx$ 10 Mpixels/s.

The output signals from one edge of the CCD wafer are processed by an ASIC located next to the CCD wafer. This ASIC will have functions of amplifier, low-pass filter, correlated double sampler, and analog-to-digital converter (ADC) for 16 channels (Fig. 4).

3. Status R&D on FPCCD

Small Prototype Tests

We have made small prototype sensors with 6 μm pixel size and full size prototypes for the inner layers (Fig. 5). The readout system has been developed with 3 front-end ASIC's prototypes already fabricated. The latest ASIC prototype matches most of the design requirements [5] when operating at frequencies lower than 50 MHz. At high frequency (100 MHz) we observe an increase in the noise of the readout system. Figure 6 shows the sensor response when irradiated with Fe^{55} .

We estimate the amount of noise as 30 electrons, which is below the required value for the FPCCD (50 electrons). The main noise contribution is the CCD readout circuit.

Software R&D

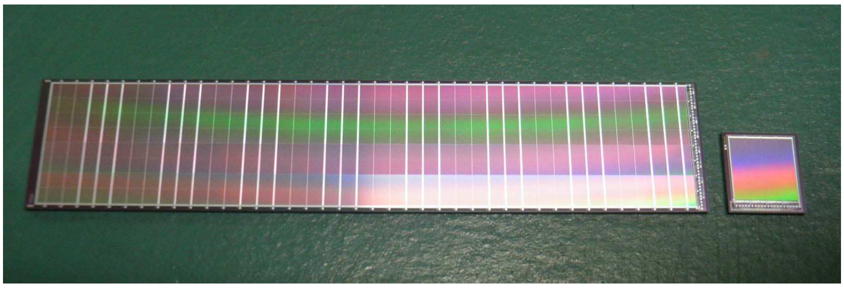

Figure 5: Small and full size prototype sensor with 6 μm pixel size.

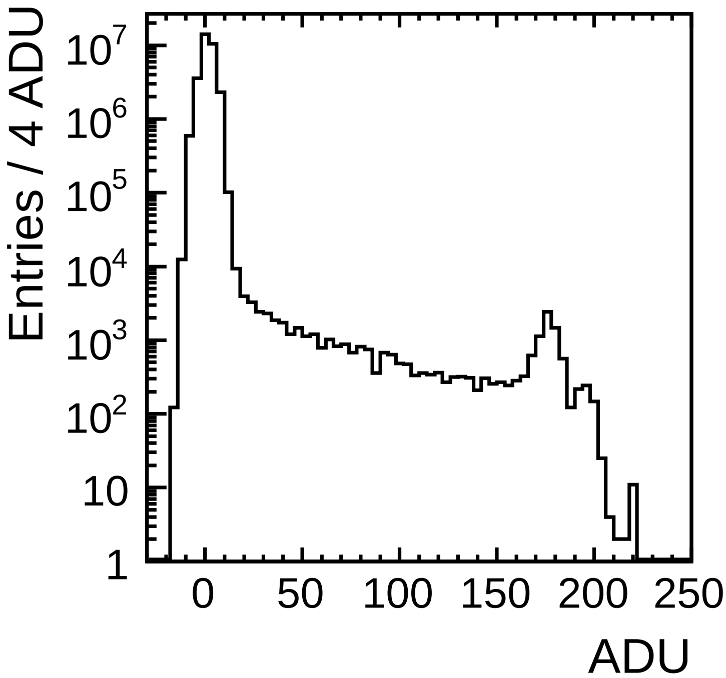

Figure 6: FPCCD response when irradiated with Fe^{55}. The two peaks in the range [150, 200] correspond with emissions of photons at energies 5.899 KeV and 6.490 keV.

We have developed a new vertex tracking, FPCCD Track Finder [6].

The new track finder tracking efficiency is $\approx$ 99% for $p_T > 0.6$ GeV/c. Figure 7 shows the improvement in the tracking efficiency for low p_T tracks when using FPCCD.

We have found that using a bigger pixel size (10 μm) in the outer layers saves $\approx$ 30% power consumption with no impact on the performance [6].

4. Conclusion

The Fine Pixel CCD (FPCCD) is one of the three sensor technologies being actively developed

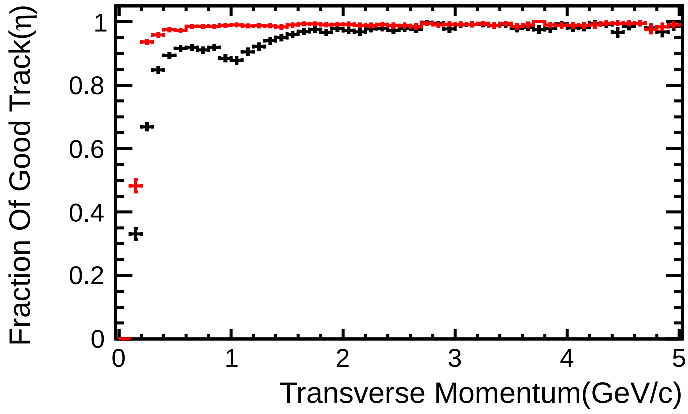

Figure 7: Comparison of the FPCCD Track Finder (red) with a previous version of the vertex tracking code [7] (black).

for the ILD vertex detector. We have covered the status of the R&D in the FPCCD detector. The tests carried out on the small prototypes matches the design requirements on noise level and power consumption at frequencies below 50 MHz.

We have developed a new Silicon Tracking, FPCCD Track Finder, which improves tracking efficiency on low p_T tracks.

We have found that using pixel sizes of 10 μm^2 in the outer layers reduces the power consumption by 30% while keeping similar impact parameter resolution and occupancy. We are analyzing the Charge Transfer Inefficiency (CTI) for the FPCCD. We plan to perform a beam test to study the radiation hardness of the sensors.

References

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