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Recent Results for 3D Pixel Integrated Circuits using Copper-Copper and Oxide-Oxide Bonding

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Abstract. Efforts have been on going for several years to develop a 3D integrated pixel circuit with a bonded sensor. The development process has experienced numerous fabrication problems. The two wafer bonding processes used for 3D assembly were copper-copper thermo-compression and oxide-oxide bonding. This paper will cover the main problems that were encountered along with techniques used to study the problems. It will also examine the sensor to 3D bonding technology that was used. Finally the first performance results of a successfully bonded 3D IC to sensor using these techniques will be presented.

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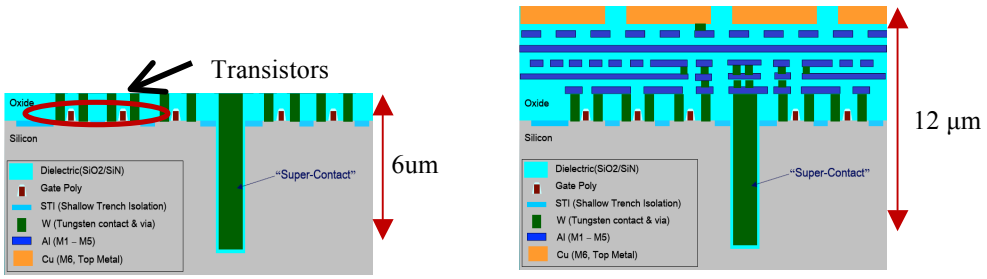
1. Introduction

Pixel readout devices for HEP (high energy physics) and related applications have continually pushed performance and space boundaries. 3D integrated circuits offers another means to achieve these goals. 3D integrated circuits offer the promise of pixel systems with finer pitch, less mass, greater localized detector intelligence, an alternative to conventional bump bonding, and pixel arrays without dead space. Two of the most promising wafer bonding technologies for 3D wafer bonding are copper-copper thermo compression and oxide-oxide bonding. These technologies have been explored at Fermilab for several years. Since these technologies have not yet become mainstream technologies with large production lines, numerous fabrication issues were encountered. Recent successes, however, have shown the feasibility of these technologies for HEP related applications. The issues encountered and some of the tools used to study them are discussed in this paper. Positive results from a 3D readout chip bonded to a sensor are reported for the first time.

2. Wafer Bonding

All of the wafers used for 3D bonding were fabricated by Global Foundries in the 0.13 um CMOS process. Access to the foundry was through Tezzaron [1]. 3D vias were inserted into the wafers at Global Foundries using a via middle process developed by Tezzaron.



Wafer after FEOL processing and via filling

Wafer after BEOL processing including M6 pads

Figure 1 – Wafer fabrication with via insertion

After fabrication of the CMOS transistors, 1 micron diameter, 6 micron deep, blind vias (super contacts) are inserted into the wafers. The super contacts are filled with tungsten at the same time connections are made with the transistors as shown in figure 1. Afterwards, the back end of line (BEOL) processing is completed with the additions of metal layers 1 through 6. The metal 6 layer is used exclusively for the fabrication of copper pads for electrical connection between wafers in a face-to-face bonding arrangement. The copper pads are arranged in a uniform hexagonal pattern on a 4 micron pitch across the wafer as shown in figure 2.

Our 3D wafers were bonded face-to-face which means that the blind vias extend away from the bonding interface and into the substrate. In different applications, 3D vias may be present in both of the wafers being bonded.

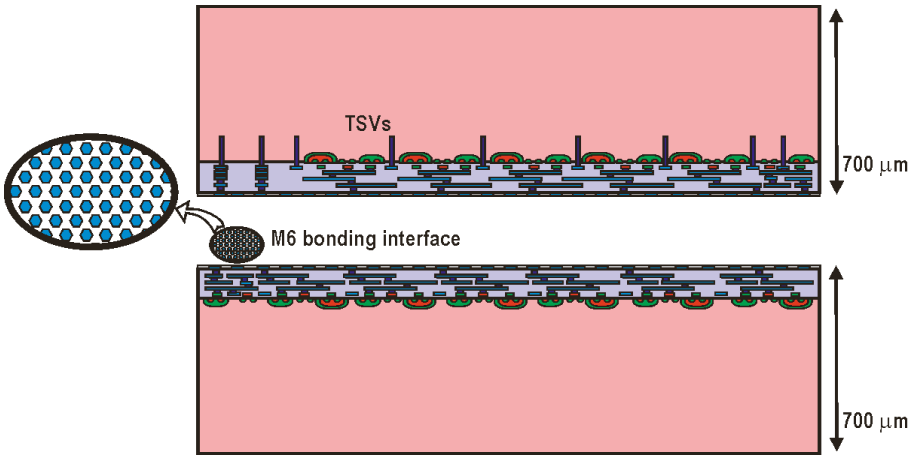


Figure 2 – Wafers to be bonded showing bond interface pattern and TSVs

A design consortium of 15 institutions led by Fermilab submitted a two-tier 3D multi project wafer run for fabrication. The 2 tier face-to-face designs used one set of masks to reduce costs. Numerous delays ensued and when the lot of 30 wafers was delivered, it was discovered that the wafer frames were offset from the centerline by 1.2 mm, which was beyond the allowed misalignment in the wafer bonder [2]. Consequently a new set of wafers had to be fabricated causing additional delays.

When the new set of wafers arrived, the M6 copper pads were prepared for bonding. The wafers were aligned face to face and then moved to the bonder to form the copper-copper thermo compression bonds, which provide both the mechanical and electrical connection between the wafers. After bonding, the top wafer was thinned to 12 microns to expose the TSVs and bond pads were added for wire bonding and detector mounting as shown in figure 3.

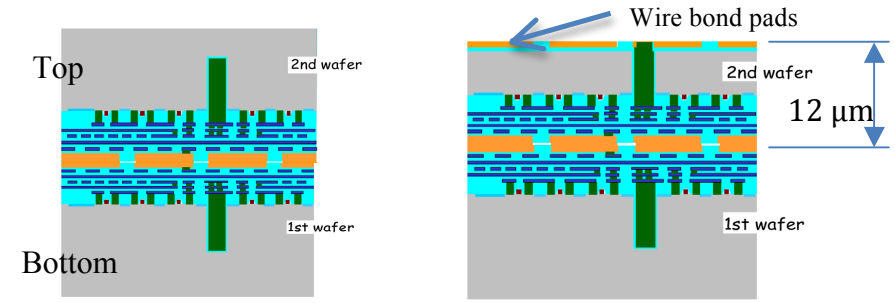


Figure 3 – Tezzaron copper-copper thermo compression 3D process

The first 6 wafers, which were bonded, failed due to residual carbon on the copper pads. The bad bonds could be observed in the acoustic images of the bonded wafers as seen in figure 4. The light areas indicate insufficient bonding. The dark ring around the perimeter indicates good bonding. These wafers would not survive the mechanical stress of thinning one wafer.

After cleaning the remaining wafers, a second set of 6 wafers was bonded at the same bonding facility. When tested, chips from these wafers exhibited electrical shorts and opens. The problem was found to be due to misalignment of the wafers as shown in Figure 5.

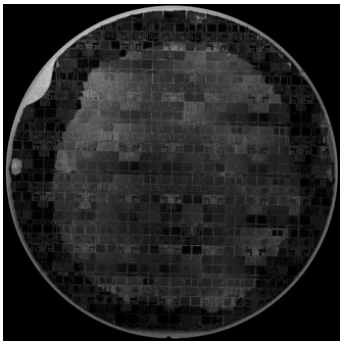


Figure 4- Poor wafer bonding

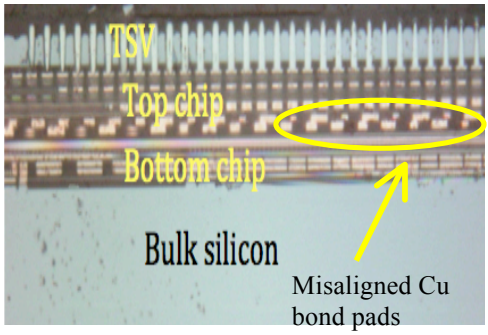


Figure 5- Wafer to wafer misalignment

The remaining wafers were sent to a facility in Austria where better bonding results had been previously obtained on other runs. Numerous attempts were made to bond a set of 8 wafers. However, in spite of higher bonding pressures and the use of a forming gas, unsatisfactory results were obtained. After analysis, it was determined that the copper bond pads on the wafers had developed large grain boundaries over time that inhibited bonding. As a result the last remaining wafers were sent to have the bond pads reconditioned. When these wafers were returned to Austria and bonded, good bonding in the shape of an eye pattern occurred mainly in the center of the wafer as shown in figure 6. The problem was that bonding had occurred initially around the perimeter of the wafers, trapping gas in the interior portions of the wafer which inhibited bonding.

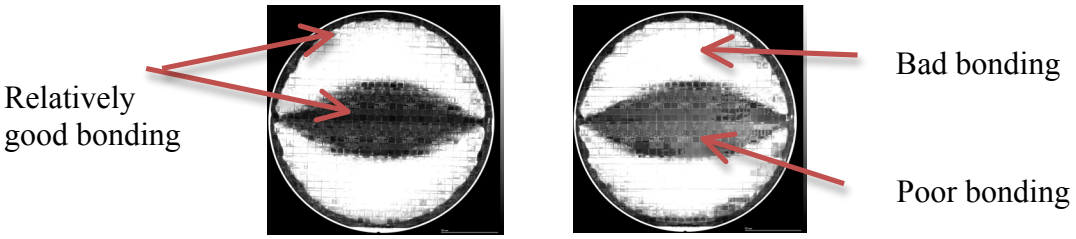


Figure 6 – Acoustic images of Cu-Cu bonded wafers showing good, poor and bad bonding areas.

After experiencing so many problems with the copper-copper bonding, it was suggested that oxide-oxide bonding using the Ziptronix DBI process might produce better results [3]. As an experiment, a pair of poorly bonded wafers were separated, the copper bond pads reconditioned, and the wafers rebonded with the DBI process. Bonded wafers using the DBI process and the copper-copper process are shown in figure 7.

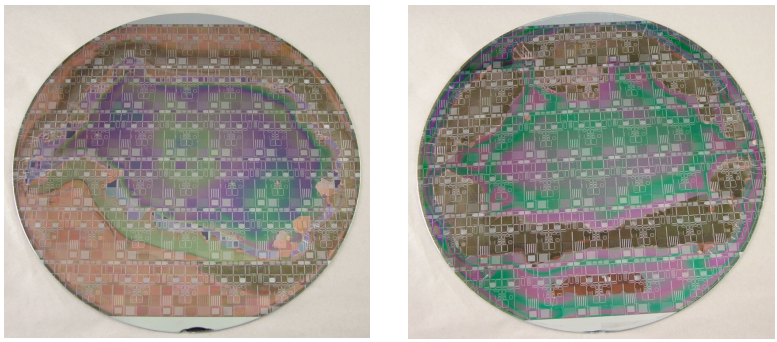


Figure 7- (left) DBI wafer pair, (right) copper-copper thermo compression bonded pair

The previously mentioned eye pattern is apparent in the copper-copper bonded wafers. Due to the prior wafer damage and repair, the DBI bonding was considered a significant success even though only the center bonded properly.

Consortium designs from the center of each of these wafers were distributed to the consortium members for evaluation. Fermilab had 3 different designs (VIP2b, VIPIC, VICTR) on these wafers. In spite of the fabrication problems up to this point, fully functional parts were tested at Fermilab and at the consortium facilities. This paper only discusses the VIPIC

We have found that the quality of the bonded wafers for the processes we used can be predicted by looking at the alignment keys on the bonded wafers before dicing of parts. Alignment keys, which are distributed across the wafer, can be used to look for translational and rotational misalignment. Our alignment keys are comprised of 3.8 um squares with a 6 um pitch, which are arranged in two distinct cross patterns as shown in figure 8. It is important to note that our copper bond interface is comprised of 2.7 um octagons on a 4 um pitch which means that alignment between wafers must be better than 1 um to avoid bonding problems.

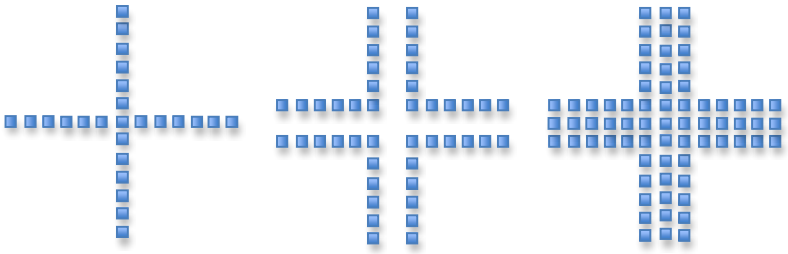
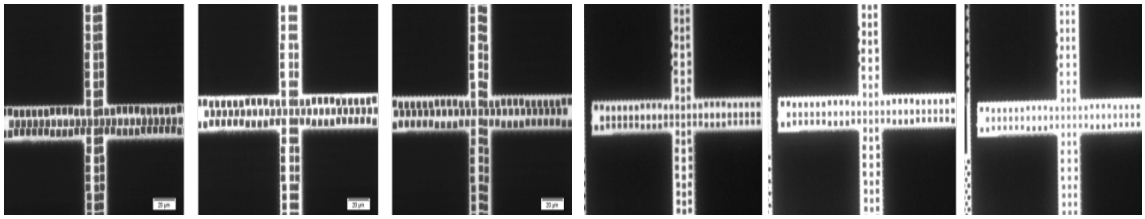


Figure 8 – Top wafer alignment key, bottom wafer key, proper key alignment

Figure 9 shows the alignment keys for the best Cu-Cu bonded wafer and the only DBI bonded wafer from the original batch of wafers. It is clear that there is better overall alignment with the DBI bonded wafer.



Cu-Cu bonded wafer DBI bonded wafer

Figure 9 – Left, middle, and right position wafer alignment keys

Due to the problems with the initial lot of wafers, another lot of 18 wafers was fabricated for 3D bonding. These wafers were assembled using both Cu-Cu bonding and DBI oxide bonding. The wafers were received over a period of time from March to July 2013. The four Cu-Cu bonded wafers exhibited significant variations in alignment quality ranging from bad to good as shown by the right alignment keys in figure 10. Unfortunately a bad wafer was diced before the alignment key information was received resulting in bad parts for initial testing.

From left to right alignment keys for wafers 1, 2, 3, and 4

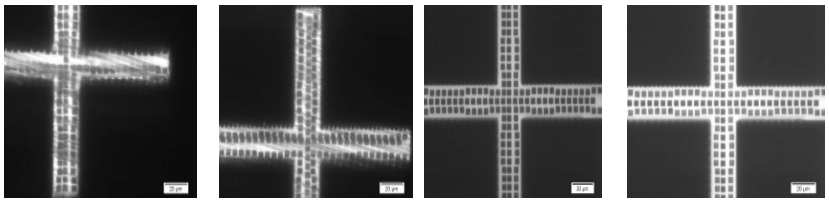


Figure 10- Right alignment keys showing alignment variations between wafers 1 ,2, 3, and 4

Four other wafer pairs were bonded using the DBI process. As can be seen from figure 11 the quality of the DBI process is much more consistent and significantly better than the Cu-Cu wafers we received. Wafer #6 was diced and parts distributed to 3D consortium members. Testing has been done at Fermilab on several VIPIC parts from the DBI processed wafer and all parts have been found to be functional suggesting a high yield. At this point all wafers from the HEP 3D consortium engineering run have been received and no additional wafers will be fabricated.

From left to right, alignment keys for wafers 5, 6, 7, and 8

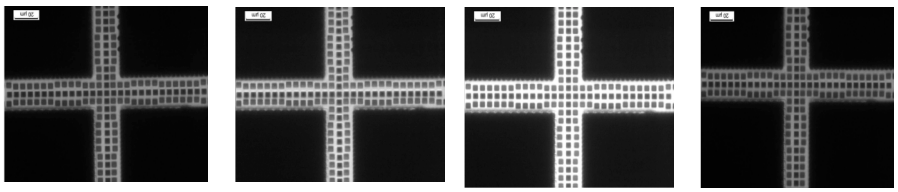


Figure -11- Right alignment keys for four DBI processed wafer pairs

3. VIPIC Test Results

The Vertically Integrated Photon Imaging Chip (VIPIC) is a pixel chip designed for photon science applications such as X-ray photon correlation spectroscopy [4]. The chip is designed to quickly count the number of hits in every pixel and read out the number of hits and addresses in a dead timeless manner. To achieve the desired speed requires a sparsified digital readout, where only the pixels that have registered a hit are read out. To implement the sparsified readout in a 130 nm process requires a digital design that would not fit in the desired pixel size of 80 μm x 80 μm along with the analog circuitry. Thus the pixel design was split into analog and digital design layers of equal area to meet the pixel size requirement. This division requires a large number of signals (25) to be passed between the analog and digital section of every pixel (over 100,000 connections/chip).

The VIPIC operates in two different modes: 1) Timed mode – sparsified readout of number of hits and addresses at low occupancy (~10 photons/cm^2/10 μsec), 2) Imaging mode - alternating 5 bit counters readout of number of hits in each time slot without addresses (there is less data without addresses). The VIPIC was tailored for X-rays at an 8 keV light source. Specifications are covered in reference [5].

A simplified block diagram of the VIPIC showing the column structure and parallel readout along with a single pixel is shown in figure 12.

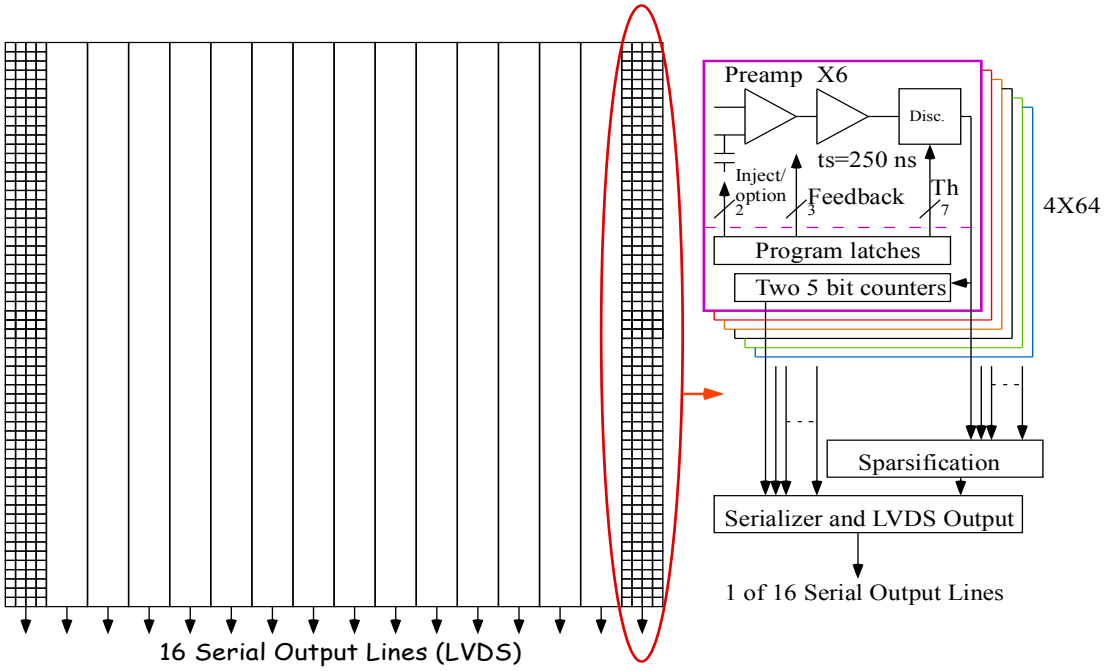


Figure 12 – VIPIC pixel arrangement on the left, single readout channel on the right.

The inject/option, feedback, and threshold signals are differential signals that are passed between the analog and digital section of every pixel (the discriminator output is single ended) resulting in over 100,0000 vertical interconnects in the 4096 pixel chip.

After visual inspection, initial tests were performed on a few chips (without sensors attached) from the Cu-Cu bonded and DBI wafers in the initial lot of 30 wafers. Of the 5 tested chips one Cu-Cu bonded chip was working and two DBI bonded chips were working. All three working chips performed similarly [5]. Tests confirmed that the 49152 bit configuration register was working, the address encoder was working, chips operated in both the counting and imaging modes, the counters were working, the sparsification was working, the pixel set and reset was working, and the performance of the thinned analog tier closely matched the simulated noise and power.

The 7 bit threshold DAC in every pixel was set to the end values (all 1's and all 0's) and the desired shift in noise hits for all pixels, as shown below in figure 13, confirmed that the DAC range was sufficient to trim all pixels.

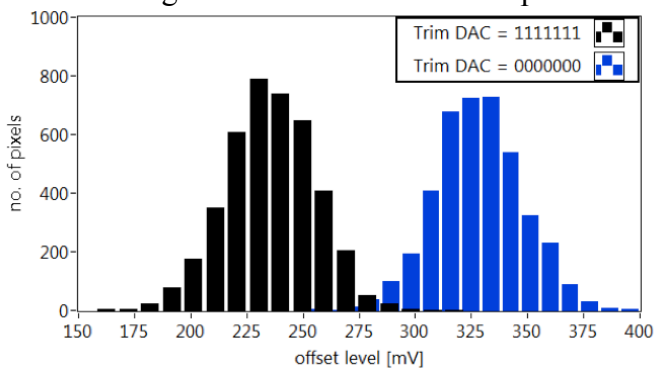


Figure 13 – Noise hits for all pixels at extreme ends of DAC settings

Due to the excellent alignment found on the DBI processed wafer 6, several parts from wafer 6 were sent out to have pixel sensors attached. The chips were not tested before sensor attachment. To expedite the testing, the 3D chips which have an 80 μm pitch were bonded to an available 32x38 pixel sensor arrays with a 100 μm pitch. An array of pads with a 100 μm pitch was deposited on the VIPIC to make the bonding possible. This left every 5th VIPIC input unbonded as shown in figure 14.

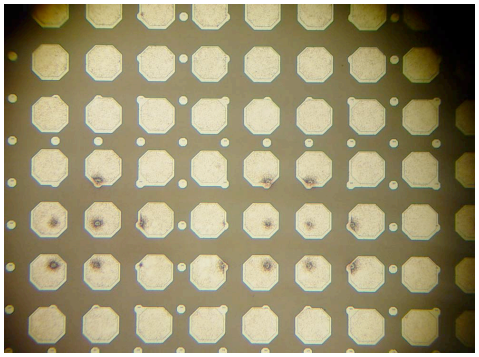


Figure 14- VIPIC bond pads for sensor

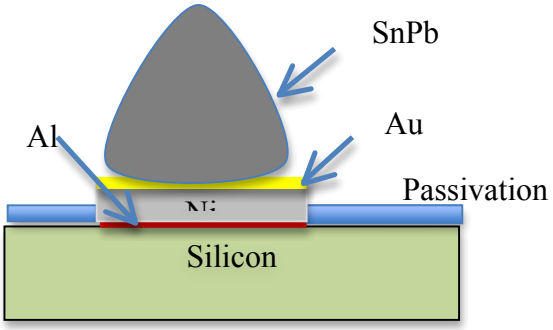


Figure 15- bump bond pad on sensor

It was decided to use conventional bump bonding to attach sensors to the VIPIC chip since it could be done on a chip-to-chip basis. The sensors were bonded by CVInc [6]. A solderable under bump metallization, comprised of Ni and Au, was added over the Al pads [7]. A 75 μm high eutectic SnPb bump was then deposited with ultimately 100% yield. The pads on both the VIPIC and sensor were approximately 60 μm in diameter. An under fill was added for mechanical strength

With the sensor attached but not biased, hits from 22 keV X-rays were observed from a ^{109}Cd source. With a threshold of ~40 mV (200 ADC counts) and no source, the noise hits disappeared as expected. See figure 16. When X-rays illuminate the sensor, hits are observed as shown in figure 17. (Note every 5th VIPIC readout channel is dark since no pixel is connected to it.) When the threshold was raised to ~240 mV (1200 counts), all hits disappeared.

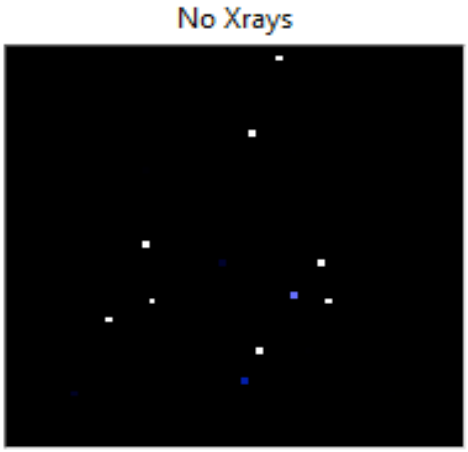


Figure 16 – 40 mV threshold- no hits

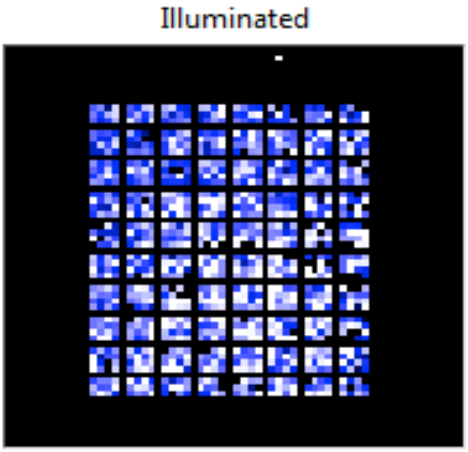


Figure 17 – sensor sees X-rays

Additional tests were performed with a fully depleted sensor using both a 22 keV ^{109}Cd and a 5.9 keV ^{55}Fe source. A radiogram image of a small tungsten mask placed on top of the sensor was taken as shown in figure 18.

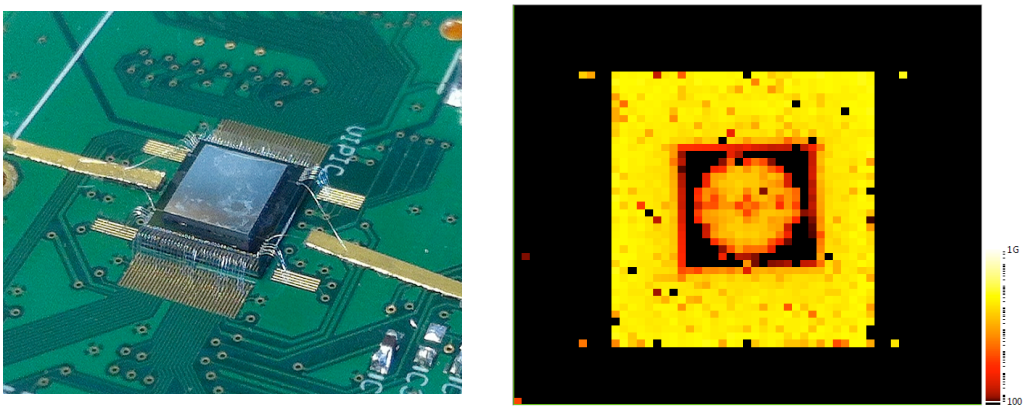


Figure 18 – (left) wire bonded VIPIC and sensor, (right) radiogram with tungsten mask

The dark area around the perimeter is from the area of the VIPIC without a sensor input. The square yellow area is the sensor without the mask. The inside black square is due to the mask and the roundish yellow center is the opening in the mask. The fully sparsified readout from all 16 groups of 128 pixels was used in the acquisition and readout. Every 5th skipped pixel was removed in software from the radiogram image.

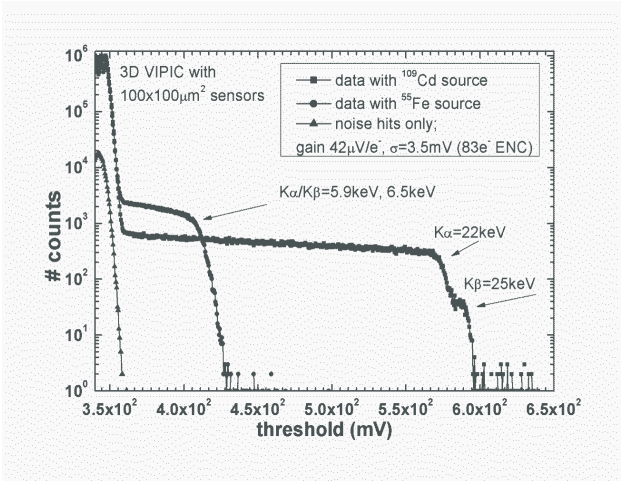


Figure 19 – Single pixel threshold scan for both Cd and Fe sources

To establish gain and noise more accurately, threshold scans with 0.5 mV resolution were performed on a single pixel in a fully depleted sensor with a flat field illumination using both Cd and Fe sources as shown in figure 19. Tests were run using a 50 Mhz clock and a fully sparsified readout. The gain was measured to be 42 μV/e- and the noise, 83 e- rms. It should be noted that the response of the VIPIC is approximately linear up to 18 keV, which is more than sufficient for targeted 8 keV photons.

4. Future Work

The VIPIC was initially bump bonded to a sensor chip to establish the performance of the VIPIC and to avoid the risk of losing VIPICs on wafers. One of the goals of the 3D effort is to eliminate the conventional bump bonding which has often proved to be

costly and problematic. Since the successful testing of the VIPIC with a sensor, work is now progressing to bond 80 μm pitch sensor wafers to VIPIC wafers using the Ziptronix DBI process. When this is completed we will have a 3 tier stack of electronics and sensors without bump bonds and without missing channels. Additional work is also anticipated to place the VIPIC and sensor assemblies in a light source to test the sparsified read out performance under realistic conditions.

4.Conclusions

The path towards assembly of 3D integrated circuits using Cu-Cu thermo compression and oxide-oxide DBI for fine pitch pixel devices encountered numerous problems along the way. Recently however, positive results have been obtained with the testing of the VIPIC. Although both the Cu-Cu and DBI process yielded working devices, the DBI process was more consistent and had higher yields. In hindsight, if our designs had used a coarser bond pad pitch and if we had pursued the DBI process sooner, a couple of years of development work could have been saved.

Nevertheless, the successful testing of the VIPIC with a sensor represents the first known 3D chip and sensor developed for photon science and the related HEP community in general. This accomplishment should be considered a proof of principle for future 3D work within HEP and photon science.

Acknowledgements

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