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Novel powering schemes for pixel and tracking detectors

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Future pixel and tracking systems like the ones foreseen in the upgrade programs of the LHC experiments are very demanding on the power supply systems. An increased amount of power has to be supplied to the front-end electronics at a reduced voltage, through existing cable plants. Novel powering schemes are needed to avoid excessive cable losses. The two schemes under consideration, serial powering and DC-DC conversion, are reviewed. Particular emphasis is put on system integration aspects. As an example, the new CMS pixel system, which will be powered via DC-DC conversion, is presented in more detail. This allows to discuss challenges and solutions for a concrete application while the conclusions should be relevant for other applications as well.

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1. The power challenge

Pixel and tracking detectors need to be supplied with typically many kilo-watts of power at rather small voltages in the range of a few volts. Due to the tight space constraints, the harsh radiation environment, and the high magnetic field inside the detector volume, the power supplies have to be located tens of meters away such that long cable runs are needed between the supplies and the detector. The CMS strip tracker may serve as an example [1]. It consists of some 15'000 detector modules which are organized in about 2'000 power groups. Each power group is supplied by a power supply unit via a ≈ 50 m long cable (see Fig. 1). These power supplies sit in racks located on the balconies at the walls of the experimental cavern. The total front-end power consumption amounts to 33 kW. Since the front-end ASIC supply voltages are 2.5 V and 1.25 V, this power corresponds to a total current of about 15 kA. Given the ≈ 50 m cable length Ohmic losses are substantial and even though the available cable channels have been fully used these losses amount to about 34 kW, i.e. the same power as is required by the front ends: 50% of the power is lost in the cables.

Future pixel and tracking systems like the ones foreseen in the upgrade programs of the LHC experiments are even more demanding on their power supply systems. The need for higher resolution and more robust pattern recognition leads to designs with a much increased density and total number of channels. More functionality inside the front-end ASICs like analogue to digital conversion or hit correlation for triggering is often desirable. Data transmission speeds need to be increased substantially. All this costs power. Fortunately ASIC technology scaling from the currently widely used 250 nm down to 130 nm and 65 nm can be used to reduce the power per transistor so that the total power budget of these systems does not simply scale with the number of channels. Still the future systems will typically consume more power. An estimate for the CMS tracker upgrade arrives at 70 kW, i.e. about a factor of two higher than today. There is, however, a price to pay when using smaller ASIC technologies: the required supply voltages decrease as well, from 2.5 V to 1.2 V and 0.9 V for the technologies mentioned above, and so do the allowed voltage margins. More power at smaller voltages leads inevitably to much increased currents. Again for the example of the CMS tracker, the total current will increase by roughly a factor four. Because Ohmic losses scale as current squared, the power lost in the cables would be higher by a factor of about 16! Since there is no way to increase the copper cross sections of the cables to mitigate this effect one comes to the conclusion that the pixel and tracking systems planned for the LHC experimental upgrades and also in some other experiments just cannot be powered in the traditional way. Novel powering schemes are needed which are able to provide more power to the front-ends, at a similar or even lower supply current than today [2]. This may also allow to reduce cable cross sections inside the detector volume which is highly desirable as multiple scattering in the detector material is limiting

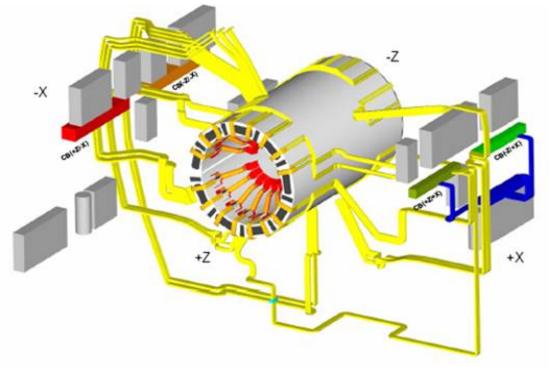

Figure 1: Routing of CMS tracker cables.

the measurement resolution at low momenta. Such a novel powering scheme has to supply the required voltages to the front-ends within the small allowed margins. It also has to be very robust and reliable with sufficient slow control features and fault tolerance. Obviously the extra material needed to implement such a powering scheme should be kept to the minimum.

2. Powering options

From the point of view of system design, possible solutions to the power challenge can be grouped in three categories of increasing deviation from today's system design. They all rely on the fact that power is voltage times current and therefore the supply current can be reduced by a certain factor when power is supplied at a voltage increased by the same factor. Cable losses are then reduced by the square of this factor which may allow to actually reduce the amount of material represented by cables and copper traces inside the detector volume.

Voltage conversion at each front-end ASIC

In the first category the problem is solved locally at each front-end ASIC by the addition of some circuitry such that it can be powered at 2.5 V or higher. This approach is widely used in modern commercial CPUs. However, for several reasons including radiation and magnetic field tolerance the solutions cannot be just transferred. Charge pumps with a conversion factor of 2:1 have been identified as viable solutions. They charge up capacitors in series and discharge them in parallel such that the voltage is reduced and the current increased. Besides some switching and control circuitry on the ASIC they typically require external capacitors next to each ASIC. As the front-end ASICs include very sensitive amplifiers for the small detector signals, switching noise of the charge pump has to be limited to acceptable levels. Such charge pumps have been developed and implemented in several recent front-end ASICs and have generally shown to work (see for example [3]). The advantage of this approach is that the overall system design can be kept identical to today's. However, these charge pumps are currently considered insufficient to fully address the power challenge. They might however provide a first voltage conversion step in the schemes to be described next. Since the focus of this review is on system aspects these charge pumps are not covered in more detail here.

Voltage conversion for a group of modules

Higher conversion factors up to 8:1 and beyond as well as higher currents can be achieved by DC-DC converters of the buck type which will be described in detail in section 4. Since they represent a certain amount of material they need to be implemented at the level of one module or a group of modules. On the other hand this approach avoids extra components close to each front-end ASIC. These converters are switching devices as well and therefore switching noise is a concern, although these converters are located further away from the small signal paths. Fig. 2 compares such a DC-DC powering scheme to a conventional powering scheme as used today. Although the figure only provides a very much simplified representation of these systems it can be seen that a system design including DC-DC conversion is still rather similar to today's powering systems. More details are given in sections 4 and 5.

Serial powering of modules

An alternative approach which allows for even higher conversion factors and potentially very little extra material is to power many detector modules in series. Provisions have to be made to control the voltage that each module sees and to be able to bypass any module in the chain in case of failure. This has to be achieved by some shunt regulation and bypass circuitry which can be implemented either as a separate ASIC or as part of the front-end ASICs. The absence of fast switching of large currents relieves this approach from switching noise concerns. On the other hand all modules in a chain are coupled and changes in the current consumption of one module may have effects on other modules. In terms of system design this scheme is rather different from the conventional scheme (Fig. 2). All modules are at different ground potentials which makes grounding and shielding challenging and requires special care in the layout of the communication with each module. More details on this scheme are given in the next section.

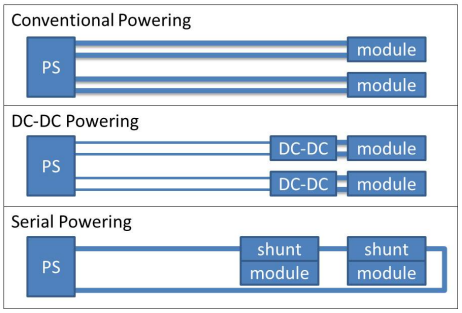

Figure 2: Schematic comparison of the different powering schemes.

3. Serial powering

A serially powered chain of detector modules is supplied by a constant current source. The required current is determined by the biggest load in the chain so that this scheme is most easily implemented for a chain of modules which all require the same current like in a typical barrel layer. For detector end-caps on the other hand where typically modules with different number of ASICs or different hit rates are mixed in a chain this scheme is less optimal. A shunt regulator is needed for each module which bypasses part of the current such that the voltage provided to the module stays constant, independent of the current consumed by the module. In fact, if the module requires more than one voltage then such a regulator is needed for each voltage separately. Different implementations of these shunt regulators have been devised [4], including a solution where all functionality is concentrated in one ASIC and various schemes in which the functionality is shared between a regulator ASIC and circuitry in each front-end ASIC. A bypass transistor is needed in addition at each module which can take the full current in the chain in case the module fails and stops drawing current. Even with shunt regulators in place, fast load variations of individual modules can still lead to supply voltage variations on other modules in the chain. Therefore also passive filtering in the chain may be needed. An inherent feature of the serial powering scheme is that each module in the chain has a different reference potential. One consequence is that readout and control signals have to be AC or opto coupled which requires some extra components at each module. Still the amount of material required for the implementation of serial powering is low and since in principal many modules can be put in series (e.g. 10-20) high gain factors can be achieved in terms of cable losses and material budget. An example of the implementation of a serial powering scheme is prototyping work for the ATLAS pixel detector [5], [6]. Figure 3 shows a stave with a chain of four operational pixel modules. A shunt regulator ASIC (ShuLDO) has been

developed which is a combination of a shunt and a low drop-out regulator (LDO). Two ShuLDOs can be operated in parallel such that the modules can be supplied with two different voltages as required. It has been demonstrated that this chain of modules can be operated safely with noise values which are very similar to those obtained for modules with conventional powering. In order to test the stability of the chain, individual modules have been made noisy by lowering the hit detection threshold. In these tests the other unchanged modules did not show a significant increase in noise. It can therefore be concluded that this work represents a proof of concept that serial powering works for such systems.

Further research on serial powering has been carried out for the ATLAS strip tracker [7]. A distributed serial powering architecture has been implemented where the shunt transistors were located in the front-end ASICs with one control block per hybrid. Prototypes with four modules (eight hybrids) showed good performance. Longer prototypes with 24 hybrids are in preparation.

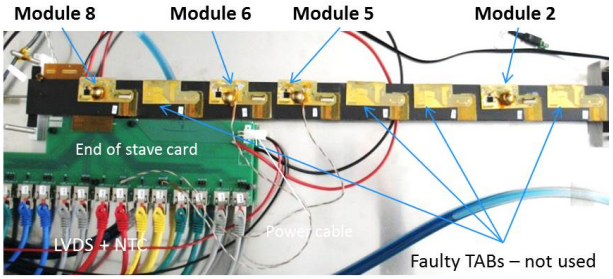

Figure 3: Prototype of a stave with four serially powered pixel modules for the ATLAS pixel detector.

4. DC-DC powering

In a DC-DC powering scheme DC-DC converters are placed either on the detector modules or at a certain distance to those, depending in particular on space constraints. These converters transform a high voltage (e.g. 10 V) into the required low voltage while the current drawn from the supply is lower than the current provided to the module by the same conversion factor (apart from inefficiencies). Cable cross sections between the power supplies and these converters profit from the reduced current while the power lines between the converters and the modules remain as in a conventional scheme. Voltage drops have to be carefully analysed in case the converters are located at a distance to the modules. Since the converters themselves represent a negative impedance load to the power supply, the voltage regulation of the power supplies has to be appropriately designed. The DC-DC converters will typically implement a number of protection features for instance against over-current and over-temperature. Furthermore, control of and status information from the converters may be desirable. Due to their fast switching (MHz range) the converters should themselves be well shielded and the system design should in addition ensure that detrimental effects due to electromagnetic interference are avoided [8].

The main new component in a DC-DC powering scheme is the converter itself. Buck type converters are an appropriate choice since they consist of relatively few components and can supply currents of several amps at high efficiency. DC-DC converters are widely used in commercial electronics. The harsh radiation environment and high magnetic fields make the application of DC-DC converters in high energy physics experiments however quite special. Since commercial converters may at best be accidentally radiation tolerant a dedicated development of radiation tolerant DC-DC converters seems appropriate, in particular in view of possible single event effects.

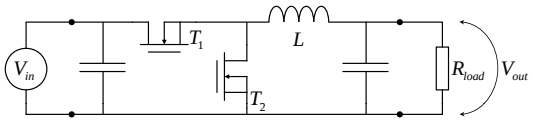

Figure 4: Simplified schematics of a DC-DC buck converter. Transistors T_1 and T_2 are operated by a pulse width modulation logic which is not shown.

The operation principle of a buck converter can be seen in Fig. 4. The main components are an ASIC which contains two large transistors and control logic, an inductor as energy buffer, and filter networks. The load is connected in series with the inductor to the power supply via one of the transistors (T_1). This transistor is closed only for part of the time (duty cycle D) while for the rest of the time the inductor keeps the current to the load flowing via the second transistor (T_2). Since the average current drawn from the power supply is reduced by the factor D, energy conservation requires that the input voltage to the converter has to be higher by the inverse factor, assuming a lossless converter: $V_{in} = V_{out}/D$. Typical conversion ratios are in the range 2 to 10. Pulse width modulation logic is used to regulate the output voltage. Since the current ripple at the inductor decreases with switching frequency, high frequency operation seems advisable to minimize this ripple and the corresponding resistive losses in the inductor and the transistors. However, switching and driving losses of the transistors increase with frequency and a switching frequency in the range of $1-3$ MHz turns out to be an optimal choice for the ASIC technologies used. Efficiencies, defined as the ratio of the power provided by the converter to its input power, are in the range 60 to 90 %.

An ASIC for such DC-DC converters has been developed over the past years by a group at CERN [9]. There have been several iterations, all manufactured in a commercial 0.35 μm CMOS technology, with a high voltage module developed mainly for automotive applications. It has been shown that this technology is radiation tolerant up to a total ionizing dose above 200 Mrad and displacement damage up to $5 \cdot 10^{14}$ 1-MeV-n/cm^2. These ASICs, of which AMIS5 was the latest available version at the time of the conference, can provide 3 A output current (more with appropriate cooling) at an output voltage adjustable between 1.2 V and 4 V. The input voltage can be up to 12 V. The switching frequency is adjustable in the range 1 MHz to 3.5 MHz. Besides the two big transistors T_1 and T_2 the ASIC contains the pulse width modulation logic which regulates the output voltage based on a band gap reference. Furthermore it contains protection against over-temperature, input-under-voltage and output-over-current. The ASIC can be disabled and outputs a power good status signal. This development work is being continued with the FEAST ASIC, manufactured in the same technology, which is intended to be used in upgrade detector systems.

5. The CMS pixel detector upgrade

In order to be able to illustrate some of the system design issues of implementing a DC-DC conversion scheme in a big detector system, the CMS pixel detector upgrade is taken as an example [10], [11]. It will actually be the first application of DC-DC conversion in such a large system. While the current pixel detector has been specified for the LHC design luminosity of $1 \cdot 10^{34}$cm^{-2}s^{-1} the LHC upgrade planning foresees an increase of the luminosity to about twice this value before the next long shutdown around 2018. This would lead to excessive dead time in the read-out ASIC. CMS plans to exchange the current pixel detector at the end of 2016 with a new system with an improved read-out ASIC. The new system will furthermore have one more detection

layer (4 barrel layers and 3 disks at each end) which improves considerably the pattern recognition and track parameter measurements at the expected high track densities. This will, however, lead to an increase of the number of channels and a corresponding increase of the power consumption by a factor of 1.9. Since the installed cable plant must be re-used the heat load on the supply cables would increase by almost a factor of four which would not be tolerable. CMS has decided to use a DC-DC conversion powering scheme to operate the new pixel detector. The converters will transform an input voltage of 10 V to output voltages of 2.4 V and 3.0 V, corresponding to a conversion ratio of $3-4$ and therefore a reduction of the cable losses by about an order of magnitude.

5.1 System integration

Figure 5 shows an overview of the new CMS pixel system. The barrel detector (BPIX) and end-cap disks (FPIX) are located in the centre. They are supported and supplied with services by means of supply tubes (for BPIX) and service cylinders (for FPIX) which are attached at both ends. The DC-DC converters will be located on these carbon fibre structures, for BPIX inside channels on the outside of the supply tube, for FPIX on the inside of the service cylinder. In this way the converters will be between about 0.5 m and 2 m away from the pixel modules at a pseudorapidity around four, i.e. outside of the acceptance of the CMS tracking system. The converters are cooled by CO_2 cooling pipes which run along the tubes and cylinders.

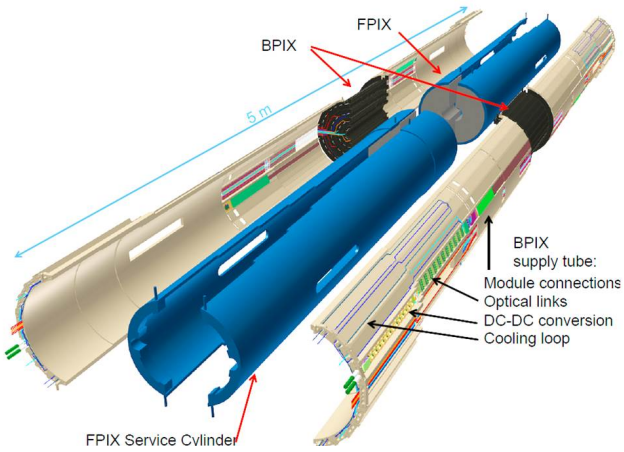

Figure 5: CAD drawing of the new CMS pixel system.

In total 1184 DC-DC converters will be needed. Since the pixel read-out ASIC requires two different voltages for its analogue and digital sections, converters of two different output voltages will be used in pairs to power the modules. Figure 6 shows 13 pairs of converters for BPIX, mounted on a PCB called 'bus board'. Six to seven converter pairs are powered from one dual channel power supply. Each converter pair in turn powers one to four pixel modules, depending on the layer in which the modules are mounted since the digital current scales with the hit rate which is higher in the inner layers. The maximum required output current per converters is below 3 A.

A number of system integration issues had to be considered and addressed. Since DC-DC converters inside the detector volume are a new concept there is no working experience to rely on. In particular it was unclear which control and protection features are necessary. The chosen approach can be summarized as follows. The converters switch off in case of over-temperature and input-under-voltage and switch back on when conditions are again fine; the output current is limited. A solid state fuse disables converters with excessive current permanently so that the other converters on the same supply line can still be operated. Converters can be dis-/enabled

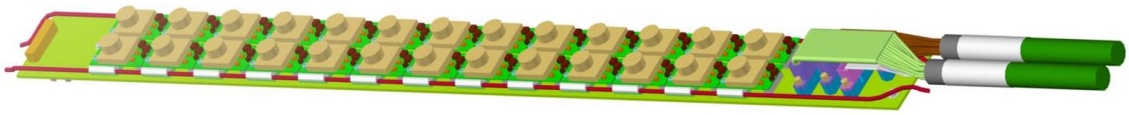

Figure 6: A bus board carrying 26 DC-DC converters. Two cables from the distant power supplies are connected on the right while the connections towards the pixel modules are on the left side. Each pair of converters sits on a cooling bridge for thermal contact to the CO_2 cooling pipes.

and their status read via slow control communications. No remote sensing at the pixel modules is foreseen, i.e. voltage drops need careful attention. The design of the converters themselves and their integration into the system have to ensure that there is no electromagnetic interference between the converters and the pixel modules which in this application is less critical due to the relatively large distance between the converters and the pixel modules. Single event upsets in the DC-DC converters have to be expected at some level and the system design must be able to tolerate the corresponding resets of the converters. Several PCBs (bus boards etc.) are needed to distribute large currents to and from the converters. They need to be carefully designed in order to equalize and minimize voltage drops between the converters and the pixel modules. Further issues to be addressed are the tight space constraints and the accessibility of the converters for possible repair work. Finally, since each converter dissipates about $1-2$ W of heat, active cooling is required.

5.2 DC-DC converter development

A DC-DC converter tailored to the requirements of the CMS pixel upgrade has been developed at RWTH Aachen University [11],[12],[13],[14], based on the CERN ASICs of the AMISx family and will soon be adapted to the FEAST ASICs. Figure 7 shows the current prototype version. It consists of a two-layer PCB of size 2.8 cm $\times$ 1.7 cm, which carries the ASIC, the inductor, as well as pi filters at the input and output. An input voltage of 10 V is converted to either 2.4 V or 3.0 V at a switching frequency of 1.5 MHz. The inductor, made in industry, consists of copper wire wound around a plastic core and has an inductance of about 450 nH. Due to the high magnetic field of 3.8 T in CMS any ferrite would be saturated and therefore such an 'air core' coil has to be used. The toroidal shape reduces electromagnetic emissions considerably, compared to a solenoid. The

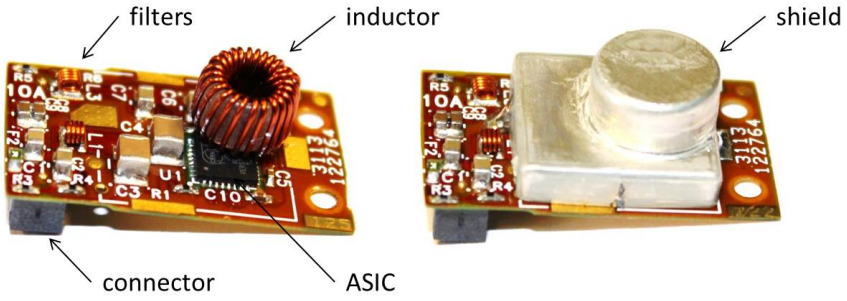

Figure 7: DC-DC converter without (left) and with (right) shield.

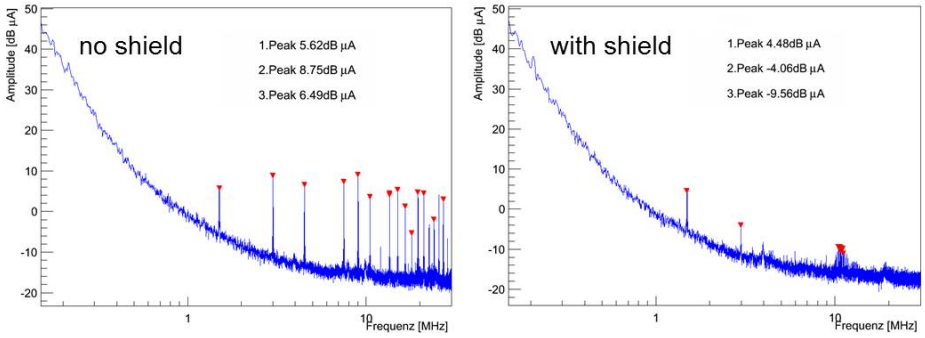

Figure 8: Common mode noise spectrum of a DC-DC converter without (left) and with (right) shield.

right part of Fig. 7 shows the converter in its final configuration with a shield covering the ASIC, the inductor, and the noisy parts of the circuit. This shield is made of plastic with 0.3 mm wall thickness, covered with 30 μm of copper and 1 μm of tin on both sides. It has three functions: it shields the magnetic emissions by means of eddy currents in the metal layers, it segregates the noisy parts of the circuit from the output filters, and it acts as a cooling contact for the inductor. Because of the latter function the space between inductor and shield is filled with heat conductive paste. The total weight of one converter is around 3 g. About 100 DC-DC converter prototypes have been built so far.

Extensive tests have been performed to check the functionality of these DC-DC converters [13], [14]. The electromagnetic emissions of the converters and in particular the effectiveness of the shield have been measured by scanning the emitted electromagnetic field with a pick-up probe. The shield reduces the emissions by more than an order of magnitude to a level which is found to be negligible. Figure 8 shows the common mode noise spectrum measured on the output lines of a converter without and with shield. The higher harmonics of the switching frequency are damped very efficiently by the shield so that the noise seen by the pixel modules is very low. From these and further measurements it can be concluded that emissions due to the switching of the converters have been successfully minimized by the chosen design including the shield.

The efficiency is another important property of the converters. Figure 9 shows the measured efficiency, averaged over 5 converters with 2.5 V output voltage, as a function of input voltage and output current. The efficiency is rather uniform with values around 80 % which is sufficient for this application. The efficiency of converters with 3 V output is a bit higher. The spread between converters if very low. Further measurements have confirmed that the maximum efficiency is reached for the chosen switching frequency of 1.5 MHz and that there is a very mild temperature dependence of about 1 % efficiency increase per 20° C temperature decrease.

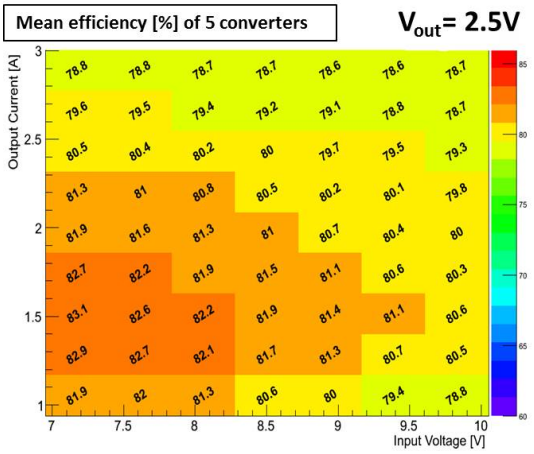

Figure 9: Mean efficiency measured on 5 converter prototypes with 2.5 V output voltage in percent as a function of input voltage and output current.

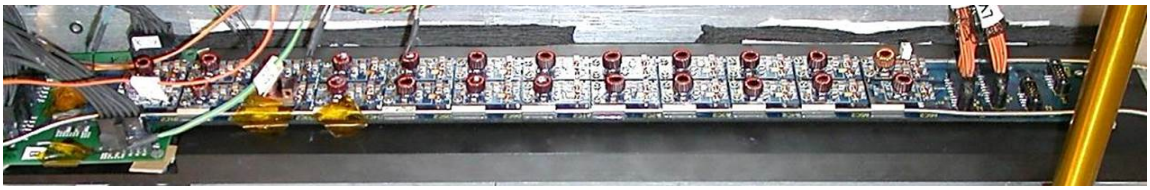

Figure 10: 24 DC-DC converter prototypes mounted on a bus board and CO_2 cooling pipes for system test measurements.

5.3 System tests

A system test was set up which was intended to resemble, as far as possible, the final system in the experiment. Figure 10 shows a bus board which was equipped with 24 DC-DC converters. These were screwed onto aluminium cooling bridges which were attached to CO_2 cooling pipes. The system was powered by a prototype pixel power supply via a 40 m long cable as will be the case in the experiment. Two barrel pixel modules (of the current type since the new ones are not yet available) were powered by the DC-DC converters, via 2 m of low mass cables. An additional electronic load has been used to fully load the system. In the first step the thermal performance was tested. The two phase CO_2 system was operated at $-20°$C with all converters running under full load. While the cooling bridges were at around 0°C, the temperatures measured on the ASICs and the inductors were just below $+20°$C at 3 A output current per converter, demonstrating the proper thermal functionality of the full system.

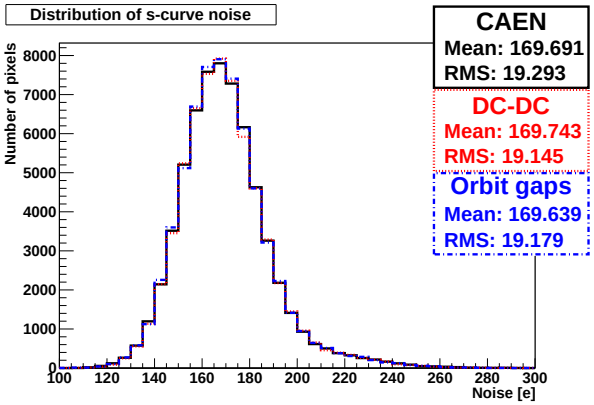

Figure 11: Noise distribution (in electrons) of all pixels on a present CMS pixel module when operated with CAEN power supplies as in the experiment today (solid black histogram), by a pair of DC-DC converters with 24 converters operating in parallel (dotted red histogram), and when fast load changes as expected from the LHC orbit gap are simulated (dash-dotted blue histogram).

Then data were taken with the two pixel modules in order to measure the noise distribution of all pixels on these modules. Three scenarios have been compared. In the first one, power was provided directly by the external power supply as in the present pixel system. In the second case the two modules were powered via DC-DC converters with all 24 converters running in parallel. Finally a test was performed to determine if the fast load variations expected due to the LHC beam structure (3 μs abort gap every 89 μs during which the digital activity and therefore the corresponding current of the modules drops to zero) has an impact on the stability of the system. As can be seen from Fig. 11 the noise distributions measured in these cases are practically identical. Both tested modules show the same result. These measurements demonstrate that in as close an approximation to the final system as can be operated presently, the DC-DC converters do not have any adverse effect on the noise of the pixel modules.

6. Summary

Future pixel and tracking systems need improved powering schemes due to the large power required at low voltages. Different schemes, namely DC-DC conversion at each read-out ASIC, DC-DC conversion to power (multiple) modules, and serial powering, have been proposed to efficiently provide power to these detector systems. All options have been shown to work in the small systems tested so far. System integration aspects have to be carefully analysed and should guide the choice of an appropriate powering scheme. The first large detector system based on such a novel powering scheme will be the CMS pixel detector upgrade to be installed in 2016 which has been used as a case study to describe system integration issues in more detail.

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