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Low Mass Integrated Cooling

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Low mass on-detector cooling systems are being developed and studied by the Detector Technology group (PH-DT) in the CERN Physics Department in close collaboration with LHC and non-LHC experiments. Two approaches are currently being investigated. The first approach, for barrel configurations, consists in integrating the cooling apparatus in light mechanical structures supporting the detectors. In this case, the thermal management can be achieved either with light cooling pipes and thin plates or with a network of microchannels embedded in thin strips of silicon or polyimide. Both configurations are being investigated in the context of the 2018 upgrade program of the ALICE Inner Tracking System (ITS). Moreover, it is also possible to use a silicon microchannel cooling device itself as structural support for the detectors and electronics. Such a configuration has been adopted by the NA62 collaboration for their GigaTracKer (GTK) as well as by the LHCb collaboration for the 2018 major upgrade of the Vertex Locator (VeLo).

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1. Introduction

When designing thermal management systems for tracking detectors, the following three points should be addressed:

a. Minimization of the material budget,
b. Enhancement of the cooling power for a given material budget, and
c. Minimization of the temperature difference between heat source and heat sink.

Moreover, integration aspects of on-detector cooling systems should be evaluated very early in the design stage of the detector [1]. "The cooling has to be considered as an integral part of the detector and the experiment, therefore physicists and engineers shall collaborate from the beginning of the conceptual design of the systems, with an overall view on all subparts" [2].

This paper gives an overview of two approaches that are being pursued by the CERN PH-DT group in collaboration with experiments for the integrated cooling of silicon tracking detectors. They are schematically represented in Figure 1. The first approach consists in thermally interfacing a light cold plate with a high thermal conductivity and embedded cooling pipes to the backside of the readout electronics in order to dissipate the heat produced by the electronics and to maintain the detector at the desired temperature (see Figure 1(a)). The temperature difference, ΔT, between the heat source (readout electronics) and the heat sink (cooling pipes) for a power dissipation of 1 W/cm^2 is of the order of 10ºC. This is lower than the systems with metal pipes and thermal ledges that are currently installed in the LHC where typically the ΔT is about 15ºC [3]. Further reduction of this ΔT can be obtained by replacing the cold plate and pipes with a thin silicon plate with arrays of microchannels embedded within (see Figure 1(b)). Such a plate provides an active cooling distributed, partially or completely, underneath the surface of the electronic chips with very low material budgets of the order of 0.1% X_0. In this case, the thermal path is minimized and the ΔT can be as low as 5ºC. Moreover, by cooling silicon detectors with silicon microchannel plates no thermal stress is generated by eliminating any mismatch between the Coefficient of Thermal Expansion (CTE) of the heat source and the CTE of the heat sink.

These novel on-detector silicon microchannel cooling systems are based on the thermal management approach introduced in 1981 by Tuckerman and Pease [4] for integrated circuit chips. Their use for particle detectors and associated read-out electronics has been reported for the first time in 2011 [5].

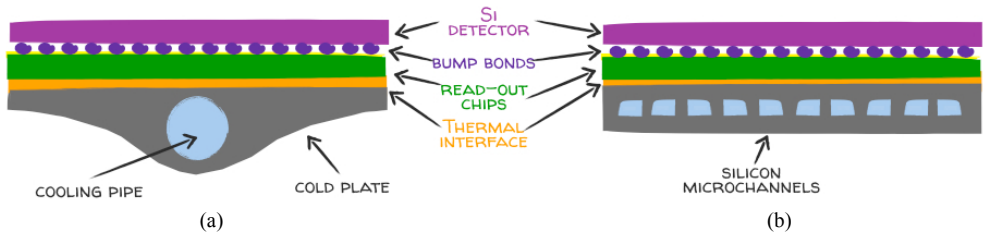

Figure 1 – Schematic representation, not to scale, of (a) a cold plate with an embedded cooling pipe and (b) cooling microchannels embedded in a silicon substrate thermally interfaced to the backside of the read-out chips of a silicon detector.

2. Integrating cold pipes and microchannels in light support structures for the upgrade of the ALICE Inner Tracking System

During the major upgrade programme of the ALICE detector [6] scheduled in 2018, a new silicon tracker detector, consisting of 7 concentric cylinders will replace the current Inner Tracking System (ITS) [7]. The new ITS will cover a region from 22 mm up to 450 mm radial distance from the Interaction Point (IP). Because of the high track density close to the IP, the three most inner layers must be equipped with high granularity pixel detectors. Monolithic pixel detectors are considered as the baseline technology for the new ITS [8]. These CMOS chips integrate in a single silicon die, the detection volume and the readout. The expected power dissipation ranges from a nominal value of 0.3 W/cm^2 to a maximum value of 0.5 W/cm^2. Owing to the relatively low radiation level in the inner region, the ITS can operate at room temperature. However, it must be maintained above the dew point of the experimental hall (about 15ºC) to avoid condensation. Moreover, for performance requirements, the temperature of the detector should be kept below 30ºC with a maximum gradient over the detection area of 5ºC. To meet these requirements and to minimize its mass, the cooling system is embedded in the mechanical support structure of the staves.

Three alternatives are being explored for the thermal management of the Inner Barrel Stave while for the Outer Barrel Stave a single solution is carried out. The baseline solution for both the Inner Barrel Stave and the Outer Barrel Stave is composed of a so-called Space Frame, which is a light carbon fibre structure providing the mechanical support and the necessary stiffness of the staves, and a single Cold Plate or two Cold Plates respectively, each with two plastic cooling pipes (see Figure 2).

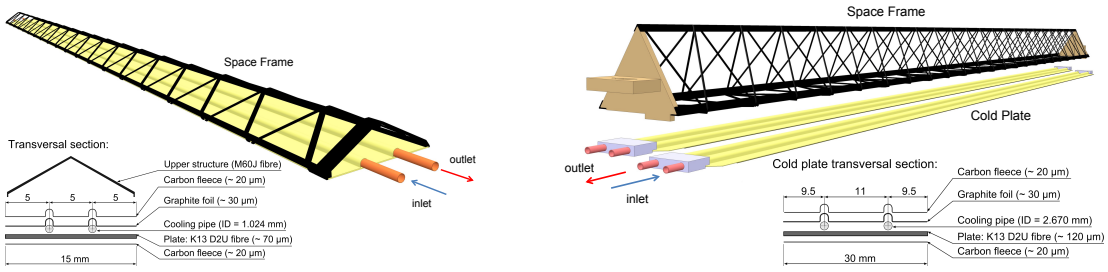

Figure 2 - Schematic layout of the mechanical and cooling structure of the (a) Inner Barrel staves and (b) Outer Barrel staves [7].

Two alternative cooling options to the Cold Plate with embedded pipes are being explored for the Inner Barrel Stave. They are based on a network of microchannels embedded either in a polyimide substrate [9] (see Figure 4) or in a silicon frame [10] (see Figure 3).

In order to minimize the material budget contribution of the cooling system, the silicon frame configuration eliminates any material contribution in the detection region while keeping all the advantages of microchannel cooling. This configuration relies on the thermal conductivity of the monolithic pixel detectors to reach the desired temperature in the central area of the sensors.

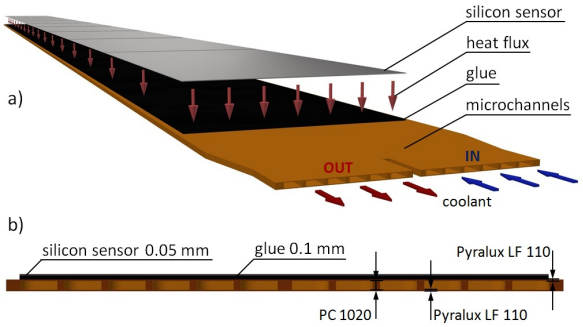

Figure 3 – (a) Sketch of the polyimide cooling system interfacing silicon sensors and (b) schematic view of the polyimide microchannels cross section [7].

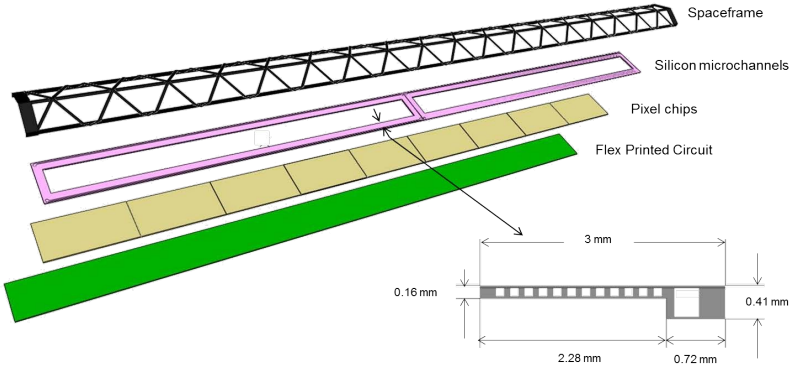

Figure 4 - Integration concept of the silicon microchannel frames into the ITS Inner Layers staves [7].

The first silicon cooling frames were fabricated on 380 µm thick 4" silicon wafers in the class 100 (ISO 2) Micro-Electro-Mechanical Systems (MEMS) cleanroom at the EPFL-CMi Center of MicroNanotechnology (CMi) [11] by PH-DT [12] in close collaboration with ALICE and the Microsystems Laboratory EPFL-LMIS4 [13]. The fabrication process was similar to the one implemented for the NA62 devices (see Figure 10), with the difference that in this case the central area was not thinned but it was completely removed and the microchannels were confined at the sides of the chip. The silicon frame was then equipped with 100 µm thick dummy silicon chips simulating the power dissipation of the pixel chips. The system was extensively tested with R1234ze flow boiling [14] and it demonstrated its ability to remove the power dissipation expected for the ITS chips (of the order of 0.3 W/cm^2) while maintaining the sensor below 30ºC with a maximum temperature gradient over the sensor area of the order of 5ºC (see Figure 5) as required by operational constraints.

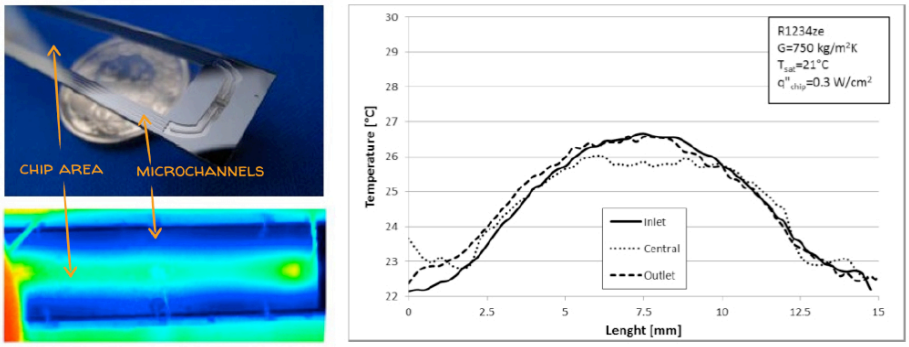

Figure 5 - The first prototype of silicon frame with embedded microchannels (top left), radial temperature profiles at three different locations along the microchannels (right plot) resulting from the IR image (bottom left) for a power dissipation on the chip area of 0.3 W/cm^2.

The cooling frames are fabricated with standard microfabrication techniques on silicon wafers. The maximum length of the frames is limited by the diameter of the wafers. In order to reach the length of the future ITS inner layers (270 mm), several frames need to be interconnected.

A first prototype of full stave cooling system was assembled with frames fabricated on 4" silicon wafers (see Figure 6). In this case, 4 devices need to be interconnected. Since one of the design requirements is to have the fluidic inlet and outlet on the same side and given the integration and space constraints, the fluidic supply and return lines are also embedded in the silicon frame (see Figure 7).

Figure 6 - The first prototype of full stave cooling system with silicon frames with embedded microchannels and distribution lines (top picture) equipped with 9 15x30 mm 100 µm thick silicon dummy chips (bottom picture).

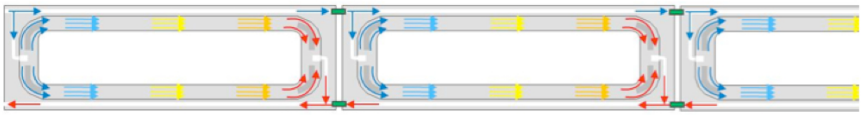

Figure 7 - Interconnection scheme of several frames for the full-stave cooling prototype.

The continuation of the two distribution lines at the edge between one frame and the following is obtained through a microfluidic bridge fabricated in the same wafer as the silicon frames. At the end of a single device, the distribution line stops and the fluid is forced to go out

orthogonally (see Figure 8). At this point the fluid enters in the micro-bridge and is then directed to the beginning of the distribution line in the following frame.

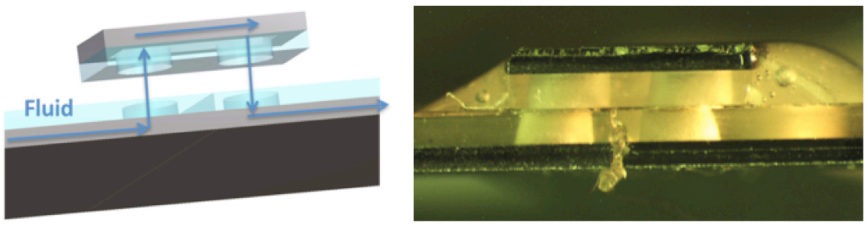

Figure 8 - The micro-bridge developed for the interconnection of several frames in the final-stave prototype. The prototype shown here consists of Si-glass chips. The final micro-bridge will be made entirely of silicon.

In collaboration with the Thai Micro Electronics Center (TMEC) [15] in Bangkok, PH-DT and ALICE are currently developing a new ultra-thin prototype on 6" wafers. This will allow having only 2 frames to cover the entire stave length, instead of 4 as it is the case now with 4" wafers. This will also reduce the number of interconnections from 3 to 1. Figure 9 shows the integration of both alternatives in the Space Frame with the pixel detectors and the flex cable.

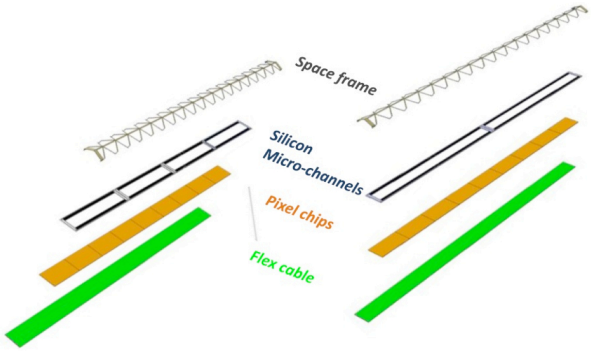

Figure 9 - Integration of the silicon microchannel cooling system into the ITS inner layer stave with 4 silicon microchannel frames (4" wafer) and 2 microchannel frames (6" wafer).

3. Ultrathin silicon cooling plate for the NA62 GigaTracKer

The thermal management of the NA62 GigaTracKer pixel detectors (GTK) is achieved by means of a thin silicon plate with embedded microchannels in which liquid C_6F_{14} is circulated [16]. In this case, the silicon cooling plate is also the support structure for the detectors. NA62-GTK tracker will be the first High-Energy Physics detector in which such a microfluidic system will be installed. This system has been demonstrated to satisfy the very stringent requirements in terms of material budget and cooling performance of the GTK. A total power of about 48 W is expected to be unevenly distributed (the digital part at the periphery of the TDCPix will dissipate more power than the central analog region) on a 60 mm x 40 mm area. The silicon cooling plate guarantees stable operation at temperatures below 0ºC with a temperature gradient of no more than 5ºC at the surface of the detector.

The microfluidic circuit design consists of 154 straight parallel channels, with a rectangular cross-section of 200 µm x 70 µm, embedded in a silicon substrate with a thickness of the order of 130 µm. The design was validated with prototypes built by PH-DT in the EPFL-CMi cleanroom in close collaboration with the EPFL-LMIS4 Laboratory [17]. After the thermo-fluidic characterisation of these prototypes, six devices from a pre-production run were shipped to CERN from IceMOS Technology [18]. They performed all the fabrication steps of the process up to the etching of the microfluidic openings (see Figure 10 (a)-(c)) while all the subsequent manufacturing operations were performed by PH-DT at CMi.

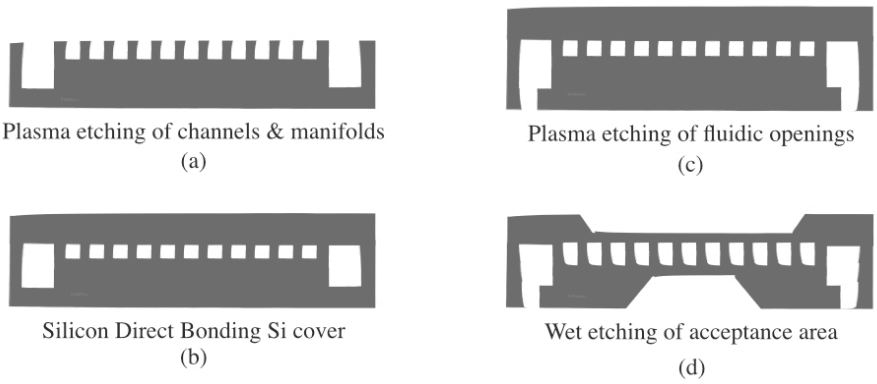

Figure 10 - Microfabrication process-flow of silicon cooling plates for the NA62-GTK pixel detectors. (a) 70 µm deep microchannels and 280 µm deep distribution manifolds are etched in a 380 µm thick 4" Si wafer. (b) A 310 µm thick Si wafer is bonded to the etched wafer to close the microchannels and manifolds. (c) Inlets and outlets are etched on the backside of the first wafer to open the microfluidic circuit. (d) The cooling plate is thinned to 130 µm in the acceptance area.

4. Evaporative CO_2 in silicon microchannels for the upgrade of the LHCb Vertex Locator

The last application presented in this paper is the in-vacuum, silicon microchannel cooling system with evaporative CO_2 developed for the pixel modules of the of the LHCb Vertex Locator (VeLo). In the context of the 2018 upgrade programme of the LHCb experiment [19], the VeLo detector will be replaced. With the current VeLo, the LHCb collaboration has pioneered the use of evaporative CO_2 cooling for particle detectors [20]. The upgraded detector modules of the VeLo will be placed only few mm away from the LHC beam and will be subject to very intense radiation levels. To be robust against radiation damage, the sensors will have to be maintained at a temperature below -20ºC. The active electronics of the detector modules is expected to dissipate about 2 W/cm^2 over a surface of 2.8×4.2 cm^2 per each half of the 42 detecting planes, with an estimated power dissipation in the detector volume close to 2 kW. The present cooling configuration relies on evaporative CO_2 in metal pipes connected to the modules periphery by thermal ledges. The approach for the thermal management of the upgrade is to replace these pipes and thermal ledges by silicon microchannel cooling plates still operating with two-phase CO_2 as coolant [21]. 400 µm thick silicon microchannel prototypes have been fabricated and successfully tested at temperatures down to -30ºC and pressures greater than 160

bars. Like for the NA62-GTK, the silicon microchannel cooling plates of LHCb hold the pixel detectors in position in the final assembly (see Figure 11(b)). The serpentine-like design of the channels embedded in the L-shaped cooling plates shown in Figure 11(a) allows to efficiently cool the 6 ASICs on each half module.

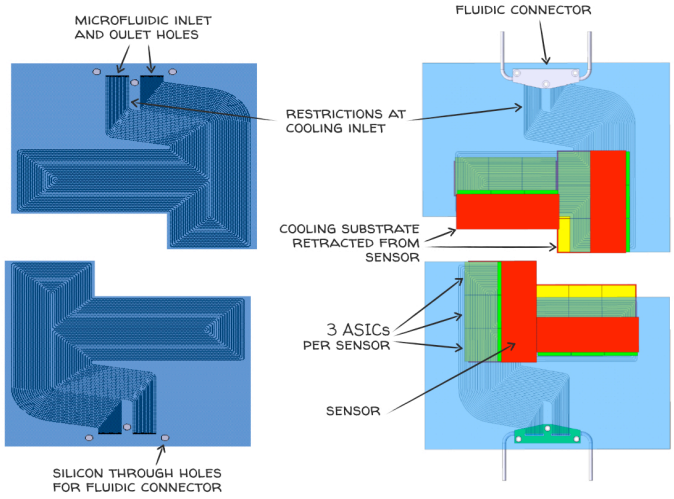

Figure 11 – Schematic representation of (a) 2 bare L-shaped cooling substrates and (b) 2 L-shaped cooling substrates equipped with 2 detector modules each. A single detector module consists of 1 detector and 3 ASICs.

Several thermo-fluidic tests were performed at CERN using rectangular samples with an embedded microchannel network. Silicon chips with resistive lines were glued to these samples to simulate the heat dissipated by the electronics. The outcome of the tests performed in a vacuum vessel using the TRACI CO_2 cooling plant [22] indicate that the VeLo upgrade sensors can be kept well below -20ºC with CO_2 inlet temperatures of the order of -30ºC [22].

5. Conclusions

Recent developments at CERN have demonstrated the integrability of low mass on-detector cooling systems to silicon tracking detectors. Light materials with high thermal conductivities can be integrated to mechanical structures and provide the required cooling efficiency.

A great effort is currently being carried out by the CERN PH-DT group in close collaboration with experiments to develop networks of microchannels embedded in thin silicon plates to be used as single-phase or two-phase cooling systems. The NA62-GTK has adopted such a solution with liquid C_6F_{14} where the silicon microchannel cooling plate is also the mechanical support for the tracking detectors. LHCb relies on a similar solution with evaporative CO_2 circulating in a silicon microchannel cooling plate for the 2018 major upgrade of the VeLo detectors. In the same context, ALICE is investigating three alternatives for the ITS (*i.e.* a Cold Plate with cooling pipes, polyimide microchannels and silicon microchannels). The three options rely on light carbon structure in which the cooling system is integrated.

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