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Upgrading the ATLAS Tile Calorimeter electronics

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The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment at LHC. Its main upgrade will occur for the High Luminosity LHC phase (phase 2, which is foreseen for 2022-2023), when the peak luminosity will increase 5-fold compared to the design luminosity ($10^{34} cm^2 s^{-1}$) at a proton beam energy of 7 TeV. An additional increase of the average luminosity with a factor of 2 can be achieved by luminosity leveling. The upgrade aims at replacing the majority of the on- and off-detector electronics so that all calorimeter signals are digitized and sent by optical fiber to the off-detector electronics in the counting room. To achieve the required reliability, redundancy has been introduced at several different levels. Three different options are presently being investigated for the front-end electronic upgrade. Which one to use will be decided after extensive test beam studies. 10 Gbps optical links are used to read out all digitized data to the counting room while 5 Gbps down-links are used for synchronization, configuration and detector control. For the off-detector electronics, a pre-processor is being developed, which takes care of the initial trigger processing while temporarily storing the main data flow in pipeline and de-randomizer memories. One demonstrator prototype module with the new calorimeter module electronics, but still compatible with the present system, is planned to be inserted in ATLAS this year, i.e. mid 2014 (at the end of the phase 0 upgrade).

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1. Introduction

The ATLAS (A Toroidal LHC ApparatuS) [1] experiment is a general purpose detector, installed along the Large Hadronic Collider (LHC) at CERN, designed for precision Standard Model measurements and search for physics beyond the Standard Model. In order to perform those measurements, it is composed by 6 different subsystems: The Inner Detector, the Solenoidal Magnet, the Electromagnetic and Hadronic Calorimeters, the Toroid Magnets and the Muon Spectrometer. Each subsystem is showed in Figure 1.

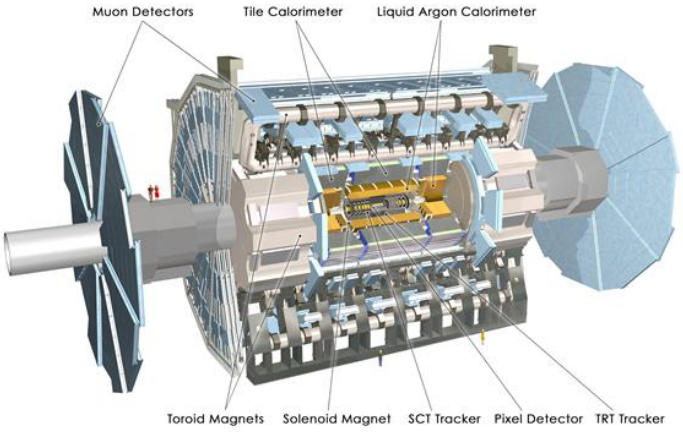

Figure 1: The ATLAS detector and its subsystems.

In the most central region of ATLAS, covering $|\eta| < 1.7$, the Tile Calorimeter [2] (TileCal), one of the Hadronic Calorimeters of ATLAS, is located. With the shape of a hollow cylinder, it is mechanically divided in a central barrel, known as Long Barrel (or LB) and two extended barrels (EBA and EBC). Each of these partitions is partitioned in azimuthal angle by 64 wedge-shaped modules. While it is mechanically a single structure, the central barrel electronics are split in two partitions (LBA and LBC).

TileCal functionality is based on a sampling technique where plastic scintillator plates (tiles) are embedded in a steel absorber structure. When high energy particles cross those steel plates, this interaction generates showers of lower energy particles which in turn interacts with the plastic scintillators generating light that is collected and transmitted through wavelength shifting (WLS) fibers to the outermost region of each module, where the photomultipliers (PMT's) are located.

The signal obtained by each PMT is proportional to the energy deposited in a certain region of plastic and steel plates, referred to as a TileCal cell. Each cell is read-out from two sides by two different PMT's, giving one level of redundancy on the cell energy measurement. In total, TileCal has 9852 PMT's. Figure 2 shows the structure and components of one single module.

2. TileCal Upgrade for HL-LHC Scenario

A significant increase in the LHC luminosity is expected for the next years of operation. It is scheduled for 2023 (so called "Phase II"), with a peak luminosity of $5.10^{34} cm^2 s^{-1}$ at a proton beam

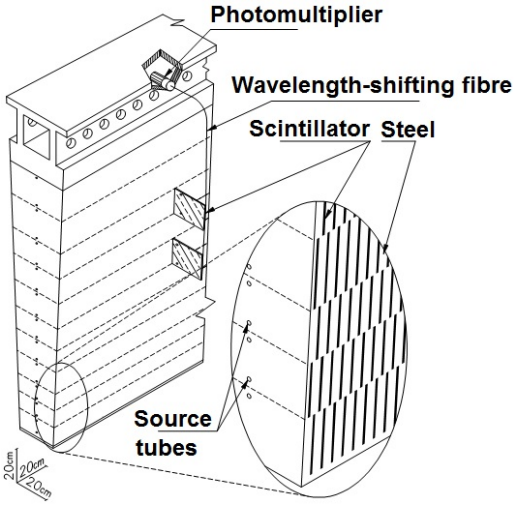

Figure 2: TileCal module components and structure.

energy of 7 TeV); this luminosity is 5 times bigger than the TileCal current system was designed for. Moreover, this new operational condition implies in a higher radiation tolerance level requirement for the components installed in the detector. By the time of Phase-II, the current electronics will have reached their maximum total integrated radiation dose. Finally, another requirement for the upgrade is the usage of a full-digital trigger system with a bandwidth of up to 80 Tbs (the current TileCal trigger output for the Level-1 is analog).

Additionally, new features and read-out strategies are going to be implemented in the TileCal front-end and back-end electronics. In summary, the purpose of the upgraded design is to perform a full digitalization of signals and full transmission to off-detector electronics at the bunch-crossing rate, reduce the single point failures by adding redundancy to power distribution and to the read-out path, and the usage of protocols with error correction for data transmission.

2.1 Current Electronics Architecture Versus Proposed New Architecture

2.1.1 Current Electronics

In the outermost region of each TileCal module is located the front-end (or on-detector) electronics. The first step of that electronic chain is the PMT, which generates an electrical signal that is proportional to the energy deposited by a high energy particle in a TileCal cell. This signal is transmitted to the 3-in-1 cards (front-end boards - FEB) where the analog signal is amplified, shaped and sent to two detector outputs, one with a gain of 64 and another of 1. An additional output from the 3-in-1 cards, at the low gain, is summed into towers for the Level-1 Trigger.

The next step in the front-end chain is in the Digitizer Boards, where the two detector outputs are digitized at 40 MHz by 10 bit Analog to Digital Converters (ADC). Finally, all signals from a TileCal module are merged and formatted into packages, in the Interface Boards, to be sent through high speed optical links to the back-end (or off-detector) electronics.

The first stage of the off-detector electronics is the Read-Out Driver (ROD). They receive the on-detector data in a rate of 100 kHz and perform data processing tasks to send the data to the

Read-Out Buffers in the Level-2 trigger. In figure 3 is shown a diagram of TileCal read-out current architecture.

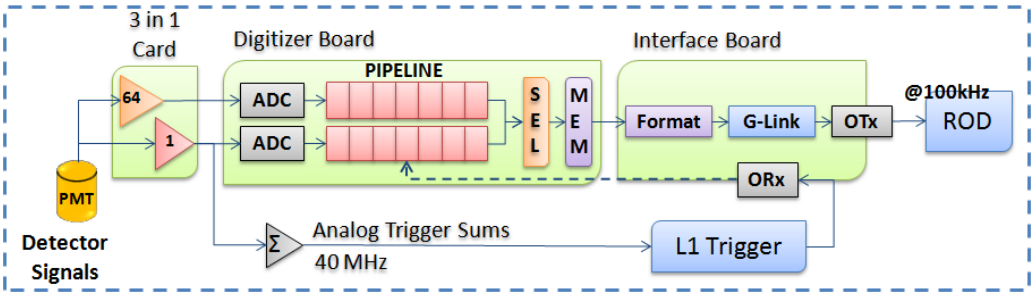

Figure 3: TileCal current electronic architecture.

2.1.2 Proposed New Architecture

The main concept of the Tile Calorimeter electronics is not going to change for the HL-LHC scenario, but several new features are going to be added to the electronic chain. Figure 4 shows a diagram of the proposed new architecture.

First of all, the higher event rate implies a higher current in the PMT's voltage dividers, requiring new high voltage power supplies and PMT dividers. The PMT signals are shaped and amplified by frontend boards. At this point, there are three different new boards under evaluation for Phase II.

Front-End Boards: The first option for being the new FEB is a modified version of the current 3-in-1 card [3], but with better linearity and lower noise, being developed by the *Enrico Fermi Institute* (University of Chicago). It is composed of discrete components and can provide two different analog outputs with different gains, besides having calibration capabilities.

The second possible FEB for the new TileCal electronic architecture has been developed in joint collaboration between the Argonne National Laboratory (ANL) and Fermilab. It is a custom ASIC that includes a version of the Charge Integrator and Encoder (QIE) [4] chip. It has the capability of splitting the PMT output signal into four different ranges (16/23, 4/23, 2/23, 1/23), followed by a gated integrator. In addition, it also has a 6-bit ADC that digitizes the selected range.

The Front-End for Atlas TileCal Integrated Circuit (FATALIC) [5] is the third option. Designed at Laboratoire de Physique Corpusculaire in Clermont-Ferrand (LPC), it combines the FATALIC shaper/amplifier with "Twelve bits AdC for s-atlas Tilecal Integrated Circuit" (TACTIC) in a ASIC solution and includes a multi gain 3-gain current conveyor (CC) associated with a shaping stage.

Main Board: The output signals coming from the FEB's are sent to the Main Board, where they are digitized (depending on the FEB chosen for Phase II), serialized, and sent to a high-bandwidth Daughter Board. In addition, the Main Boards are able to control and monitor the FEB and the low voltage power supply of the front-end electronic.

The final version of the Main Board is going to rely on the FEB chosen for Phase II, but the first prototype is compatible with the modified 3-in-1 card, was designed by the *Enrico Fermi Institute* (University of Chicago) and is equipped with 4 Altera Cyclone IV FPGAs, 12-bit Linear Technology LTC 2264 ADCs and hosts up to 12 modified 3-in-1 cards.

Daughter Board: For the interface between the on- and off- detector electronic in the new TileCal electronics architecture is going to be used the Daughter Board [6]. Its main function is to collect the digital data coming from the Main Boards, format it and transmit the data to the sROD, but adding redundant high speed links. In addition, it implements the Detector Control System (DCS) commands for controlling the high voltage power supplies.

The Daughter Board is already in the third version and is being developed by Stockholm University. The most recent version is equipped with 2 Xilinx Kintex 7 FPGAs, two Quad Small Form-factor Pluggable (QSFP) optical modules and two GBTx chips.

Super Read-Out Driver: The Super Read-Out Driver (sROD) [7] is the first element of the new back-end electronic chain. Basically, it is going to be responsible of processing the received data from the front-end electronics and sending it to the trigger system. In addition, should be capable of distributing the Trigger and Timing and Control (TTC) to the on-detector electronics. Instituto de Física Corpuscular (IFIC) - CSIC and Universidad de Valencia (UV) is developing the sROD.

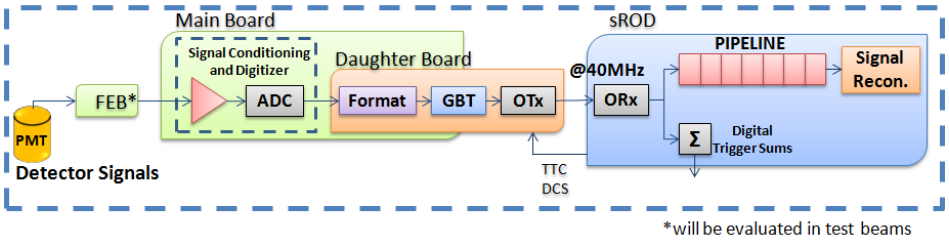

Figure 4: TileCal proposed electronic architecture for upgrade.

2.2 The Demonstrator Project

The LHC is going through the first long shutdown (LS1), where everything is being prepared for the new operational conditions during the next 2 years of data taking. Considering the complexity of the proposed new TileCal electronic architecture, and given the accessibility to the ATLAS detector during this shutdown, we aim to install a prototype "demonstrator" unit in the detector during LS1. The tile Demonstrator [8] is a hybrid drawer that combines features of the current system, such as the analog trigger path, with future read-out requirements. This project aims to evaluate and qualify the proposed new electronics before a complete replacement for Phase II. Figure 5 shows a diagram with the demonstrator architecture.

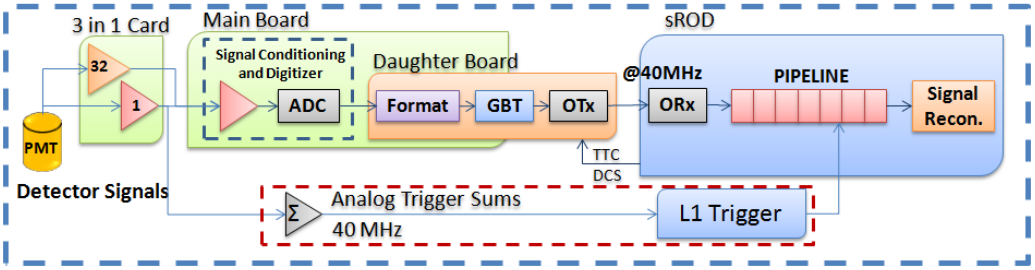

Figure 5: TileCal Demonstrator architecture.

3. Conclusions

The new operational conditions expected in the next years of the LHC, with higher radiation levels and data rates, require a complete redesign of the read-out electronics of the Tile Calorimeter. The upgrade plan is to develop a system with full digitalization of signals and transmission to the off-detector electronics at bunch-crossing rate, with a reduced number of possible single points of failure, higher radiation tolerance and higher redundancy on the read-out path and in the power distribution.

Such an extensive redesign requires advance field testing. To this end, we have built a hybrid TileCal Phase-II Demonstrator, which combines current features, like the analog path with the other requirements for Phase II.

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