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Total Ionization Damage Compensations in Double Silicon-on-Insulator Pixel Sensors

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We are developing monolithic pixel sensors based on a 0.2 μm fully-depleted Silicon-on-Insulator (SOI) technology. SOI sensors have properties such as high-speed operation, low-power dissipation, and SEU/SET immunity. The major issues applying them in high-radiation environments are the total ionization dose (TID) effects. The effects are rather substantial in the SOI devices since the transistors are enclosed in the oxide layers where generated holes are trapped and affect the operation of the near-by transistors. Double SOI sensors that provide an independent electrode underneath the buried oxide (BOX) layer have been developed. A negative voltage applied to this electrode is expected to cancel any positive potential due to hole traps in the BOX layer. We have irradiated transistor test elements and pixel sensors with γ-rays. By adjusting the potential of this electrode, the TID effects are shown to be compensated. The transistors irradiated to 2 MGy recovered their performances by applying a bias to the electrode. The transistors showed to have modest differences in behaviors of TID compensations according to their types. The pixel sensor irradiated to 100 kGy recovered its functionality by applying a bias to the electrode. The radiation tolerance of the SOI devices has been substantially improved by employing the innovative double SOI.

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1. SOI Pixel Device

The potential of novel monolithic pixel devices utilizing a 0.2 μm fully depleted silicon-on-insulator (FD-SOI) technology has been intensively explored for various applications including high-energy, space, γ/X-ray imaging, and other applications[1][2][3][4]. As the technology characteristics of our SOI pixel devices, we adapt "bonded"-wafers provided by SOITEC Co.[5] and utilize the commercial reliable process by Lapis Semiconductor[6]. SOI bonded wafers were fabricated from two silicon wafers with optimized resistivities. Separated by a 200 nm thick buried oxide (BOX) layer, nominally the active layer is 40 nm thick silicon of 18 Ωcm used as the circuit part, and the handle wafer is 50$\sim$500 μm thickness of 700$\sim$25k Ωcm resistivity used as the sensing part. Table 1 summarizes the main characteristics of the Lapis FD-SOI process, and typical silicon types and resistivities.

Fig. 1 shows schematically the structure of an SOI pixel device. Because this design does not require mechanical bump bonds, a high pixel density can be realized. Not needing the bump bonds is expected to reduce the fabrication cost substantially. The thickness and resistivity of the sensing part can be optimized per application. Low-power and high-speed operations are realized by FD-SOI, providing a large operation temperature range from less than 1 K to 630 K.

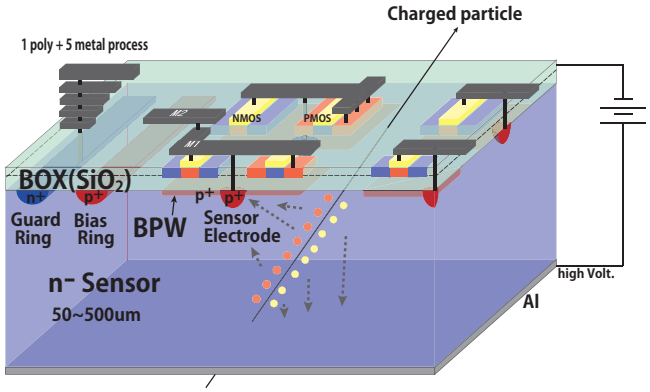

Figure 1: Schematics of SOI pixel device. Two silicon wafers are bonded interleaved with 200 nm thick buried oxide (BOX) layer. The pixel electrodes are fabricated by implantation of p or n dopants after removing the top silicon and BOX layers. The transistors are inter-connected via aluminum metal placed on top (five metal layers available). The detector bias is applied from the backplane, or from the front contact (bias ring). The BPW is to isolate the back-gate effect to the front transistor circuits.

Table 1: Lapis FD-SOI process

Process	0.2 μm low leakage fully-depleted SOI CMOS
	1poly+5metal layers, MIM(1.5 μF/μm^2), DMOS
	Core(I/O) voltage = 1.8(3.3) V
SOI Wafer	Diameter : 200 mmϕ
	Top Si : CZ (p $\sim$18 Ωcm), 40nm thick
	Buried oxide : 200 nm thick
	Handle wafer : CZ (n $\sim$0.7 kΩcm), FZ(n $\sim$7 kΩcm / p $\sim$25 kΩcm)
	Double-SOI available
Backside	Mechanical grind(down to 200 μm), chemical etching,
	implant, laser annealing, Al plating.
	Further thinning to 50,100 μm available.

We have identified three issues to solve to utilize SOI devices in high energy experiments. One is the back-gate effect where the bias voltage applied for sensor depletion affects the operation of the SOI circuit. To shield the electric-field from the bias voltage, buried p-well (BPW) electrode for p-type sensor nodes (buried n-well (BNW) for n-type sensor nodes) has been developed. However, the BPW electrode increases the sensor capacitance, hence modifies the signal response shape. An alternative option is preferable.

The second issue is the cross-talk between sensor nodes and near-by SOI circuit, which is typical in devices with a thin BOX layer.

The third is that the radiation effect is relatively complicated. The total ionization dose (TID) effect [7] is rather substantial. Each SOI transistor is fully enclosed in oxide layers. With the radiation, generated holes are trapped in BOX, and affect the operation of the SOI circuit; the transistor threshold shifts negatively [8][9][10]. Characteristics of the SOI transistor, *e.g.* the threshold, should be restorable by applying a negative voltage to the positively charged region. The developed BPW is not suitable for this purpose because the potential configuration is limited with respect to the near-by pixel node and backside potential. The BNW with n-type pixel nodes may be effective provided that the sheet resistance is low enough. Although, the additional BPW/BNW electrodes increase the sensor capacitance further more and tend to increase the coupling noise among the circuits through this common electrode.

2. Double-SOI Process

In order to solve these issues, we have developed double SOI wafers with SOITEC first in 2012. The double SOI wafer has two sets of low resistive silicon and BOX pair layers made by SmartCut technology repeated twice. The second silicon layer (SOI2) interleaved with the BOX layers is used as an individual electrode with controllable potential. A negative voltage applied to the SOI2 compensates the effect of trapped hole charge, therefore it is expected the transistor characteristics to be recovered. Also the same layer should be effective to suppress the back-gate effect and the cross-talk. The double SOI wafer we evaluated uses p-type CZ silicon (10∼18 Ωcm) for the top-side active layer (SOI1) and 80 nm-thick SOI2 layer. These two layers, SOI1 and SOI2, are interleaved with a BOX layer (BOX2), SOI2 and the handle with another 150 nm-thick BOX layer (BOX1). Fig. 2 shows TEM images from the first succeeded double SOI process.

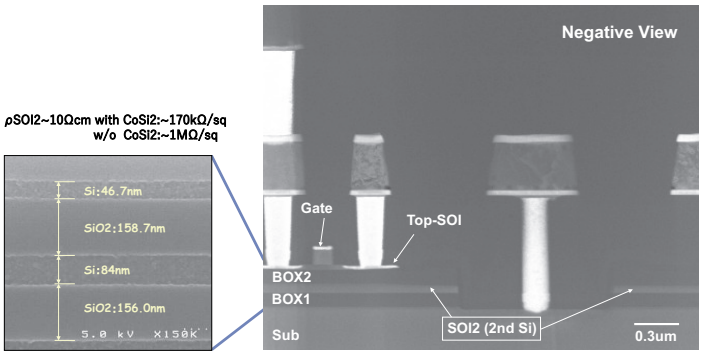

Figure 2: TEM image of the double-SOI wafer and across processed transistor and pixel node.

3. Tested Samples and Cobalt Irradiation

We evaluate the radiation damage and the compensation of TID with SOI2 using transistor-test-element-group (TrTEG) chips, TrTEG6, and integration-type pixel sensors, INTPIXh2.

TrTEG6 contains 18 transistor types each for PMOS and NMOS, as listed in Table 2. The core transistors (with oxide thickness t_{ox}=4 nm) are provided with low (LVT) and normal (NVT) threshold types, and IO (t_{ox}=7 nm) with normal (NVT) and high (HVT) threshold types. Transistors

are tested for several gate lengths and widths, with body floating (BF) or three kinds of body connections (two versions of body connected to source, S-TIE and S-TIE2, and one with voltage applicable externally, MULTIB-TIE).

INTPIXh2, with pixel size of 18 μm square, has an on-pixel circuit as shown in Fig. 3. The pixel outputs in the same column are sent out one after the other to a 12-bit ADC located outside the chip. Since the irradiation was performed on a chip by chip basis, the functionality of the on-pixel circuits together with a common on-chip peripheral circuit including output buffers and switching logics was evaluated all together. The tested version has SOI2 layers to which only a single voltage can be applied, therefore fine voltage tuning between *e.g.* PMOS and NMOS transistors was not possible.

Table 2: Tested transistors. M is the number of transistors connected in series, giving the effective transistor width as W$\times$M.

No.	L[μm]	W[μm]	M	COMMENT
0	0.20	5	4	NVT_BF
1	0.50	5	10	NVT_BF
2	1.00	5	20	NVT_BF
3	0.20	5	4	LVT_BF
4	0.50	5	10	LVT_BF
5	1.00	5	20	LVT_BF
6	0.35	5	7	IOHVT_BF
7	0.35	5	7	IOHVT_BF
8	0.20	5	4	LVT_S-TIE
9	0.50	5	10	LVT_S-TIE
10	1.00	5	20	LVT_S-TIE
11	0.40	10	4	NVT_S-TIE2
12	0.60	6	10	NVT_S-TIE2
13	1.00	5	20	NVT_S-TIE2
14	0.20	5	4	NVT_MULTIB-TIE
15	0.50	5	10	NVT_MULTIB-TIE
16	1.00	5	20	NVT_MULTIB-TIE
17	1.00	5	20	IONVT_S-TIE

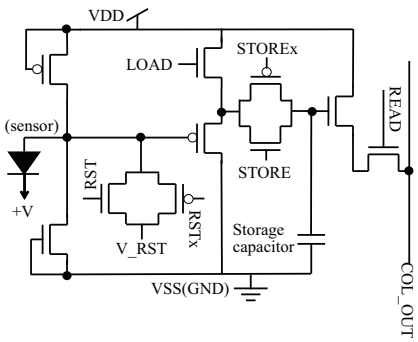

Figure 3: INTPIXh2 on-pixel circuit

TrTEG chips and INTPIXh2 sensors were irradiated with ^{60}Co γ-rays at Takasaki Advanced Radiation Research Institute, JAEA. The total dose ranged from 3 kGy up to 2 MGy for TrTEG6 chips, and up to 100 kGy for INTPIXh2 sensors. All samples were grounded and kept at room temperature during the irradiation. The irradiation time was typically 20 h (up to $\sim$200 kGy for TrTEG6, $\sim$20 kGy for INTPIXh2) or 200 h ($\sim$2 MGy for TrTEG6, $\sim$100 kGy for INTPIXh2). The samples were brought to University of Tsukuba in four hours at room temperature, then kept at -20 $^{\circ}$C in the refrigerator except during the measurements.

4. Transistor Performance

The transistor characteristics were evaluated through I_D-V_G curves, which were measured at V_D = 1.8 V, V_S = 0 V for NMOS, V_D = 0 V, V_S = 1.8 V for PMOS with V_{BPW} grounded, V_{BACK} floating, and V_B = V_S for MULTIB-TIE types. The I_D-V_G curves shift negatively with increasing dose due to trapped holes. Therefore NMOS transistors become always ON after a high enough dose. We define the threshold voltage as V_G at I_D=100×W/L [nA]. Fig. 4 shows threshold shifts of a typical transistor (TrTEG6 NO.10) as a function of the total dose. Also shown are the shifts with various V_{SOI2} settings. By applying V_{SOI2} properly, the threshold can be set to the pre-irradiation value up to 2MGy.

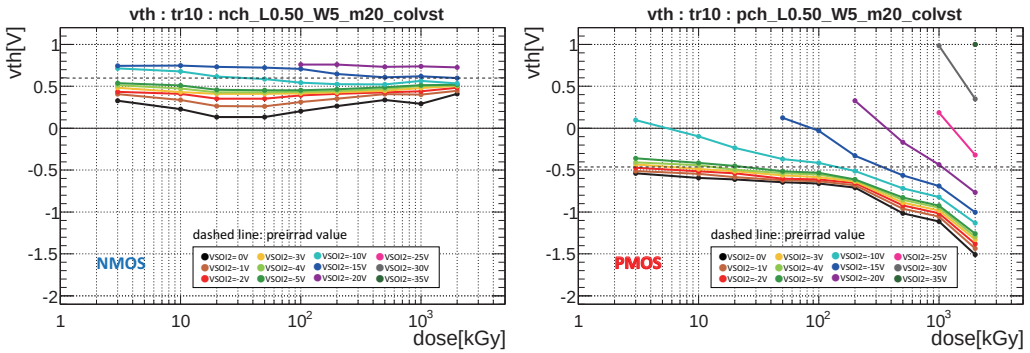

Figure 4: Threshold voltage shifts of typical (left) NMOS and (right) PMOS transistors as a function of the dose. The curves are shown for various V_{SOI2} settings. The dashed lines are the pre-irradiation values.

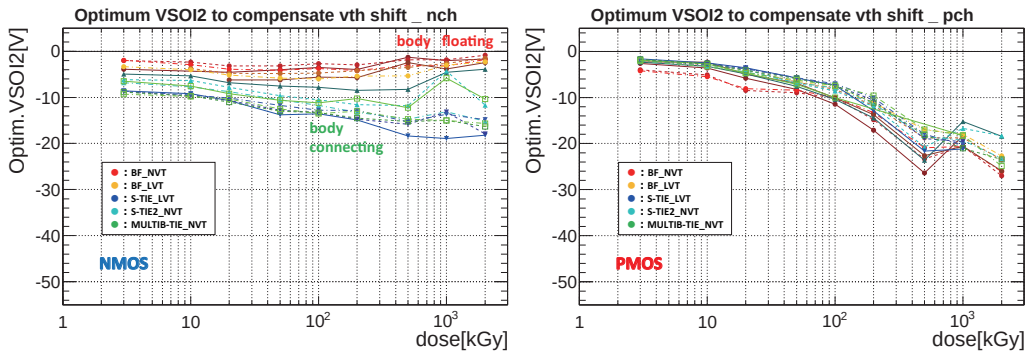

Figure 5: The optimum V_{SOI2} voltages for various types of (left) NMOS and (right) PMOS core transistors.

Considering the operation of a pixel sensor, where various transistors are incorporated, we should evaluate whether all transistors can be recovered equally with a same V_{SOI2}. Optimum V_{SOI2} is defined as the V_{SOI2} per dose and per transistor type to recover the threshold to the pre-irradiation value measured at V_{SOI2}=0 V. Here, we evaluate the optimum V_{SOI2} dependence on the core transistor types, since the dependence on the I/O transistors is relatively smaller than on the core transistors [11]. As shown in Fig. 5, noticeable differences are observed between NMOS and PMOS. Furthermore, there is a systematic difference observed among body connections notably in NMOS. The BF NMOS transistors tend to "rebound" [12] more significantly than other types.

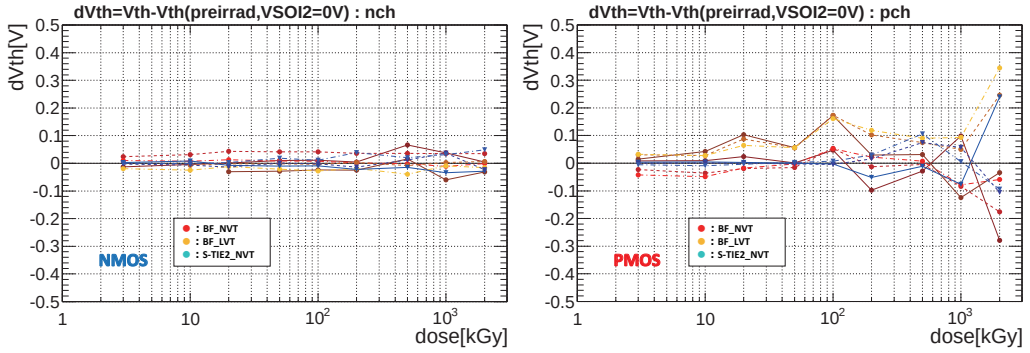

Figure 6: Compensation of the threshold voltages as a function of the dose, where four average V_{SOI2} curves (see text) are used.

Separate V_{SOI2} settings may be required to fully compensate heavily irradiated transistors for the TID. In order to demonstrate this, here we assume that four voltages are usable as V_{SOI2} for BF and S-TIE2 for NMOS, and BF and S-TIE2 for PMOS. (INTPIXh2 uses mostly S-TIE2 and BF transistors, and no S-TIE nor MULTIB-TIE.) Each V_{SOI2} dependence on the dose is the average of optimum V_{SOI2} values in the same category. Fig. 6 shows the compensation of the threshold voltage under this assumption for all the transistors. The threshold voltages are compensated to within ± 0.05 V for NMOS and ± 0.1 V for PMOS transistors. We notice that the wider variation for the PMOS is due to larger variation of the threshold voltage against V_{SOI2} at higher doses.

5. Response of INTPIXh2 Pixel Detector

The functionality of the pixel electronic, shown in Fig. 7, was examined by measuring the response to reset voltages RSTV (see Fig. 3). After 100 kGy irradiation, the output exceeds the ADC full range at V_{SOI2}=0 V for any RSTV. By applying a V_{SOI2}, the RSTV response is obtained. As the V_{SOI2} increased, the linear response range becomes wider. The dynamic range is not fully recovered at $V_{SOI2} = -10$ V. This is explained that a single V_{SOI2} is employed in the present design. At $V_{SOI2} = -10$ V, the threshold voltages of some transistors (mainly PMOS) are not fully compensated at 100 kGy, see Fig. 5. Since multiple and various transistors are involved in the circuit, the response curve is not completely back to the original one. Since the functionality as a pixel device is recovered, V_{SOI2} settings dependent on the transistor type should recover the functionality further.

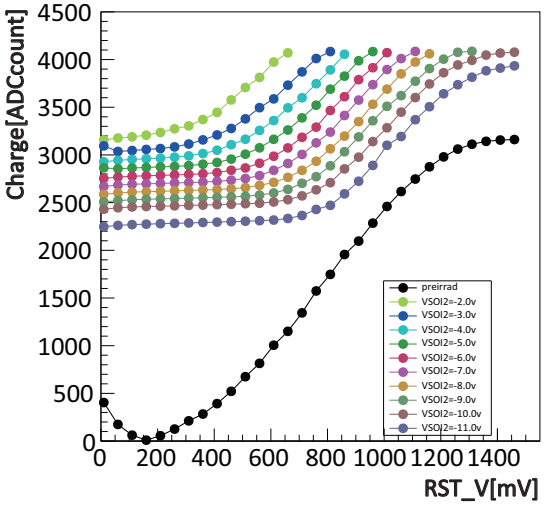

Figure 7: INTPIXh2 RSTV curves for pre-irradiation and after 100 kGy. For 100 kGy sample, the curves are taken with various V_{SOI2} values.

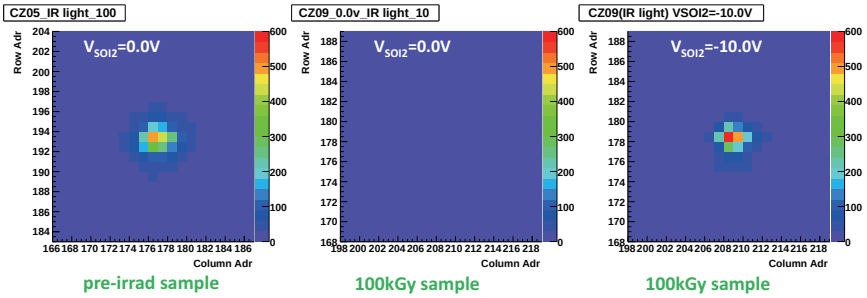

Figure 8: INTPIXh2 response to IR laser. (left) pre-irradiation, (center) after 100 kGy with $V_{SOI2} = 0$ V, and (right) after 100 kGy with $V_{SOI2} = -10$ V.

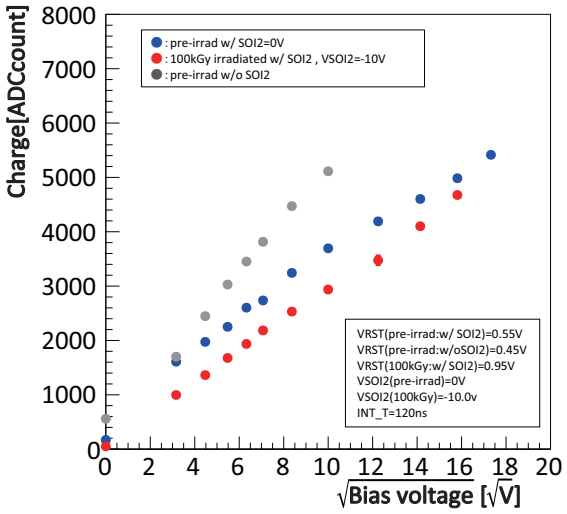

Figure 9: INTPIXh2 response to IR laser as a function of the bias voltage, for double SOI pixels before and after 100 kGy irradiation, and single SOI pixel at pre-irradiation.

After confirming the functionality of the electronics part, we measured the pixel response to an infrared (IR) laser pulse of 1064 nm wavelength and 10 ns pulse duration. The response of the sample irradiated up to 100 kGy is saturated at $V_{SOI2} = 0$ V and the image could not be obtained. By applying $V_{SOI2} = -10$ V, the image is recovered, as shown in the Fig. 8. To evaluate the response quantitatively, we plot the average ADC output as a function of the square root of the sensor bias. A linear response is obtained from the pre-irradiation sample, as shown in Fig. 9. The sample irradiated to 100 kGy showed a similar linearity at $V_{SOI2} = -10$ V. Also plotted in the figure is the linearity measured for a non-irradiated single SOI pixel device. The difference is understood as a larger detector capacitance in the double SOI devices, which leads to a slightly degraded sensitivity compared to the single SOI device.

6. Summary

We have evaluated the TID effects in the newly developed double SOI devices, demonstrating that the TID effects in the SOI transistors can be mostly compensated for by V_{SOI2} adjustment in the dose range up to 2 MGy. The optimum V_{SOI2} is found to show some modest differences among the samples, NMOS and PMOS, source-tied and body floating. Some separate values of SOI2 voltages can be optimized further to compensate for the TID effects.A design based on the obtained information is the next step to minimize the TID effects in larger dose range.

The pixel devices irradiated up to 100 kGy showed substantial recovery in response, although periodical calibration and V_{SOI2} tuning depending on transistor type are required to maintain the

original performance.

Further studies are now in progress to evaluate the compensation in the actual pixel readout read out chain. Other SOI2 issues, back-gate effect and cross-talk suppressions, are being evaluated.

In summary, the radiation tolerance has been enhanced substantially by employing the innovative double SOI. The observed differences of compensation among diffferent transistor-types are to be taken into account to design radiation tolerant devices operational in dose range exceeding 100kGy. The present study reported in this paper encourages us to work toward the realization of double SOI pixel detectors to be operational in future collider experiments.

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