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Monolithic pixel detectors fabricated with single and double SOI wafers

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Monolithic pixel detectors have been fabricated with single and double SOI wafers using SOI technology for a next-generation radiation sensor. A single SOI sensor consists of a thin SOI layer as SOI-CMOS circuit, a thick silicon substrate as a sensor, and a buried oxide layer as an insulator between two silicon layers. A double SOI sensor has another thin SOI layer to prevent unwanted effects such as the back-gate effect, the sensor – circuit crosstalk and total ionization dose effect. In 2013, the integration type pixel sensor, INTPIXh2, has been fabricated for the evaluation of single and double SOI sensors. The document describes comparison test results in single and double SOI sensors by measuring the leakage current and X-ray spectra. X-ray spectra in double SOI sensors were obtained for the first time. The problem and future prospect are discussed.

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1.Introduction

Monolithic pixel sensors using SOI technology could be among the next generation of semiconductor radiation sensor. This is because of the following features: It utilizes SOI-CMOS process and thus high speed and low noise circuits compared with bulk CMOS ones are available; No bump bonding is needed; the sensor contact area can easily be reduced to less than 1 μm resulting in high sensor gain. We have developed SOI pixel sensors since 2005 as part of the Detector Technology Project (DTP) at KEK, and we reported the performance and evaluation test results in refs. [1-4]. The SOI monolithic pixel sensor has mainly three known problems. The first is the back-gate effect in which high voltages at the back side of silicon substrate affect the behavior of transistors in the SOI layer. The second is radiation tolerance, especially the total ionization dose (TID) effect in which holes generated by radiation in the Buried OXide (BOX) layer affect the transistor performance. The third is the crosstalk between sensor and circuit. To solve these problems, we are trying several solutions. One solution is to utilize a double SOI (DSOI) wafer including two thin SOI layers. It can be developed by applying the Smart Cut^{TM} method (Soitec) twice [5]. In 2011, we developed the DSOI sensor for the first time and observed two major problems. One was the lower breakdown voltage at the edge of the bias ring due to the remaining middle SOI layer. In addition, the middle SOI layers between pixels caused a flat potential distribution affecting the charge collection efficiency. To solve these problems, a test chip named INTPIXh2 was developed in 2012. Three types of wafers, N-type Czochralski (NCZ), N-type Float Zone (NFZ) and DSOI were used to develop the INTPIXh2 sensors. We performed comparison tests using these sensors. In section 2, the design of INTPIXh2 is described. The test results of the measurement of X-ray spectra and the leakage current are presented in section 3 and 4. The problems emerging during the test and future prospects are discussed in section 5.

2. Design of INTPIXh2

The integration-type pixel sensor, INTPIXh2, was fabricated in the first multi-project wafer (MPW) run in 2012 (MX1594). Table 1 shows the specification of INTPIXh2. The pixel size is 18 x 18 μm^2 and the number of pixels is 280 (H) x 240 (V) resulting in a sensor area of 5.04 x 4.32 mm^2. The chip includes raw and column address decoders, 3 bias circuit blocks, and a column buffer array. IO pads are available on one side, and include analog buffer circuit blocks. In the process, NCZ, NFZ and DSOI wafers were utilized. The DSOI wafer was fabricated using NCZ wafers and therefore the resistivity of the substrate is the same as NCZ wafer, about 700 Ω cm. The substrate thickness of the NCZ and DSOI samples is 300 μm. The resistivity of NFZ substrate is 2-7 kΩ cm depending on process. The substrate thickness is 500 μm. Operation voltage was set to 100 V for NCZ and NFZ sensors. In the DSOI sensor, operation voltage was set to 60 V in section 3 or 100 V in section 4.

Table 1 Specification of INTPIXh2

chip size [mm^2]		6x6
pixel size [μm^2]		18x18
# of pixels		280 (H) x 240 (V)
Sensitive area [mm^2]		5.04 (H) x 4.32 (V)
sensor thickness	(wafer type)	
[μm]	NCZ	300
	NFZ	500
	DSOI	300

Fig. 1 shows the pixel circuit and Fig. 2 shows top and side views of the pixel layout. The INTPIXh2 includes 3 test pixel structures, named "r1(R1)", "r2(R2)" and "r3(R3)". The number of pixel in r1 is 280 (H) x 128(V), in r2, 128 (H) x 112 (V), and in r3, 152 (H) x 112 (V). Only pixels in r1 have a gain switch, as shown in Fig. 1, to select high or low gain mode. R2 only has Buried-N-Well (BNW) between pixels. In the DSOI, each region has different intermediate SOI shapes because the SOI below transistors can not be removed. The pixel in r1 has a large DMOS capacitor between pixels and therefore the intermediate SOI area is large, and eventually it is connected between adjacent pixels aligned vertically. R2 has the smallest intermediate SOI islands. The intermediate SOI in r1 and r2 is floating. On the other hand, the pixel in r3 has an intermediate SOI contact and therefore its potential can be controlled. The area of the intermediate SOI layer in a pixel is 14 by 14 μm. All the pixels have a Buried P-Well (BPW), which is connected to the sense node (P+), and therefore at the same potential [4].

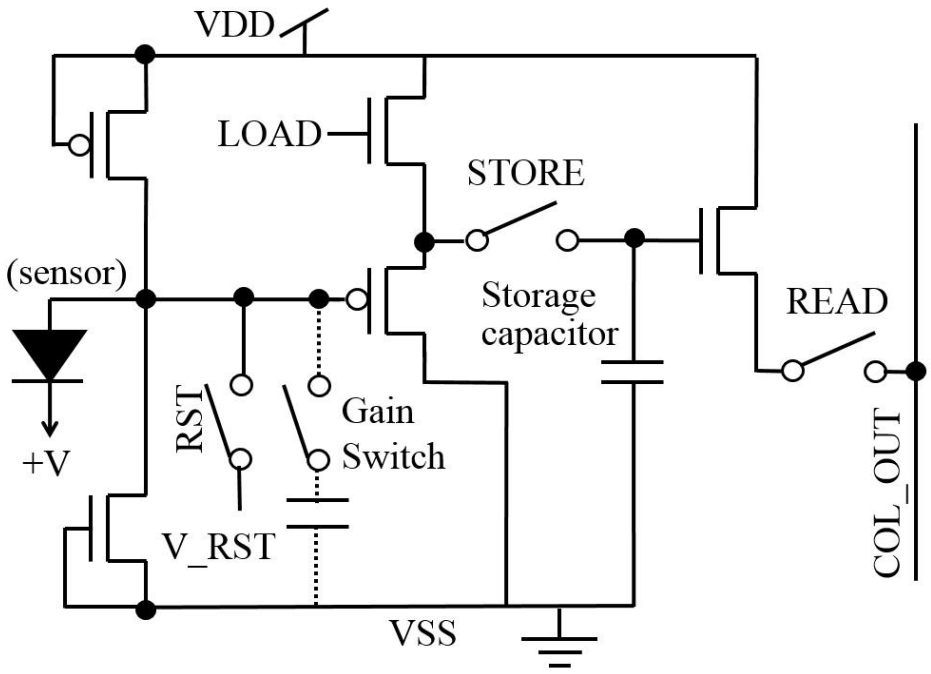

Fig. 1 INTPIXh2 pixel circuit

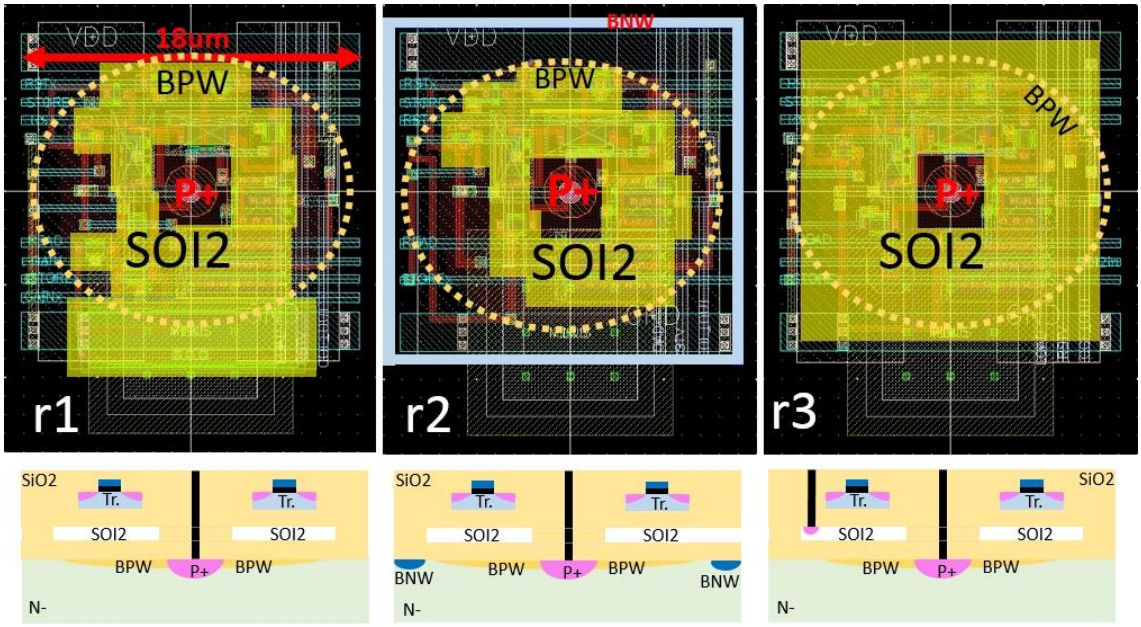

Fig. 2 Top and side views of pixels in three regions (r1:left, r2:middle, r3:right).

3. Measurement of Am-241 X-ray spectra

X-ray spectra were measured in NCZ-, NFZ-, and DSOI-INTPIXh2 using an Am-241 source. The DAQ system was put into thermostat chamber and kept in at -60 ºC. Limited pixels (100 x 100 pixels) were selected to extract the spectra. Estimated depletion depth for those is about 150 μm for NCZ-, 300 μm for NFZ-, and 100 μm for DSOI-INTPIXh2, respectively. X-ray was measured in 1 msec per frame, and accumulated 20000 frames, for a total irradiation time of 20 sec. Am-241 source with 4 MBq was used. Fig. 3 shows an X-ray spectrum in region 3 of NFZ-INTPIXh2. Energies of measurable X-rays are 13.95, 17.75, 20.78, 26.34, and 59.45 keV. With such a thin silicon thickness of SOI sensors, it is difficult to identify the 26.34 keV X-ray peak in some regions. Therefore part of X-ray peaks were utilized to evaluate the sensor gain. Fig. 4 shows X-ray spectra for the 3 regions of the NCZ-, NFZ- and DSOI-INTPIXh2 samples. Cluster size distributions are also shown. Fig. 5 shows the sensor gain curves in each wafer and each region. The features of sensors in each wafer were the following:

(1) In the NCZ-INTPIXh2, the energy resolution in r1 and r3 was good. Sensor gain was high in r2. Pixels in r3 showed the best performance because both of the energy resolution and the sensor gain was good. The sensor gain was low in r1 probably because it has an additional leak path for gain switch. The energy resolution was not good in region 2 probably because there is BNW between pixels.

(2) In the NFZ-INTPIXh2, the energy resolution was good for all the regions. Cluster size was relatively large probably because the NFZ wafer was thick. Because the NFZ wafer had high resistivity, the 59.45 keV X-ray peak was clearly observed. Sensor gain was low compared with NCZ sensors in r2 and r3. This means the probability of recombination is slightly high in NFZ wafer partly because the electric field is weak when applying the same voltage at the back side of wafer. The reason

might also be related to wafer fabrication process. The difference of sensor gain between regions was found to be small.

(3) In the DSOI-INTPIXh2, specific features were seen in each regions. In r1, the sensor gain was very low. As explained in section 2, the middle SOI layer between pixels might cause a flatness of potential and therefore a part of generated charges is trapped in a small region between pixels. In r2, the spectrum shape was almost the same as NCZ-INTPIXh2. The gain was not decreased because the middle SOI area is small, as shown in Fig. 2, and there are BNW between pixels. In r3, the sensor gain was extracted using the limited number of pixels, the limited cluster size and the 59.45 keV peak, and it was slightly lower. This may have two reasons: an additional parasitic capacitance between the middle SOI layer and the BPW area, or that the area of middle SOI layer is large and there is no BNW between pixels. Some charges could be trapped at the surface between pixels. The energy resolution was very bad probably because the potential fluctuation of middle SOI area in each pixel was high due to high resistivity of middle SOI layer. The resistivity of the middle SOI layer will be reduced in the next fabrication.

The best energy resolution for the13.95 keV peak is 6% (rms) with cluster size = 2 at r3 of NCZ-INTPIXh2, about 0.8 keV. The pixel circuit has no correlated double sampling (CDS) circuit and therefore the result was not good the other integration-type pixel sensors in ref. [6]. When the input transistor in the pixel circuit changes from NMOS to PMOS, the resolution might be improved, as shown in ref. [7].

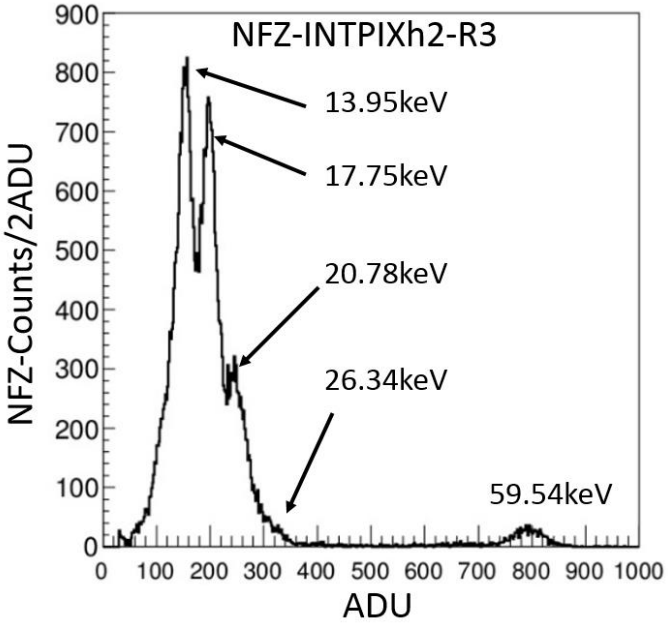

Fig. 3 Am-241 X-ray spectrum measured by r3 of the NFZ-INTPIXh2 SOI sensor. Characteristic X-ray energies are also shown.

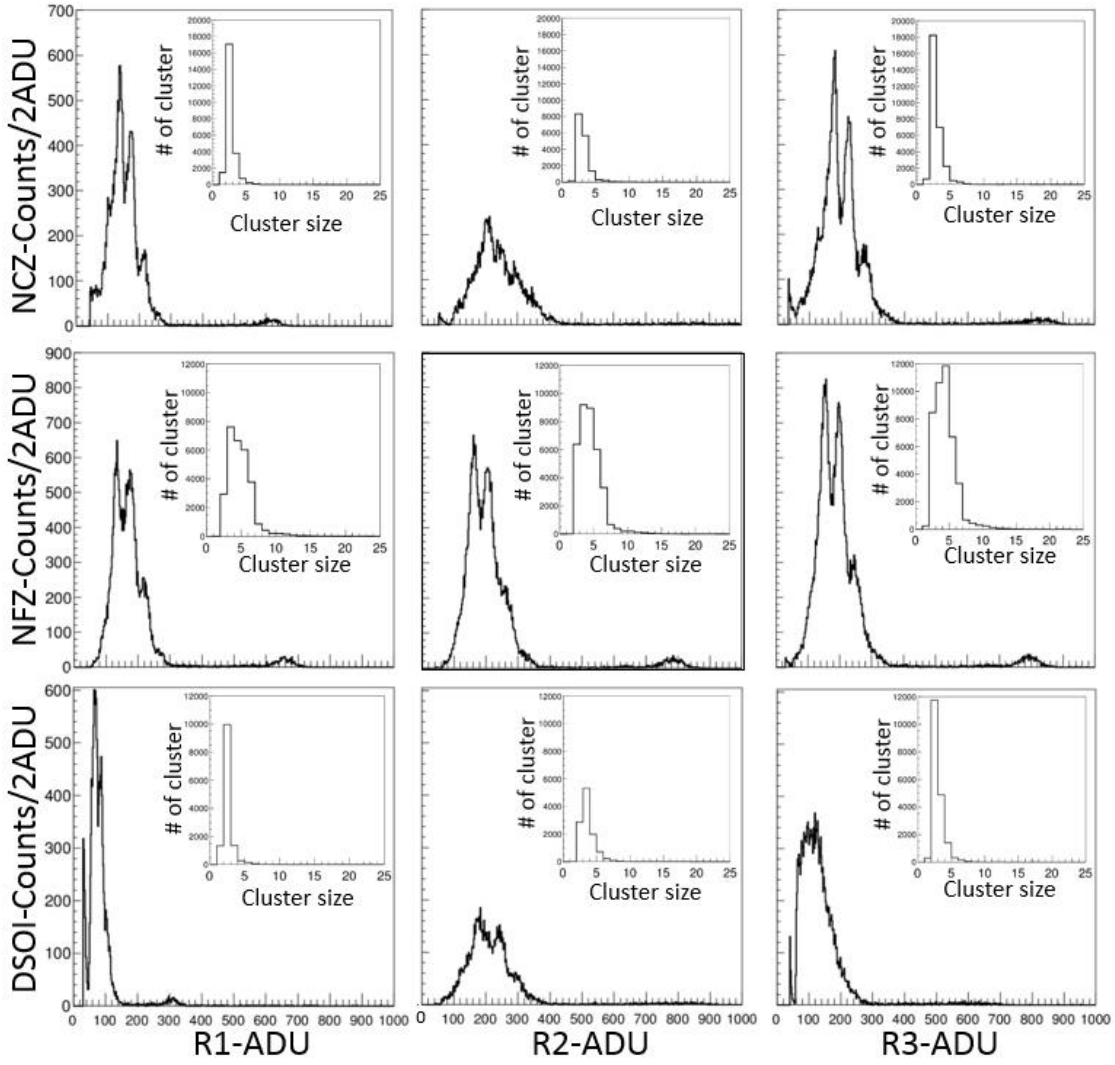

Fig. 4 Am-241 X-ray spectra and cluster distributions for 3 regions of NCZ-, NFZ- and DSOI-INTPIXh2.

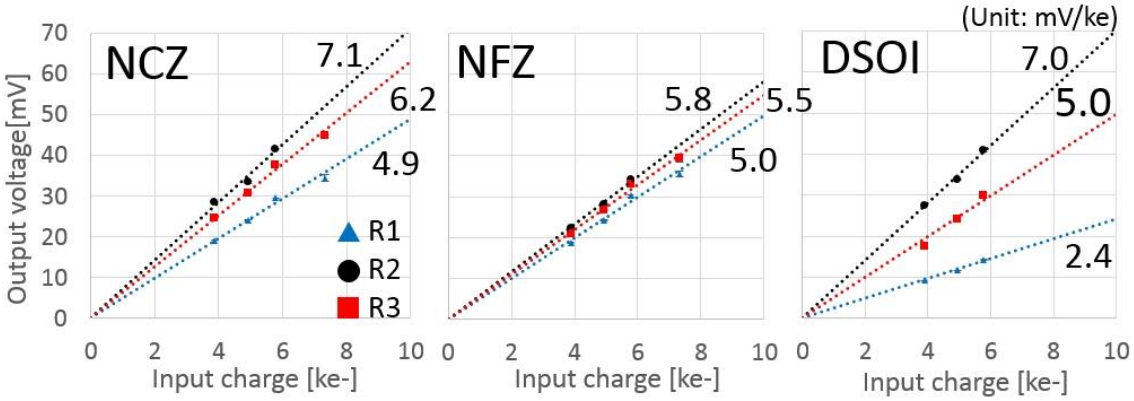

Fig. 5 Pixel gain curves for 3 regions of NCZ-, NFZ-, and DSOI-INTPIXh2. The numbers near fit graph are the sensor gains in mV/ke.

4. Pixel leakage current

Leakage current measurement was performed at different temperatures. In this measurement, the back bias voltage was set to 100 V for all sensors. For each temperature, the average value of pixel output voltage within several integration times was extracted. The voltage shift corresponds to the pixel leakage current. Fig. 6 shows the Arrhenius plot of the dark rate in three pixel types of three sensors. When the slope (activation energy) is close to a half of excitation energy, Eg/2 = 0.56 eV, most of leakage current source is thermal generation current in the substrate. Pixels with lower activation energies were seen to exhibit a higher dark current. When the dark rate is 10^{-3} V/ms, the pixel leakage current in nA/cm^2 is equal to 50 x G, where G is the sensor gain in mV/ke, assuming that the substrate leak is dominant in pixel leak current. Other sources might be protection diode, the gain switch, or any other transistors connected the sensor signal path. Compared with regions, r2 has the highest leakage current probably because it has BNW between pixels and therefore there might be a current source at the interface between Si and BOX above the BNW. The leakage current in r1 was more than that in r3 probably because the gain switch might form another leakage current path.

The features of leakage current in each region is the following;

(1) In NCZ-INTPIXh2, the minimum leakage current was 16 nA/cm^2 at -60 ºC in r3. The slope is slightly small compared with Eg/2, implying that there are other current sources.

(2) In NFZ-INTPIXh2, the leakage current was low. The minimum leakage current was 4 nA/cm^2 at -60 ºC and r3. The curve was fit except data at -50 and -60 ºC. Above -40 ºC, the substrate generation current is dominant because the slope is close to Eg/2. Below 10 nA/cm^2, there might be other sources of leakage current.

(3) In DSOI-INTPIXh2, the minimum leakage current was 140 nA/cm^2 at -60ºC in r3. The reason of the high leakage current is unknown. The slope is less than a half of activation energy and therefore some leakage current sources other than the case of NCZ and NFZ wafers might be present.

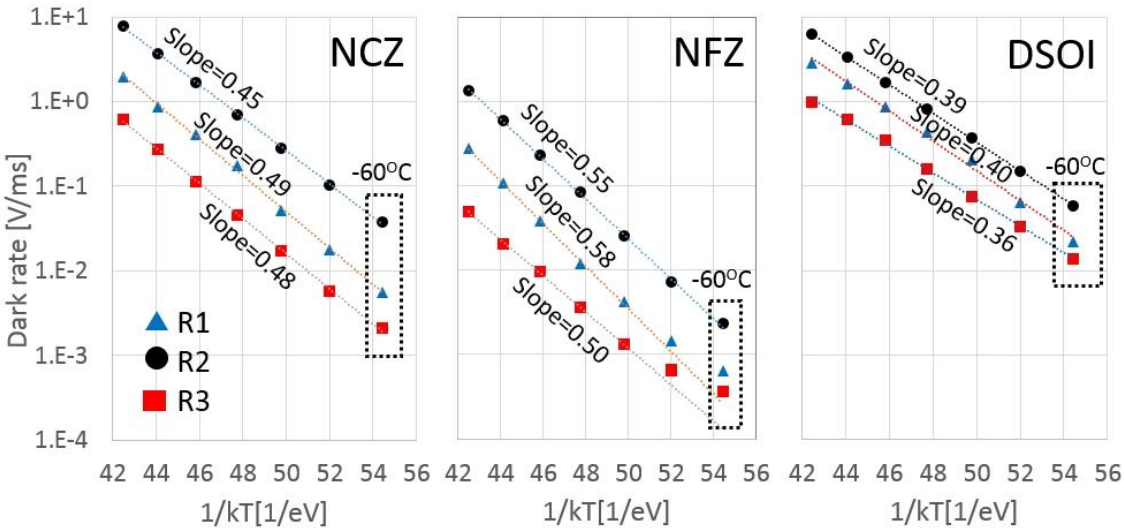

Fig. 6 Temperature dependence of pixel dark rate

5. Summary and outlook

We have developed an integration-type pixel sensor, INTPIXh2, with single and double SOI wafer. In the DSOI-INTPIXh2, the leakage current was higher than that of NCZ- and NFZ-INTPIXh2, and thus the energy resolution of Am-241 spectra was high. It was realized that optimization of BPW, BNW and middle SOI area was a key issue when utilizing the DSOI wafer as a sensor. From the second MPW runs, a double SOI wafer made by a different vendor will be used. The properties of double SOI sensors might be changed even though the basic properties are expected to be the same. As for the sensor and circuit crosstalk, we will evaluate them by using counting type pixel sensors currently under design. The TID tolerance study is described in ref [8]. Our goal in this study is to develop integration-type sensors with 10 mV/ke- of sensor gain, without the back-gate effect and sensor-circuit crosstalk, and TID tolerance above 10 Mrad.

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