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Development of CMOS Pixel Sensors Featuring Pixel-Level Discrimination for the ALICE-ITS Upgrade

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A 180 nm imaging CMOS technology is being used to develop CMOS pixel sensors (CPS) for the upgrade of the ALICE Inner Tracking System (ITS) [1, 2]. The process allows in particular for full CMOS integration inside the pixels thanks to the available deep P-wells. Therefore, a novel concept of pixel with integrated discriminator was realized in order to develop a fast and power-efficient rolling shutter CPS architecture, called ASTRAL. Compared with the conventional CPS using column-level discrimination, the in-pixel discrimination sets the analogue processing within the pixel. Thus the analogue buffer driving the long-distance column bus is no longer needed and the static current consumption per pixel can be largely reduced, from 120 μA down to less than 15 μA. Moreover, the row processing time can be halved down to 100 ns thanks to small local parasitics. As a proof of concept, the prototype chip called AROM-0 was developed. Full functionality and noise performance of the chip have been validated in laboratory. Based on AROM-0, improved pixel designs have been implemented in the series of more advanced chips called AROM-1, which incorporate the intermediate design anticipating the upstream architecture of ASTRAL. It features an array of 64 $\times$ 64 pixels with double-row readout while integrating on chip the JTAG programmable biasing/reference and sequence control circuitry. This paper will mainly present the design and laboratory test results of AROM-0 and AROM-1 chips. Also, a brief introduction to the first prototype chip of the full scale building block for ASTRAL will be given, supposed to verify the full chain and functionality of the ASTRAL sensor.

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1. Introduction

After over 10 years of development, CMOS pixel sensors based on a rolling shutter architecture have entered a mature stage in tracking and vertexing applications. This is illustrated by the ULTIMATE sensor equipping the STAR-PXL detector [3]. Fabricated in a 0.35 μm technology, it has a sensitive surface of $\sim$ 3.8 cm^2 composed of 20.7 μm pitch square pixels. The sensor is read out in rolling shutter mode with column-level discriminators to convert the analogue signals to binary values. These binary signals are then processed by a zero suppression logic to provide sparse outputs. The integration time is close to 200 μs and the power consumption exceeds slightly 150 mW/cm^2. The STAR-PXL detector, which is the first vertex detector equipped with CPS, is taking physics data since early March 2014 [4].

However, in order to adapt CMOS pixel sensors to the upgrade of the ALICE-ITS, significant improvements in radiation tolerance and readout speed should be achieved [5]. A 180 nm CMOS Image Sensor (CIS) quadruple well technology was therefore investigated. Compared with the former 0.35 μm technology, the new technology provides a sensitive volume with higher resistivity and thinner gate oxide, which tend to improve the radiation tolerance. A first generation of CPS prototypes based on this technology was fabricated in 2012 and 2013 and proven to exhibit adequate radiation tolerance [1]. As for the speed aspect, with more parallelized readout, shorter columns and optimized pixel dimensions, the readout speed was increased to fulfill the requirement of the ALICE-ITS upgrade [2]. Moreover, the reduced feature size translated into higher in-pixel microcircuit density, complemented by the available deep P-wells allowing for full CMOS integration inside pixels. These features offered the opportunity to explore new pixel structures including more functionalities.

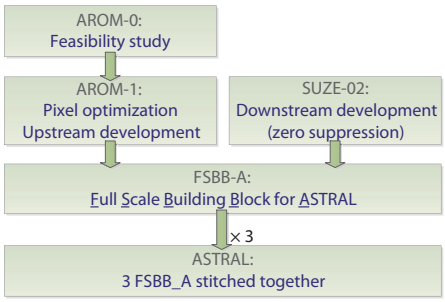


Figure 1: The R&D roadmap towards the ASTRAL sensor dedicated to the ALICE-ITS upgrade.

In this scenario, we proposed the AROM sensor (AROM stands for Accelerated Read-Out Mimosa), the prototype used to develop in-pixel signal discrimination. With pixel-level discrimination, the AROM sensor sets the analogue signal processing inside one pixel and the analogue buffer driving the long-distance column line used in ULTIMATE is no longer needed. Compared with the column-level discrimination, the static current consumption per pixel can be reduced from $\sim$ 120 μA to at best $\sim$ 14 μA per pixel. And by dealing with only the small local parasitics in the analogue readout chain, the row processing time can be halved down to 100 ns. Based on the AROM sensor, an R&D roadmap towards the sensor called ASTRAL (ASTRAL stands for AROM Sensor for the inner TRacker of ALICE) is established. The ASTRAL sensor features one of the ar-

chitectures that have been proposed for the ALICE-ITS upgrade [6]. Following the roadmap shown in figure 1, we first start with the feasibility study by prototyping the chip AROM-0. The development is pursued with several AROM-1 chips to optimize the pixel design and verify the upstream architecture of ASTRAL. In parallel, a new zero suppression logic, called SUZE-02, is being realized [7]. Extending the architecture of AROM-1 to the full scale pixel array and combining it with the SUZE-02 circuit results in the FSBB-A sensor (FSBB-A stands for Full Scale Building Block for ASTRAL), which features a sensitive area exceeding 1 cm^2. The final ASTRAL sensor will be composed of 3 FSBB-A chips operated in parallel and multiplexed at their output nodes [7].

This paper follows the roadmap and focuses mainly on the AROM sensors. In section 2 and section 3, the AROM-0 and AROM-1 sensors will be described and their test results will be summarized, respectively. Some conclusions will be drawn in the last section.

2. AROM-0

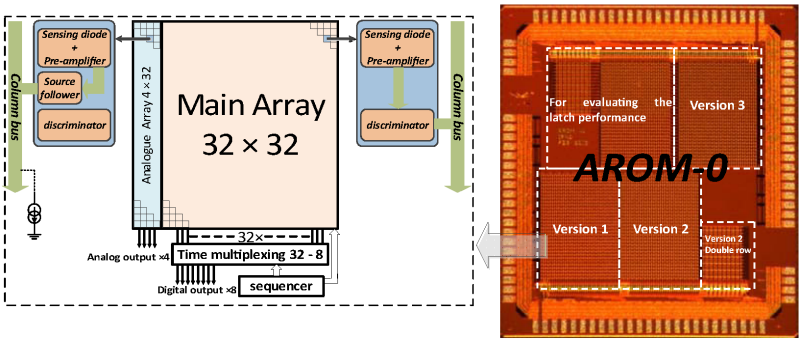
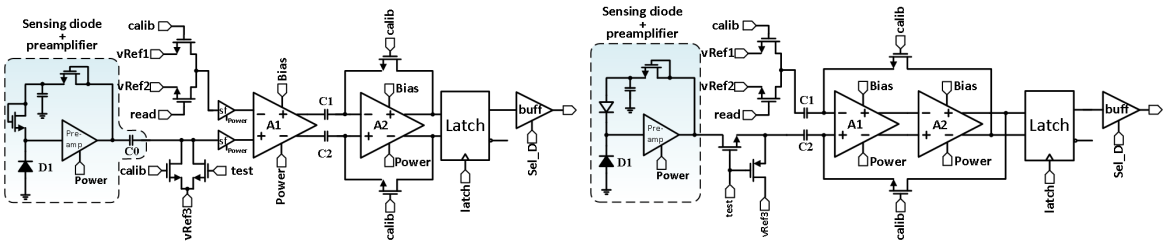


Figure 2: The microscope image of AROM-0 (right) and the structure of a typical 32-row sub-array (left).

The AROM-0 chip, as shown in figure 2 (right), has 6 sub pixelated sub-arrays, each with dedicated purposes. Three different topologies of discriminators are explored. Furthermore, both readout schemes are implemented, either single-row within 32 $\times$ 36 pixel arrays or double-row within 16 $\times$ 18 pixel arrays. Figure 2 (left) also illustrates a typical 32 rows array. In order to calibrate the charge-to-voltage conversion factor (CVF), alongside the main array, there are also 4 columns of pixels with source follower driving the analogue signal from the pre-amplifier to the column end.

2.1 Pixel design

Driven by the requirements of the ALICE-ITS upgrade, the pixel dimensions in AROM-0 were chosen to be 22 $\times$ 33 μm^2 [2]. Each pixel contains a sensing diode, a pre-amplifier, a clamping element and an offset compensated discriminator. The performance of the first three parts has been validated in previous chips [8] and their working principle is described in [9]. The charge sensitive element is formed by an N-well/P-epi diode, labelled "D1" in figure 3, which displays the schematics of the two pixel versions of AROM-0 exhibiting the most satisfactory test results. The pre-amplifier is based on a common source. Its negative, low frequency, feedback mitigates the variation of its operating point due to process dispersion.



(a) Version 1 (b) Version 2

Figure 3: Schematics of the pixels in AROM-0.

Among the three discriminators implemented in AROM-0, the two showing the most promising performances are both composed of two auto-zero amplifying stages and a dynamic latch, but feature different offset compensation schemes (see figure 3). Version 1 includes an output offset storage (OOS) for the first amplifier and an input offset storage (IOS) for the second amplifier. Moreover, a coupling capacitor ("C0" in figure 3(a)) is used between the pre-amplifier and the discriminator, allowing to set the input DC voltage of the discriminator in the appropriate range. Alternatively, in version 2 shown in figure 3(b), two amplifiers are cascaded directly forming a two-stage high gain amplifier with its offset compensated via the IOS scheme. The advantage of version 2 is that the offset storage capacitors "C1" and "C2" provide also AC coupling between the discriminator and the upstream circuitry. Thus, with fewer components, this structure reduces the layout congestion and cross-coupling. Version 2 was therefore implemented in both the single-row and the double-row readout arrays, whereas version 1 was only implemented in the single-row readout array. However, the main drawback of version 2 comes from the stability issue of the two-stage amplifier when it works in closed-loop configuration. This may increase the noise.

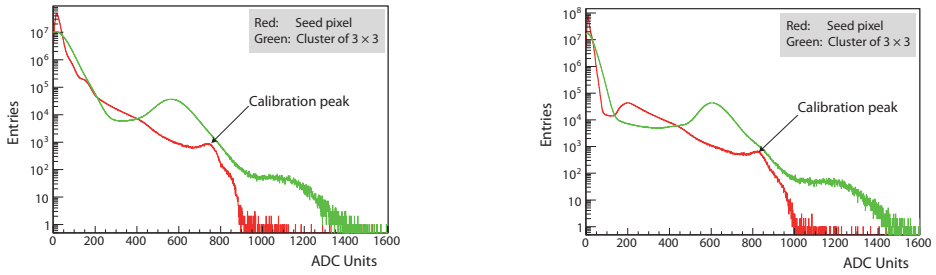
The offset compensation is achieved by applying the two non-overlapping control signals "calib" and "read" to the circuit. The offsets from the amplifiers are first memorized on the two capacitors "C1" and "C2" during the "calib" phase and then canceled in the "read" phase. The discriminator threshold voltage amounts to the difference between the two reference voltages "vRef2" and "vRef1".

The static current of the pixel is designed to be 48 μA and 35 μA for versions 1 and 2, respectively. The latter consume much less current than the conventional column-level discrimination circuitry, which has a typical value of $\sim$ 120 μA. Note that the pixel in AROM-0 is mainly aimed to validate the functionality and has not been optimized yet for power consumption. Its potential for low power operation will be further explored in AROM-1.

2.2 Test results

The test results of the 2 pixel versions described above are exposed in this section. The sensing system (sensing diode and the pre-amplifier) calibration was first performed with the 4 analogue columns in order to obtain the sensing gain after the pre-amplifier. We use an external ADC to convert the obtained analogue signal into digital units. Figure 4 shows the calibration spectra recorded with a ^{55}Fe X-ray source (emitting X-rays mostly with energy of 5.9 keV) illuminating

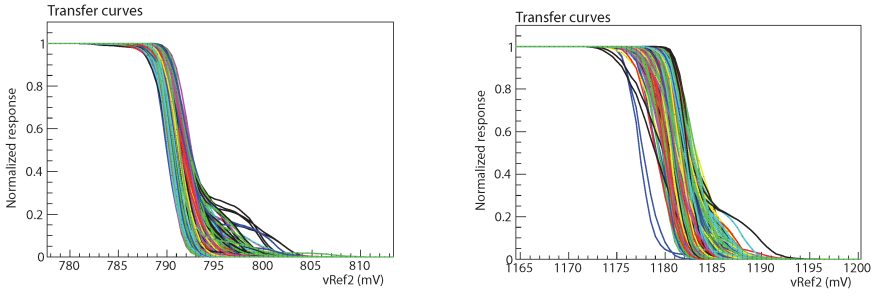
the chip operated at 15 °C. The calibration peak marked in the figure corresponds to the collection of about 1640 e^- generated by 5.9 keV X-Rays in case they impinge the sensor nearby a sensing node. The calibrated CVFs before the discriminator come out to be 52 $\mu V/e^-$ for version 1 and 57 $\mu V/e^-$ for version 2, in satisfactory agreement with the previous measurements performed with analogue pixels without in-pixel discrimination.



(a) Version 1 (b) Version 2

Figure 4: AROM-0 analogue output response obtained by illuminating the sensor with a ^{55}Fe X-ray source. The response for the seed pixel is shown in red and the response for the 3 × 3 pixel cluster is shown in green. The Charge-to-Voltage conversion Factor follows from the calibration peak position, which corresponds to about 1640 e^-.

In order to estimate the noise performance of the full in-pixel circuitry, the transfer curve (also called "S" curve) for each pixel was measured by the probability of "1" events over a large quantity of readout cycles as a function of threshold voltage. The "S" curves of the 1024 pixels obtained at the nominal speed are shown in figure 5. The temporal noise (TN) of each pixel can be extracted by taking the derivative of a corresponding "S" curve, and then calculating its standard deviation. The fixed pattern noise (FPN) is the dispersion of the mean values of those derivatives. The noise contributions are shown in table 1. Note that the TN shown in the table is the average TN value of all the pixels. The total noise is the square root of the squared sum of TN and FPN, which exceeds 1.5 mV and is dominated by TN. By dividing the noise voltage by the CVF, the equivalent noise charge (ENC) is calculated to be $\sim$ 30 e^- for both versions. Further analysis shows that the discriminator and its upstream parts contribute almost equally, each one with about 20 e^- ENC.



(a) Version 1 (b) Version 2

Figure 5: "S" curves of the full in-pixel circuitry obtained at the nominal readout speed for the two pixel versions in AROM-0.

sub-array	TN (mV)	FPN (mV)	Total noise (mV)	ENC (e^-)
Version 1	1.43	0.66	1.57	30.2
Version 2	1.55	0.49	1.62	28.4

Table 1: Noise performance of the full in-pixel circuitry in AROM-0.

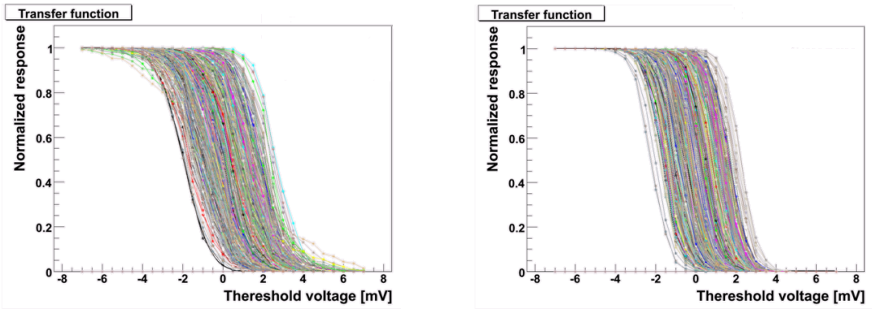
3. AROM-1

The AROM-0 prototype has demonstrated the feasibility of in-pixel discrimination within small pixels (e.g. 22 $\times$ 33 μm^2) and showed encouraging noise performances. The noise sources in the discriminators were studied and improved designs were implemented in new prototypes, the AROM-1 chips. The latter features a 64 $\times$ 64, double-row readout, pixel array. In order to approach the upstream architecture of ASTRAL, they integrate on-chip reference DACs, slow controls, and the steering control through JTAG registers. The AROM-1 chips were produced in five different versions (AROM-1 A/B/C/E/F) featuring different pixel designs. The preliminary test results of the two versions (AROM-1 B and AROM-1 E) having shown the most satisfactory performances are presented hereafter.

3.1 AROM-1 B

In August 2013, the AROM-1 B prototype derived from the AROM-0 version 2 was firstly designed and submitted for fabrication, profiting from the already existing double-row readout circuitry. The layout was optimized to reduce the cross coupling and the thermal noise from the MOS switches was mitigated.

The sensing calibration of the AROM-1 sensors hasn't finished yet. However, we believe that the CVF won't significantly vary with respect to the measurement results of the previous chips implemented with the same sensing system, which give a CVF slightly above 50 $\mu V/e^-$. Besides, the sensing system is still being optimized by several other prototype chips, and it can be easily replaced in the AROM sensor. Therefore, we present and discuss here mainly the noise voltages referred to the input of the in-pixel discriminator.



(a) "S" curves of full in-pixel circuitry (b) "S" curves of in-pixel discriminator

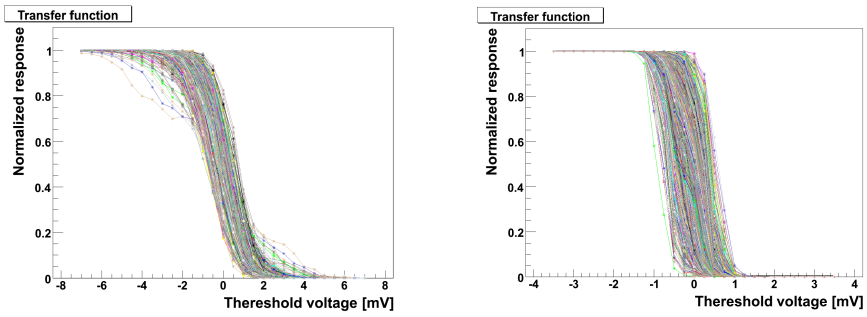
Figure 6: The "S" curves of the full in-pixel circuitry (left) and the "S" curves of the in-pixel discriminator in AROM-1 B (right).

Due to the limitation of the acquisition board used for the tests, the clock frequency was set to 100 MHz instead of the nominal value of 160 MHz. This results in a readout speed of 160 ns/2rows instead of 100 ns/2rows. The measured transfer curves of the full in-pixel circuitry are shown in figure 6(a). The TN and FPN values extracted from these transfer curves are $\sim$ 1.1 mV and $\sim$ 0.66 mV respectively.

We also measured the transfer curves of the in-pixel discriminator (in figure 6(b)) by replacing its connection to the pre-amplifier with a fixed voltage and varying the threshold voltage. The TN and FPN values observed amount to $\sim$ 0.75 mV and $\sim$ 0.63 mV, respectively. Compared with AROM-0, the noise voltage of the discriminator is reduced by $\sim$ 20% , which confirms the effectiveness of the layout and thermal noise optimization. Note that in order to mitigate the random telegraph signal (RTS) noise from the pre-amplifier, the dimension of its input transistor was increased compared to AROM-0, resulting in a lower CVF. Therefore, even though the noise performance of the discriminator was improved, it is still the dominant noise component, contributing to the TN about as much as the upstream circuitry and representing most of the FPN. Overall, the current results are nevertheless expected to allow for satisfactory SNR.

3.2 AROM-1 E

The AROM-1 E prototype is derived from the version 1 of AROM-0. It was submitted for fabrication in November 2013. The improvements with respect to AROM-0 address mainly the pixel layout and the discriminator thermal noise. Simulations predicted that AROM-1 E would have much lower discriminator noise than AROM-1 B. With respect to the latter, AROM-1 E was also further improved in terms of low power operation, resulting in a designed pixel static current consumption of $\sim$ 15 μA.



(a) "S" curves of full in-pixel circuitry (b) "S" curves of in-pixel discriminator

Figure 7: The "S" curves of the full in-pixel circuitry (left) and the "S" curves of the in-pixel discriminator in AROM-1 E (right).

The measured transfer curves of the full in-pixel circuitry using a 100 MHz clock are shown in figure 7(a). The extracted noise values are summarized in table 2. The noise performance of the in-pixel discriminator of AROM-1 E was also measured separately (in figure 7(b)), as with AROM-1 B. The results are summarized in table 3. For comparison, the test results of AROM-1 B are recalled in those tables. As expected from the simulation, the noise of the in-pixel discriminator integrated in AROM-1 E is significantly decreased, as well in terms of TN as for the FPN. Consequently,

the discriminator is no longer the dominant noise source. This result may be considered as an achievement since it validates a well performing pixel design as a baseline for future development.

Chip version	TN (mV)	FPN (mV)	Total noise (mV)
AROM-1 E	0.94	0.23	0.97
AROM-1 B	1.1	0.66	1.28

Table 2: Noise performance of full in-pixel circuitry in AROM-1 E and AROM-1 B.

Chip version	TN (mV)	FPN (mV)	Total noise (mV)
AROM-1 E	0.29	0.19	0.35
AROM-1 B	0.75	0.63	0.98

Table 3: Noise performance of in-pixel discriminator in AROM-1 E and AROM-1 B.

4. Conclusions

Based on the architecture of the CPS (called ULTIMATE) implemented in the STAR-PXL detector, a faster sensor (called ASTRAL) is being developed for the ALICE-ITS upgrade, using a CMOS process allowing for in-pixel discrimination, reduced power consumption and higher radiation tolerance. This paper focused on the achievement of a pixel design (AROM-0 and AROM-1 prototypes) exhibiting the required low noise and low power performances. After a few iterations of prototyping, the pixel design in AROM-1 E has shown very promising noise performances. The TN of its full in-pixel circuitry is ~ 0.94 mV and the FPN is ~ 0.23 mV. The in-pixel discriminator contributes with ~ 0.29 mV of TN and ~ 0.19 mV of FPN, which makes the discriminator a minor noise source. Based on the pixel in AROM-1 E, the chip called FSBB-A0 was developed in early 2014. It is the first full scale prototype of one of the three identical units composing ASTRAL. The sensitive area is made of 416×416 pixels and amounts to $\sim 13.7 \times 9.2$ mm^2. The double-row rolling shutter readout results in an integration time of ~ 20 μs. This circuit integrates a new zero suppression logic, called SUZE-02, which is more powerful than the one used in ULTIMATE.

The FSBB-A0 will verify the full chain and functionalities of the ASTRAL components but does not yet incorporate all possible optimizations. The chip has returned from foundry and is being characterized. The next step of the development will consist in fabricating the final FSBB-A design before the complete ASTRAL sensor, combining three FSBB-A units, may be manufactured.

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