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Ultra-transparent DEPFET pixel detectors for future electron-positron experiments

C. Marinas[*†]
University of Bonn, Physikalisches Institut, Germany
E-mail: cmarinas@uni-bonn.de

The DEPFET Collaboration develops highly granular, ultra-thin pixel detectors for outstanding vertex reconstruction at future collider experiments. A DEPFET sensor, by the integration of a field effect transistor on a fully depleted silicon bulk, provides simultaneously position sensitive detector capabilities and in-pixel amplification. The characterization of the latest DEPFET prototypes has proven that a comfortable signal to noise ratio and excellent single point resolution can be achieved for a sensor thickness of 50 micrometers. The close to final auxiliary ASICs have been produced and found to operate a DEPFET pixel detector of the latest generation with the required read-out speed. A complete detector concept is being developed for the Belle II experiment at the new Japanese super flavor factory. DEPFET is not only the technology of choice for the Belle II vertex detector, but also a solid candidate for the ILC. Therefore, in this paper, the status of DEPFET R&D project is reviewed in the light of the requirements of the vertex detector at a future electron-positron collider.

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[*] Speaker.
[†] On behalf of the DEPFET Collaboration.

1. Introduction

Ultra-high luminosity flavor factories are discovery instruments that complement the capabilities of the high-energy linear electron-positron colliders. Both alternatives yield excellent opportunities to stress-test the Standard Model of particle physics with a precision that goes well beyond what can be achieved at hadron machines [1].

In order to fully exploit the capabilities of such precision machines excellent detectors, beyond the current state of the art defined by the LHC experiments, are needed. In particular, the inner detector systems in both cases, luminosity and energy frontier machines, have to cope with very stringent requirements [2] [3]: high-resolution low-mass trackers and extremely ultra-transparent granular pixel vertex detectors are required.

DEPFET [1] due to its excellent spatial resolution, large signal-to-noise ratio, low material budget and reduced power consumption [4] has been chosen the baseline technology for the pixel detector of the Belle II experiment in the new Japanese super flavor factory and is one of the strong candidates for the vertex detector of the ILC detector concepts [5].

The DEPFET detectors developed for the Belle II pixel detector (PXD) are almost prototypes of the two innermost layers of the ILD vertex detector as shown in table 1. Clearly, two of the most challenging specifications (readout speed and material budget) are very similar in both applications and several of the relevant challenges for the ILC are currently being addressed by the DEPFET-based solution for Belle II.

	Belle II pixel detector	ILD vertex detector
Occupancy [hits/μm^2/s]	0.40	0.13
TID per year [Mrad]	2.0	<0.1
NIEL per cm^2 and year [1 MeV n$_{eq}$]	2.0×10^{12}	1.0×10^{11}
Frame readout time [μs]	20	25-100
Material budget per layer [X_0]	0.21 %	0.12 %
Resolution [μm]	15	5

Table 1: Comparison of the main requirements for the Belle II and ILC vertex detectors. The combination of all these factors is a substantial challenge for the detector system.

1.1 The DEPFET technology

DEPFET is an active pixel solid state detector technology that exploits the concept of amplifying p-channel field effect transistors in a fully depleted n-type silicon bulk. An additional n$^+$ implant (*internal gate*) underneath the transistor's channel forms a potential minimum for the electrons in the substrate. The signal electrons drift towards the internal gate and, once there, modulate proportionally the drain-source current in the transistor. After the read-out, the charges can be removed from the internal gate by applying a periodic voltage pulse to a *clear* contact placed on the periphery of each pixel [6]. A more detailed description of the DEPFET technology can be found in [7].

[1] **DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor.

A DEPFET sensor provides detection, fast charge collection with limited lateral diffusion and internal amplification. Due to the small capacitance of the collection node, the DEPFET has a low intrinsic noise while a large signal is achieved due to the fully depleted bulk. This combination allows the reduction of the active detector thickness to few tens of micrometers while keeping a comfortably large signal-to-noise ratio (SNR) [8]. The crucial parameter of the DEPFET technology is the gain of the first amplification stage (g_q), expressed in current variation per electron.

1.2 The all-silicon ladder

A finely segmented DEPFET detector contains a combination of individual DEPFET pixels arranged in a matrix and operated together on the surface of the sensor. Such a pixel matrix is operated using a *rolling – shutter* architecture. The gate and clear lines of the pixels placed on the same matrix row are connected to a control chip (*SwitcherB*) [9], responsible for selecting subsequent rows of pixels. An entire column of pixels is read out by a current receiver ASIC (*DCDB* or Drain Current Digitizer) [10]. The data from the DCD is further transmitted to the *DHP* (Data Handling Processor), the third ASIC in the ladder, which performs data processing and compression [11]. The latest designs and current status of the auxiliary ASICs required to operate a Belle II DEPFET sensor are discussed in more detail in reference [12].

The basic unit on a DEPFET-based vertex detector (*module*) is depicted in figure 1. By the repetition, in a cylindrical arrangement of this all-silicon ladder (two modules glued together) around the beam pipe, the geometry of the vertex detector is implemented.

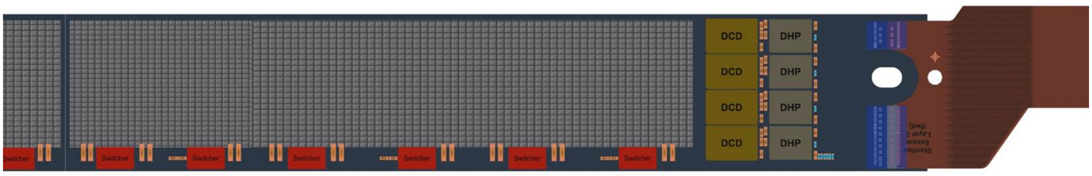

Figure 1: Schematic view of an all-silicon DEPFET module. The front-end ASICs (on the right hand side) are bump bonded directly on the thick silicon integrated support structure that keeps the stiffness of the assembly. The control chips are placed in the lateral balcony that runs next to the sensor, that fills the central part of the module.

To comply with the very tight material budget requirement, the sensitive area placed in the central part of a DEPFET ladder is ground to the thickness required by the specific application, and the material in support and services must be reduced to the bare minimum [13]. The thinning technology uses anisotropic etching on bonded wafers to create a thin, fully self supporting sensor, where no external structures are needed. The use of a single type of material for sensor and support structure furthermore reduces the mechanical stress due to absence of CTE [2] mismatch. The stiffness is provided by a thick [3] (400 μm) silicon rim around the sensor, where the auxiliary ASICs are directly bonded to.

[2] Coefficient of Thermal Expansion.

[3] Additional grooves are etched for further material reduction.

2. Latest DEPFET prototype production

The fabrication of a DEPFET sensor is a complex process, involving very different technology aggregates. The DEPFET pixel technology contains implantations, photolithographic mask steps, poly-silicon and metal layers as well as double sided wafer processing.

The latest prototype production is called PXD6. The production contains 8 SOI[4] wafers with 50 μm thin sensors. In the wafer, small test matrices tailored to the Belle II requirements with different design variations as well as full size sensors for prototyping have been produced (figure 2)).

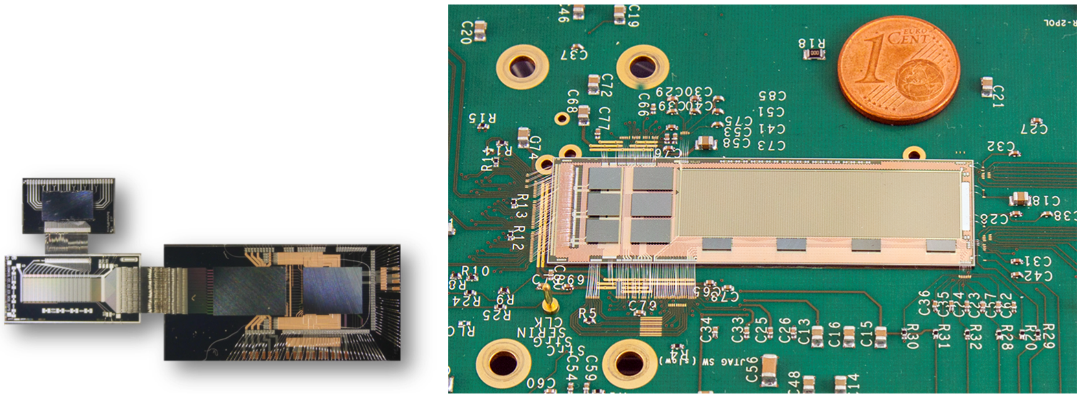

Figure 2: (Left) Picture of the Belle II system demonstrator. A system composed by one small DEPFET sensor (32×64 pixels) of the latest prototype run has been operated with close to final version of the ASICs. (Right) First large scale DEPFET ladder. The active area in the center of the image is a thin (50 μm) active silicon membrane containing 192×480 DEPFET pixels. The detector is equipped with 3 DCD/DHP pairs and 4 Switchers. The size of the control ASICs is the same in both cases.

3. Characterization of DEPFET prototypes

The performance of small thin DEPFET sensors (figure 2 (Left)) from the latest prototype production has been extensively studied with lasers and radioactive sources in the laboratory as well as in beam tests at CERN and DESY [14]. The first step before investigating the different properties of a DEPFET detector includes the optimization of the different bias voltages from the sensor and also the front-end-electronics. The charge collection uniformity of the signal over a large area of the sensor has been evaluated using a red laser scan (figure 3 (Left)). In this particular design, less than 6 % of signal spread was found in the signal collection over 400 pixels.

An absolute energy calibration of the system was performed using different transition lines from a variable X-ray source. The most probable value of the Gaussian fit to the different spectra peaks is plotted versus the expected energy deposition (figure 3 (Right)). The system response is linear within the explored range and from the slope of the linear fit the gain of the first in-pixel amplification stage can be obtained to be $g_q\sim$500 pA/e$^-$, compatible with the designed value. The internal amplification obtained by using the DEPFET drain current distributions due to perpendicularly incident MIPs on test beam campaigns gives compatible results with the laboratory calibration.

[4]Silicon-on-insulator.

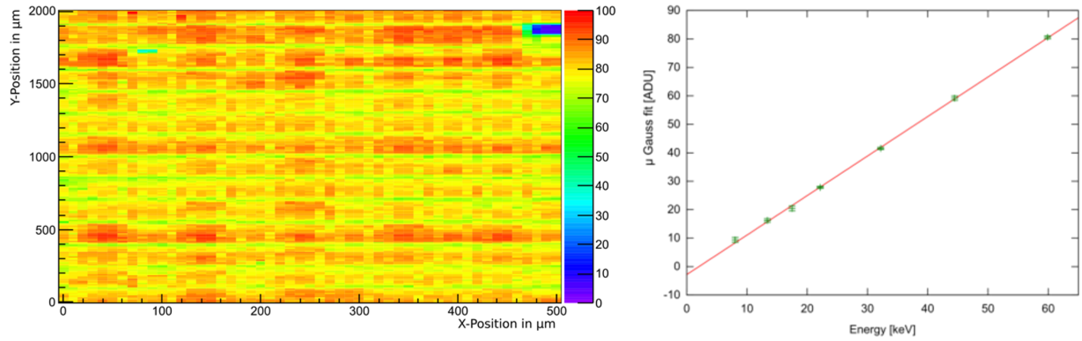

Figure 3: (Left) A 16×26 pixels area of the DEPFET sensor was scanned with a laser to study the signal collection uniformity over large regions. The percentage of charge collected by the sensor with respect of the charge created by the laser is shown (100 % corresponds to roughly 10 MIPs). (Right) Linearity of the response of the detector system versus the deposited energy in the sensor.

In addition, the intrinsic resolution of the detector matches the detector requirements for perpendicular tracks, obtaining $\sim$10 μm with a pixel pitch of 50×50 μm^2 and approaching 1 μm with 20×20 μm^2 and 450 μm thick ILC-like sensor type [15]. The efficiency stays above 99.5 % independently of the position of the impinging particle.

4. First operation of a large-scale DEPFET sensor

In December 2013 and January 2014 the first thin large-scale DEPFET ladder was operated in a beam of particles at DESY. A photograph of the ladder is shown in figure 2 (Right). It consists of a DEPFET sensor with 480×192 pixels, with a 50×75 μm^2 pixel pitch, resulting in an active area of 39.0×9.6 mm^2. The goal of the test beam period was the combined operation of a small sector of final-design components of the Belle II vertex detector; namely, a thin close-to-final size DEPFET sensor and 4 silicon micro-strip modules [16], arranged in a configuration that mimics the final Belle II vertex detector geometry. The readout of such detector system was performed using a scaled version of the final full DAQ chain [17] [18] [19]. The detectors were biased using the power supply prototypes [20] with full length services (15 m for data and power)). The cooling [21] consisted on bi-phase CO_2, delivered into the detector chamber after 15 m long distribution lines from the cooling plant. In addition, a full set of environmental monitors (temperature and humidity) based on commercial sensors and calibrated optical fiber with Bragg structures [22] were installed and integrated into the fully developed slow control system. The beam test set-up was inserted in a 1 Tesla solenoid field. The event display of figure 4 shows the reconstructed trajectory of a 5 GeV electron after entering the detector chamber through the magnet outer wall. The information contained in the micro-strip detector is used to reconstruct the track of the particle [23]. The track is further extrapolated to the DEPFET sensor and a hit was found at the intersection between the track and the DEPFET active area. The electron also leaves a signal in the six telescope planes. Analysis of the data is ongoing at the time of writing and no quantitative results beyond basic distributions (hit maps, signal distributions) that show that the DEPFET system indeed detected particles are available. This first full ladder corresponds to the Belle II design, but this achievement marks an important milestone also for the DEPFET-ILC project.

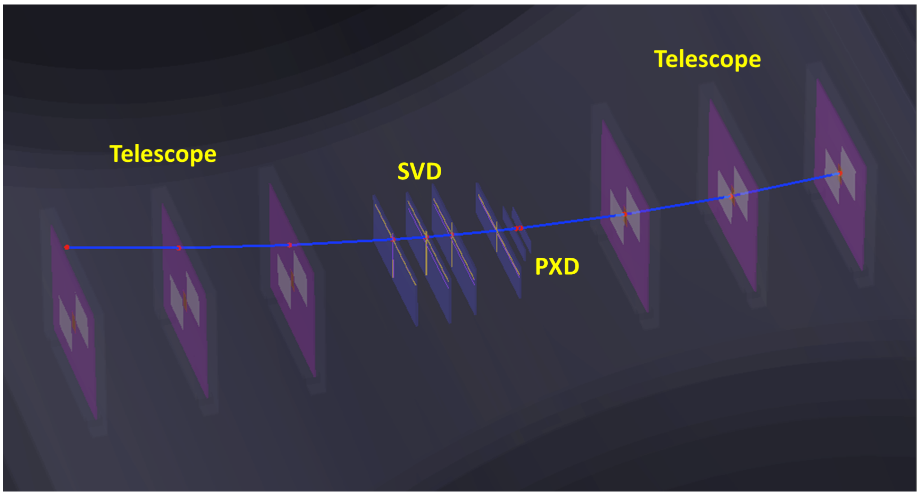

Figure 4: Event display with the reconstructed trajectory of a 5 GeV electron curling in the 1 Tesla magnetic field and leaving signal in the telescope planes, four micro-strip silicon sensors and the DEPFET ladder.

5. Micro channel cooling

The most important difference between the Belle II and ILC experiments is the angular coverage. While Belle II covers a limited and asymmetric angular range the ILC experiments, on the other hand, aim for high performance instrumentation down to a polar angle of 6 degrees. In the Belle II case, support and cooling structures [24] as well as the necessary services for the vertex detector can be safely placed outside of the acceptance, while for the ILC the material has to be kept to a bare minimum.

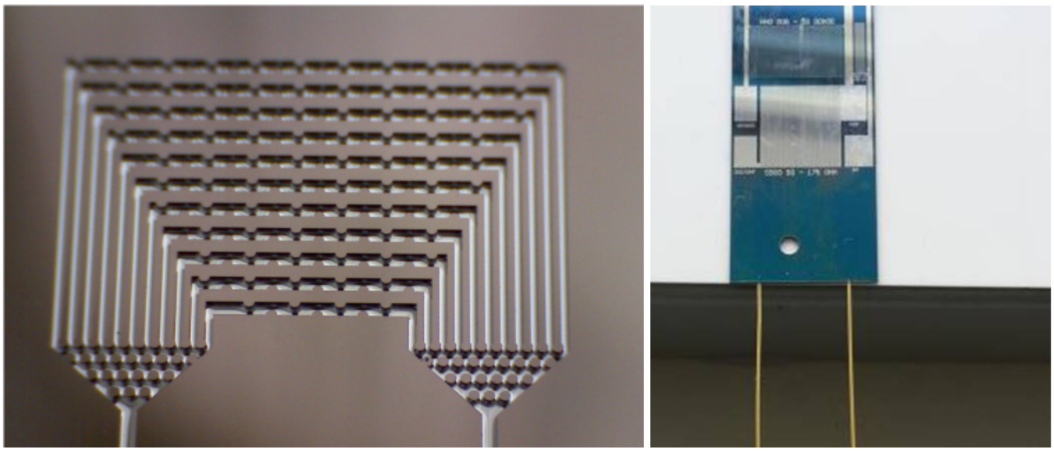

Figure 5: (Left) Picture of the micro-manifold implemented on the handle wafer before bonding the sensor on top. (Right) Inlet and outlet connections using commercial 360 μm outer diameter PEEK pipes.

The baseline cooling concept of the ILD vertex detector concepts rely on forced convection with cold air as a coolant, chosen for its simplicity and low impact on the overall detector material. With the expected power consumption a forced gas flow is deemed adequate [25]. The experience with the Belle II mock-up and simulation has strengthened confidence in the concept itself and the tools to design a working system. However, a rigorous proof of principle of the cooling concept based on forced gas flow only is still lacking, and no practical way of setting up the flow has yet been presented. The all-silicon concept aims to achieve both by integrating active material, support structures and, specifically for the ILC, integrated micro channels for cooling. Due to its higher heat transfer coefficient, the option to indirectly cool the front end electronics via micro-channels directly machined into the handle wafer is being investigated (figure 5). It is relatively straightforward to extend the DEPFET process with a mask step that creates micro-channels in the thicker end-of-ladder areas, where most of the power is dissipated. The heat conduction volume can be increased by adding protrusions to the channels and additional staggered fins were introduced to homogenize the liquid flow through the channels as well as to serve as an additional compact heat exchangers.

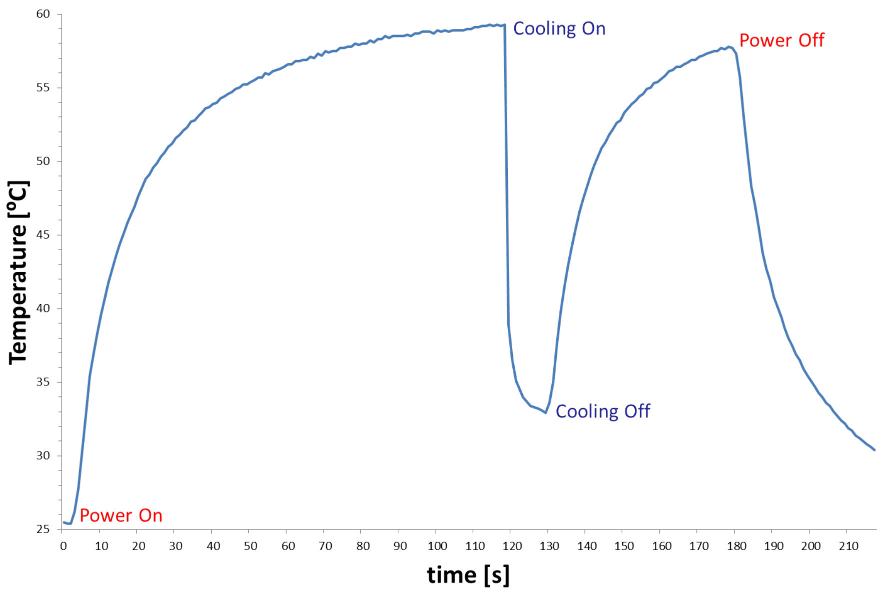

Figure 6: Time evolution of the end of module temperature.

To prove the principle, a mechanical sample was exposed to a continuous load of 2.5 W/cm^2 in the resistor circuit on the silicon surface. The evolution of the temperature with time is presented in figure 6. Without active cooling an equilibrium temperature is reached of over 60 °C, that exceeds the limits for a safe detector operation. Once a modest mass flow of 0.1 l/h of water at room temperature is circulated through the channels (corresponding to a pressure drop of less than 2.5 bar) the surface temperature decreases in a matter of seconds to less than 10 °C above the temperature of the water and surrounding air.

6. Summary

The DEPFET Collaboration develops highly granular, ultra-transparent active pixel detectors for high performance vertexing at future e^+e^- colliders. The good performance of the DEPFET detector system in terms of signal-to-noise ratio, spatial resolution and readout speed has been demonstrated with tests performed with the latest prototype production. In January 2014, the first full-scale DEPFET sensor equipped with close to final versions of the ASICs was successfully operated in a beam test at DESY, together with the micro-strip system of the Belle II detector. Additional R&D is carried on to adapt the current DEPFET detector system to cope the requirements of the future ILC and, in this direction, the first tests on silicon modules with integrated micro-channels for cooling demonstrate that this novel technique holds great promise.

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