The upgrade of the ALICE Inner Tracking System - Status of the R&D on monolithic silicon pixel sensors

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As a major part of its upgrade plans, the ALICE experiment schedules the installation of a novel Inner Tracking System (ITS) during the Long Shutdown 2 (LS2) of the LHC in 2018/19. It will replace the present silicon tracker with seven layers of Monolithic Active Pixel Sensors (MAPS) and significantly improve the detector performance in terms of tracking and rate capabilities. The choice of technology has been guided by the tight requirements on the material budget of 0.3% X/X_0/layer for the three innermost layers and backed by the significant progress in the field of MAPS in recent years.

The pixel chips are manufactured in the TowerJazz $180\,\text{nm}$ CMOS imaging sensor process on wafers with a high resistivity epitaxial layer. Within the ongoing R&D phase, several sensor chip prototypes have been developed and produced on different epitaxial layer thicknesses and resistivities. These chips are being characterized for their performance before and after irradiation using source tests, test beam and measurements using an infrared Laser.

This contribution will provide an overview of the ALICE ITS upgrade focussing on the pixel related R&D activities.

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1. Introduction

ALICE (A Large Ion Collider Experiment) [1] is the experiment at the CERN LHC optimized for ultra-relativistic nucleus-nucleus (A-A) and proton-nucleus (p-A) collisions with the main goal to study the Quark-Gluon Plasma (QGP). For the period after the Long Shutdown 2 (LS2) of the LHC, ALICE plans to significantly enhance its physics capabilities, particularly aiming for high precision measurements of rare probes at low transverse momenta. ALICE therefore scheduled a major upgrade of its apparatus, planned for installation in 2018/19.

1.1 ALICE upgrade

The ALICE upgrade strategy is based on a combination of detector upgrades and a significant increase in luminosity of Pb-Pb collisons, reaching $\mathscr{L} = 6 \times 10^{27} \, \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and resulting in an event rate of about 50 kHz. In the proposed plan, the ALICE detector will be upgraded to enable the readout of all interactions, accumulating more than $10 \, \mathrm{nb}^{-1}$ of Pb-Pb collisions following LS2. Since the majority of the rare probes in Pb-Pb collisions cannot be selected with a trigger due to a very high combinatorial background it is required to take minimum bias data. For these measurements the upgrade will provide an increase of statistics of about a factor 100 with respect to the programme until the LS2. For the measurements that are currently based on rare triggers, the increase in statistics will be a factor 10. Moreover, the intended measurements ask for a significant improvement in vertexing and tracking efficiency at low p_T. In summary, the detector upgrade consists of [2]:

- A reduction of the beam pipe diameter from 29.8 mm to 19.8 mm;

- New high resolution, low material silicon trackers:

  - **Inner Tracking System (ITS)** [3] covering mid rapidity;
  - Muon Forward Tracker (MFT) [4] covering forward rapidity to add vertexing capabilities to the current Muon Spectrometer;

- Upgrade of the Time Projection Chamber (TPC) [5], consisting of the replacement of the wire chambers with GEM detectors and new pipelined readout electronics allowing for continous readout;

- Upgrade of the readout electronics of the Transition Radiation Detector (TRD), Time Of Flight (TOF) detector, and Muon Spectrometer for high rate operation;

- Upgrade of the online and offline reconstruction and analysis framework [6].

2. ALICE ITS upgrade

The main purpose of the ITS upgrade is to improve the primary vertex position reconstruction of the decay vertices of heavy-flavour hadrons, and an improved performance for detection of low-mass dileptons emitted by the QGP. The design objectives are to record Pb-Pb collsions at 50 kHz and p-p collisions at several 100 kHz, while improving the pointing resolution by a factor three in
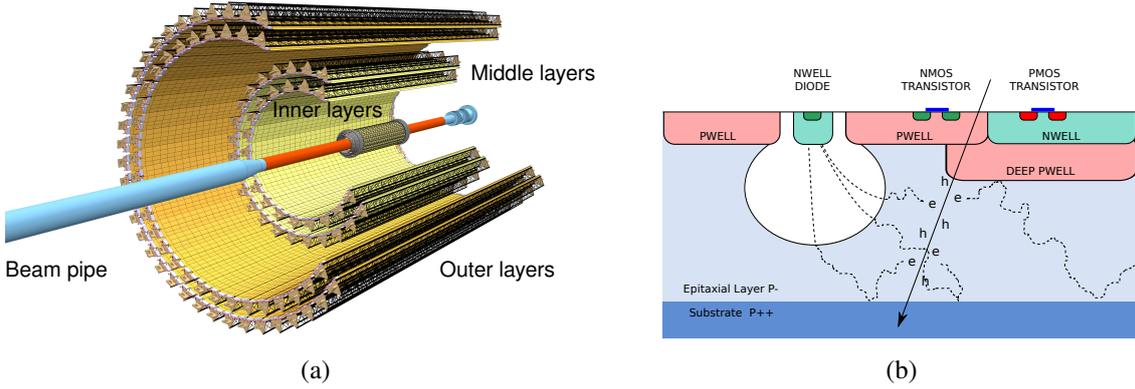
Figure 1: Proposed layout of the new ITS (a) and schematic cross section of a typical monolithic pixel in the TowerJazz 180 nm CMOS imaging process with the deep p-well feature (b).

$r\phi$ and a factor five in z at $p_T = 500$ MeV with respect to the present ITS. This is planned to be achieved by:

- reducing the distance between the first layer and the interaction point from 39 mm to 22 mm;

- reducing the material budget per layer X/X_0/layer from 1.14 % to 0.3 % for the inner layers and to 0.8 % for the outer layers;

- reducing the pixel size from 50 μm × 425 μm to the order of 30 μm × 30 μm.

The standalone tracking efficiency and p_T resolution at low transverse momenta are furthermore planned to be improved by increasing the number of layers from currently six to seven. To allow for an efficient yearly maintenance, the layout will provide the possibility for fast insertion and removal of detector parts.

2.1 Layout and expected performance of the upgraded ITS

To achieve the design objectives described above, the baseline solution for the layout of the ITS upgrade is to fully replace the present ITS detector with seven layers of pixel detectors (cf. Fig. 1a). The layers are grouped into two separate barrels, each with different requirements (cf. Tab. 1). The Inner Barrel consists of the three innermost layers, while the Outer Barrel contains the four outermost layers. The longitudinal extensions of the layers were chosen to provide a pseudo-rapidity coverage of $|\eta| < 1.22$ over 90 % of the luminous region. The radial positions of the layers were tuned to obtain the optimal combined performance in terms of pointing resolution, p_T-resolution and tracking efficiency. The new ITS will cover a surface of 10.3 m^2 with approximately 12.5×10^9 pixels with binary readout. According to the target statistics for Pb-Pb and p-p collisions, the required radiation hardness at the innermost layer, including a safety factor of ten, is 700 krad (TID) and 1×10^{13} 1 MeV n$_{eq}$/cm^2 (NIEL). To minimize the material budget, the silicon thickness of all layers will be 50 μm.

On the basis of the above considerations, monolithic silicon pixel sensors were selected as the technology for all layers, where the sensor and the readout electronics are integrated inside the same silicon chip. Monolithic pixel sensors have shown a significant progress in recent years,

Table 1: General requirements on the pixel chip [3]

Parameter	Inner Barrel	Outer Barrel
Max. silicon thickness	$50\,\mu m$	
Spatial resolution	$5\,\mu m$	$30\,\mu m$
Chip dimensions	$15 \times 30\,mm^2$ ($r\phi \times z$)	
Max. power density	$300\,mW/cm^2$	$100\,mW/cm^2$
Max. integration time	$30\,\mu s$	
TID radiation hardness[a]	$700\,krad$	$10\,krad$
NIEL radiation hardness[a]	$1 \times 10^{13}\,1\,MeV\,n_{eq}/cm^2$	$3 \times 10^{10}\,1\,MeV\,n_{eq}/cm^2$

[a]This includes a safety factor of ten
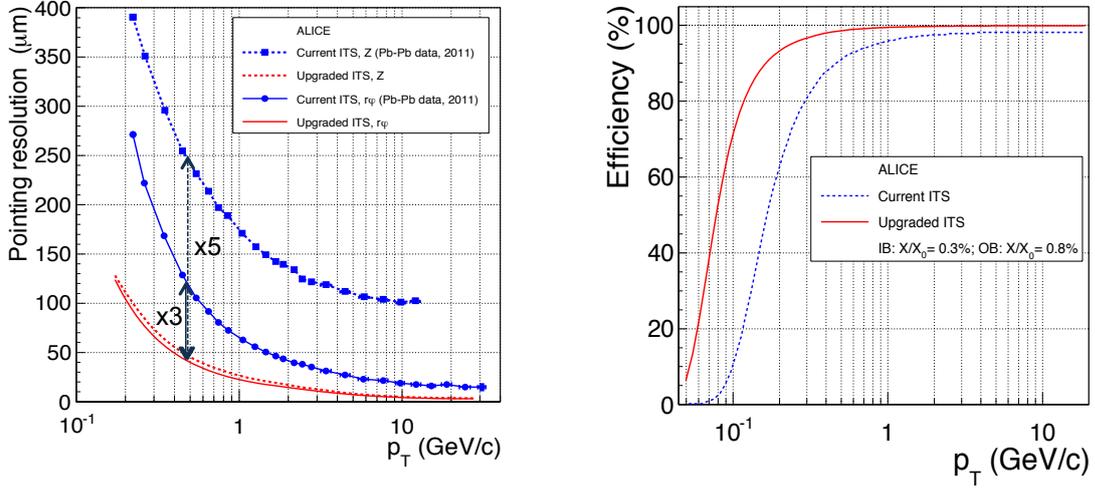
(a) Pointing resolution as a function of transverse momentum.

(b) Tracking efficiency as a funciton of transverse momentum.

Figure 2: Expected performance of the upgraded ITS [3].

the first large scale application being represented by the STAR PXL detector at RHIC, which is equipped with ULTIMATE chips [7]. However, this chip does not meet the requirements for the ALICE ITS uprade in terms of readout time, power consumption and radiation hardness, which makes further developments necessary.

Considering the base line layout presented above and the required performance of the pixel sensor, detailed Monte-Carlo simulations have been performed. The expected pointing resolution of the new ITS is compared to the one of the present ITS in Fig. 2a. It can be observed that the ITS upgrade can significantly improve the performance of the detector at low values of transverse momenta. As shown in Fig. 2b, large improvements can also be expected for the tracking efficiency.

3. Pixel sensor

The monolithic silicon pixel sensor for the new ALICE ITS was chosen to be implemented in the 180 nm CMOS imaging process of TowerJazz[1] since it offers a high-resistivity silicon epitaxial layer on a p-type substrate and a special deep p-well for full CMOS within the matrix with up to six metal layers. The pixel chip consists of a single silicon die of about 15 mm × 30 mm, which incorporates the high-resistiviy epitaxial layer as the sensor acitve volume. The signal charge is collected by an n-well implant, while additional n-wells and p-wells on top of the epitaxial layer host the in-pixel circuitry (cf. Fig. 1b). The deep p-well shields the n-well containing the PMOS transistors from the epitaxial layer and prevents it from collecting signal charge from the epitaxial layer instead of the n-well intended as charge collection diode. Additional reverse bias can be obtained by applying a negative voltage to the substrate. An increase of the reverse bias induces an enlargement of the depletion volume, with a consequent positive effect on the charge collection process and pixel capacitance. However, in the current architecture the fraction of the pixel area covered by circuitry is too large to fully deplete the epitaxial layer.

The main challenge during the development of the final pixel chip is to satisfy simultaneously the stringent requirements in terms of the spatial resolution, readout time and power consumption. Beside the contribution of the silicon sensor, a reduction of power consumption and a highly optimized scheme for the distribution of the electrical power are of importance for the reduction of the overal material budget. The general requirements on the pixel chip are presented in Tab. 1.

3.1 Architecture design streams

Currently there are two main design streams, called ASTRAL and ALPIDE. Both sensors will have in-pixel discriminators, which allow to reduce the power density significantly compared to previous designs. The ASTRAL design is derived from the UTIMATE architecture. It is based on a double-row rolling shutter readout with an end-of-column zero suppression logic and has an expected power density of 85 mW/cm^2 and a full integration time of 20 μs. The ALPIDE [8] design is based on in-matrix sparsification. Each pixel will, in addition to the discriminator, also contain a digital memory cell, where the hit information can be stored upon the arrival of a trigger. Using an in-matrix address encoder, only hit pixels will be read out, thus offering an expected power density of less than 50 mW/cm^2 and an integration time of about 4 μs.

The backup solution is the MISTRAL design stream, based on a double-row rolling shutter architecture with end-of-column discriminators. The expected power density is about 200 mW/cm^2 with a full integration time of 30 μs.

4. Status of the monolithic pixel sensor R&D

A dedicated R&D for the pixel chip was started in 2011 covering the optimisation of the pixel collection diode and in-pixel circuitry, as well as the thickness of the epitaxial layer and its resistivity. Moreover, radiation effects have been studied and different front-end and readout architectures have been explored with the main goal to reduce the power consumption and the integration time.

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[1]www.jazzsemi.com

Table 2: Pixel chip protoytypes for the different design streams.

| Architecture | Analogue | Digital | |
		small-scale	*full-scale*
ASTRAL (MISTRAL)	MIMOSA-32-x MIMOSA-34	MIMOSA-22THR-x AROM-0/1	FSBB
ALPIDE	Explorer-0 Explorer-1	pALPIDE	pALPIDEfs

The different design teams have submitted several small and large scale prototypes, each focussing on the various building blocks of the final architectures. An overview of these prototypes is presented in Tab. 2.

4.1 Measurement results of different prototypes

Following the laboratory measurments and test beams of the MIMOSA-32 [9] prototype chips in 2012, the radiation hardness of the TowerJazz 180 nm CMOS imaging process has been validated up to the combined load of 1 Mrad and 1×10^{13} 1 MeV n_{eq}/cm^2 at 30 °C. The characterisation of the Explorer-0 in early 2013 [8] validated the positive effects of reversly biasing the charge collection diode on the signal over noise ratio both before and after irradiation with 1×10^{13} 1 MeV n_{eq}/cm^2. Furthermore it was observed that the charge collection efficiency and SNR can be improved by introducing a larger spacing between the collection n-well and the surrounding p-well.

Based on the results of these early prototypes, a new set of prototypes for both the ASTRAL and the ALPIDE design streams was submitted in spring 2013 on various starting wafer types (cf. Tab. 3). In the remainder of this section, selected recent results from the related characterisation campaigns are described.

Table 3: Features of the epitaxial layers of the different starting wafer types.

Wafer type	Epi thickness [µm]	Epi resistivity [kΩ cm]
HR-18	18	> 1
HR-20	20	6.2
HR-30	30	≈ 1
HR-40A	40	≈ 1
HR-40B	40	7.5

4.1.1 Explorer-1

The Explorer-1 is a revised version of the Explorer-0 [8] intended to further optimize the diode layout and charge collection properties as well as to study the effect of applying additional reverse bias ot the n-well diode and the susceptibility to radiation damage. The possibility to apply a reverse bias voltage V_{rb} to the substrate is a distinctive feature, which effectively enables an increase of
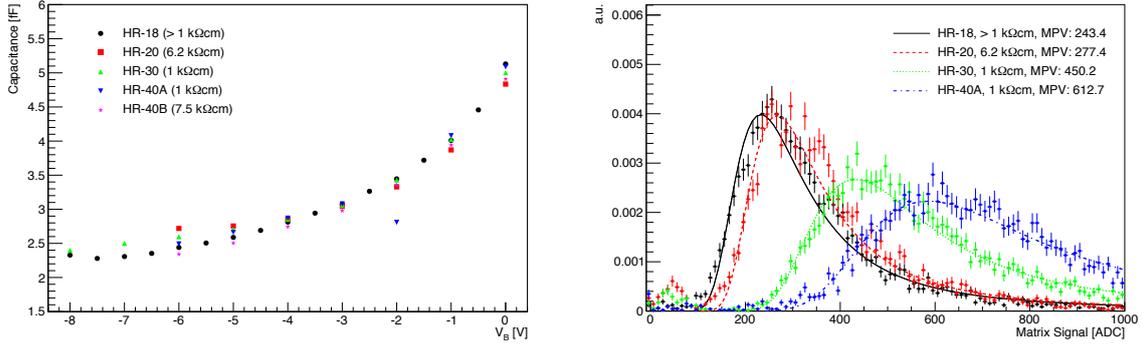
(a) Pixel input capacitance evaluated from the pixel response to 5.9 keV X-rays from an ^{55}Fe source as a function of the reverse bias voltage.

(b) Matrix signal (sum of signal of n×n^2 pixel matrix around seed pixel) measured at a reverse bias voltage of −6 V.

Figure 3: Comparison of measurement results for different starting wafer types. The data shown are taken with an Explorer-1 pixel with a 7.6 μm^2 octagonal n-well electrode and a 1.04 μm spacing between the n-well and the surrounding p-well.

signal due to a reduction of the pixel input capacitance and moreover a reduction of cluster size due to an increased depletion volume.

An increased epitaxial layer resistivity is, similarly to the biasing of the collection diode, expected to cause an increase of the depletion volume and therefore a reduction of the pixel capacitance. Considering the doping profiles of the n-well and the surrounding p-wells and deep p-wells, the magnitude of the effect will depend on the pixel design details.

The effect of the epitaxial layer resistivity on the pixel performance was studied measuring the input capacitance of the Explorer-1 pixels on different epitaxial layers. This has been performed in the laboratory combining measurements of the pixel gain and of the response to 5.9 keV X-rays from an ^{55}Fe source. Fig. 3a shows the measurement results for the 20 μm × 20 μm pixels as a function of reverse bias for five different epitaxial layers. Two main observations can be made: First, increasing the reverse bias levels entails a decrease of the pixel capacitance and second, the effects are very similar for all starting materials, suggesting only a minor influence of the epitaxial layer resistivity.

The capacitance of the sensing node can be separated into the contributions of the input routing lines and transistor C_{rt} and the diode junction capacitance C_d. Indeed increasing the reverse bias voltage reduces the junction capacitance. For the pixel under test, a cumulative value of around 5 fF is reached for $V_{rb} = 0$ V which is reduced by 50 % to about 2.5 fF for $V_{rb} = -6$ V. The minor discrepancy of the results for the various epitaxial layer resistivities is compatible with the idea that the junction capacitance C_d is dominated by the peripheral contribution between the collection n-well and the surrounding p-well with respect to the vertical contribution between the n-well and the epitaxial layer (cf. Fig. 1b). Due to the fact that the doping concentration of the p-well dominates the one of the epitaxial layer, the lateral extension of the depletion zone is significantly smaller

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[2]Due to the different cluster sizes for the different epitaxial layer thicknesses: n = 5 for HR-18 and HR-20, n = 7 for HR-30, n = 9 for HR-40A and HR-40B.
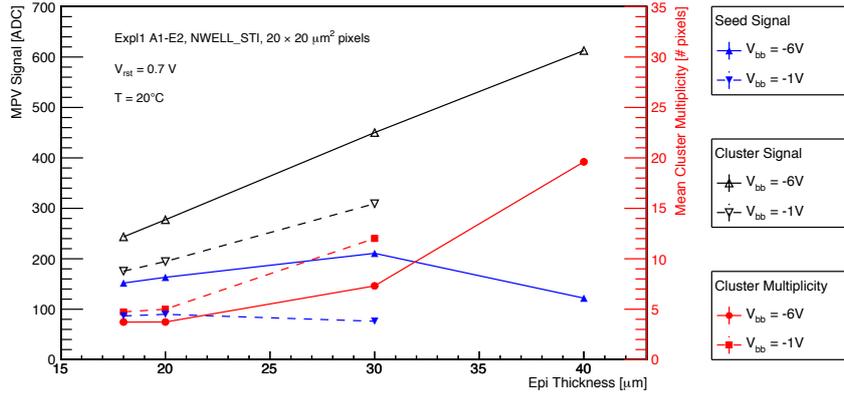
Figure 4: Comparison of Explorer-1 measurement results for different starting wafer types at a 3.2 GeV e^+ beam. The data are measured with an Explorer-1 pixel with a 7.6 µm^2 octagonal n-well electrode and a 1.04 µm spacing between the n-well and the surrounding p-well and at reverse bias voltages of -1 V and -6 V [3].

than its vertical depth. The doping concentrations of both n-well and p-well are not modified for the various starting materials. It can therefore be assumed that also the peripheral contribution to C_d and consequently the overall junction capacitance do not vary significantly depending on the epitaxial layer resistivity. The measurement results are in agreement with the simulated size of the depletion zones as reported in [3], exact predictions are very difficult to achieve since they depend on the precise knowledge of the doping profiles.

In addition to the laboratory measurements, the influence of the epitaxial layer properties was also studied in a test beam at DESY with a 3.2 GeV positrons, comparing the wafer types HR-18, HR-20, HR-30 and HR-40A. The summary for the 20 µm × 20 µm pixels is shown in Fig. 4. As expected, it is observed that the cluster signal representing the deposited charge in the sensor is proportional to the epitaxial layer thickness (cf. Fig. 3b). It can also be seen that the cluster size increases nonlinearly. These two effect have a competing influence in the process that determines the amount of charge that is collected in the seed pixel, i.e. the pixel with the largest signal within a cluster. Measurements confirmed no significant change in noise for the different starting materials. Consequently, depending on the bias conditions, the largest seed pixel SNR is obtained with different epitaxial layer thicknesses: While the optimum at a reverse bias voltage of -6 V is reached with 30 µm, it is reached with 20 µm for $V_{rb} = -1$ V.

4.1.2 MIMOSA-34

The MIMOSA-34 is a prototype with no in-pixel pre-amplification and CDS circuitry that, similarly to the chips of the Explorer family, is intended to study the charge collection properties and noise performance of a variety of pixels. The pixel dimensions range from 22 µm × 27 µm to 33 µm × 66 µm with collection n-well areas ranging from 2 µm^2 to 15 µm^2, implemented with various spacings to the surrounding p-well.

A particular focus was put on the pixels with a size of 22 µm × 33 µm, since this is the envisaged size for the pixels of the ASTRAL and MISTRAL design streams. As presented in Fig. 5a, the seed SNR of this pixel is observed to exhibit an MPV of about 44, with a small difference between
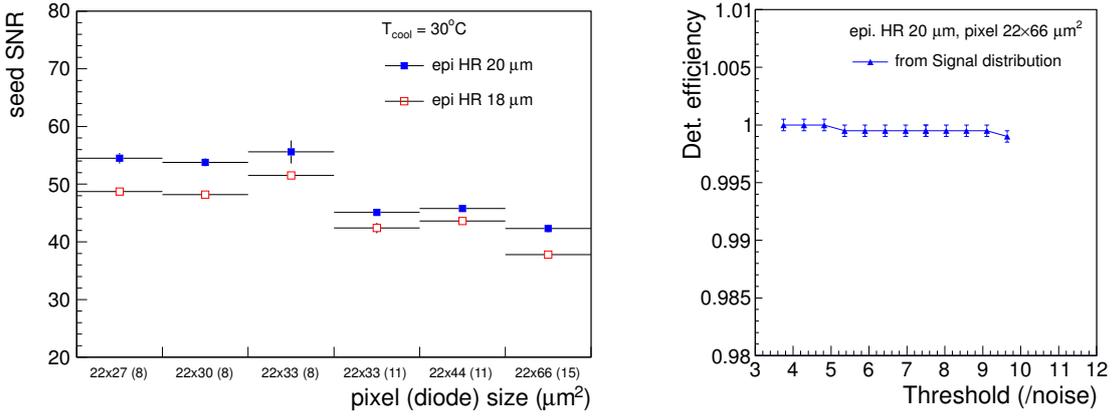
(a) Seed SNR (MPV) for various pixel geometries, for the HR-18 and HR-20 starting wafers.

(b) Detection efficiency for the $22\,\mu m \times 66\,\mu m$ pixel.

Figure 5: MIMOSA-34 measurement results [3].

the two epitaxial layers considered (HR-18 and HR-20), favouring the the HR-20. Several different larger pixel designs were also observed to show satisfactory performances in terms of CCE, seed SNR and consequently detection efficiency (cf. Fig. 5b). This offers attractive power-saving perspectives, regarding the reduced pixel density and become relevant whenever the required spatial resolution is not the main constraint.

4.1.3 MIMOSA-22THR and pALPIDE

The MIMOSA-22THR and pALPIDE are small-scale digital prototypes of the ASTRAL (MISTRAL) and the ALPIDE design stream, respectively.

The MIMOSA-22THR consists of $22\,\mu m \times 33\,\mu m$ pixels that constain in-pixel pre-amplification and CDS circuitry, and has parallel column readout and end-of-column discriminators. It exists in two versions: In version (a) the single-row readout concept used for the STAR PXL chip was reproduced and in version (b) the simultaneous readout of two rows has been addressed. Characterizing the MIMOSA-22THR, the adequancy of all main components of the MISTRAL architecture has been veryfied. Most of the results are also valid for the ASTRAL development [3].

The pALPIDE has a design close to a possible architecture of the final ALPIDE chip. It was designed to investigate the performance of the analogue front-end with in-pixel discriminator in combination with an in-matrix sparsified readout circuitry utilizing a priority encoder scheme. The pALPIDE contains one priority encoder per column, with the pixel pitch beeing $22\,\mu m$. Measurments regarding noise and spatial uniformity obtained results meeting the ITS requirements [3].

Both prototypes were in addition characterized in test beams at DESY using 3 to 6 GeV electron and positron beams. The particle detection efficiency was determined to be larger than 99 % for settings where the fake hit rate was observed to be of the order of 10^{-8}/(event × pixel). The spatial resolution of both prototypes was measured to be of the order of $5\,\mu m$. More detailed information on the chips and the related measurement results can be found in [3]. In summary, the performance of the small scale digital prototypes complies with the requirements of the final pixel chip.

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5. Conclusions

A new ALICE ITS with 7 layers of monolithic silicon pixel sensors will be installed during the LS2 in 2018/19. Different architectures for the pixel chip have been explored. Several related small-scale prototype sensors, each focussing on a particular aspect of the final chip, have been characterized in test beam and laboratory. An adequate radiation hardness of the technology has been proven, while an increased reverse bias of the pixels has shown to significantly improve the signal to noise ratio. Different epitaxial layer thicknesses have been studied in relation to the collection diode biasing conditions and optimal parameter combinations could be defined. The epitaxial layer resistivity has, in the range between $1\,k\Omega\,cm$ to $7.5\,k\Omega\,cm$, shown to have a minor influence on the performance of the set of pixels with the current layout. The performance of the small-scale digital prototypes complies with the requirements of the final pixel chip. Full-scale prototypes are currently beeing characterized in lab and test beam and first results are encouraging [10].

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